

# 74LV595

8-bit serial-in/serial-out or parallel-out shift register; 3-state

Rev. 5 — 29 September 2021

Product data sheet

## 1. General description

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The 74LV595 is an 8-bit serial-in/serial or parallel-out shift register with a storage register and 3-state outputs. Both the shift and storage register have separate clocks. The device features a serial input (DS) and a serial output (Q7S) to enable cascading and an asynchronous reset  $\overline{MR}$  input. A LOW on  $\overline{MR}$  will reset the shift register. Data is shifted on the LOW-to-HIGH transitions of the SHCP input. The data in the shift register is transferred to the storage register on a LOW-to-HIGH transition of the STCP input. If both clocks are connected together, the shift register will always be one clock pulse ahead of the storage register. Data in the storage register appears at the output whenever the output enable input ( $\overline{OE}$ ) is LOW. A HIGH on  $\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the registers. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess  $V_{CC}$ .

## 2. Features and benefits

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- Wide supply voltage range from 1.0 V to 3.6 V
- CMOS low power dissipation
- Direct interface with TTL levels
- Typical output ground bounce  $< 0.8$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Typical HIGH-level output voltage ( $V_{OH}$ ) undershoot:  $> 2$  V at  $V_{CC} = 3.3$  V and  $T_{amb} = 25$  °C
- Has a shift register with direct clear
- Output capability:
  - Parallel outputs; bus driver
  - Serial output; standard
- Latch-up performance exceeds 100 mA per JEDEC 78 Class II Level B
- Complies with JEDEC standards
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $85$  °C and  $-40$  °C to  $125$  °C

## 3. Applications

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- Serial-to-parallel data conversion
- Remote control holding register

### 4. Ordering information

Table 1. Ordering information

| Type number | Package           |         |  | Version  |
|-------------|-------------------|---------|--|----------|
|             | Temperature range | Name    | Description  |          |
| 74LV595D    | -40 °C to +125 °C | SO16    | plastic small outline package; 16 leads; body width 3.9 mm             | SOT109-1 |
| 74LV595PW   | -40 °C to +125 °C | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |

### 5. Functional diagram

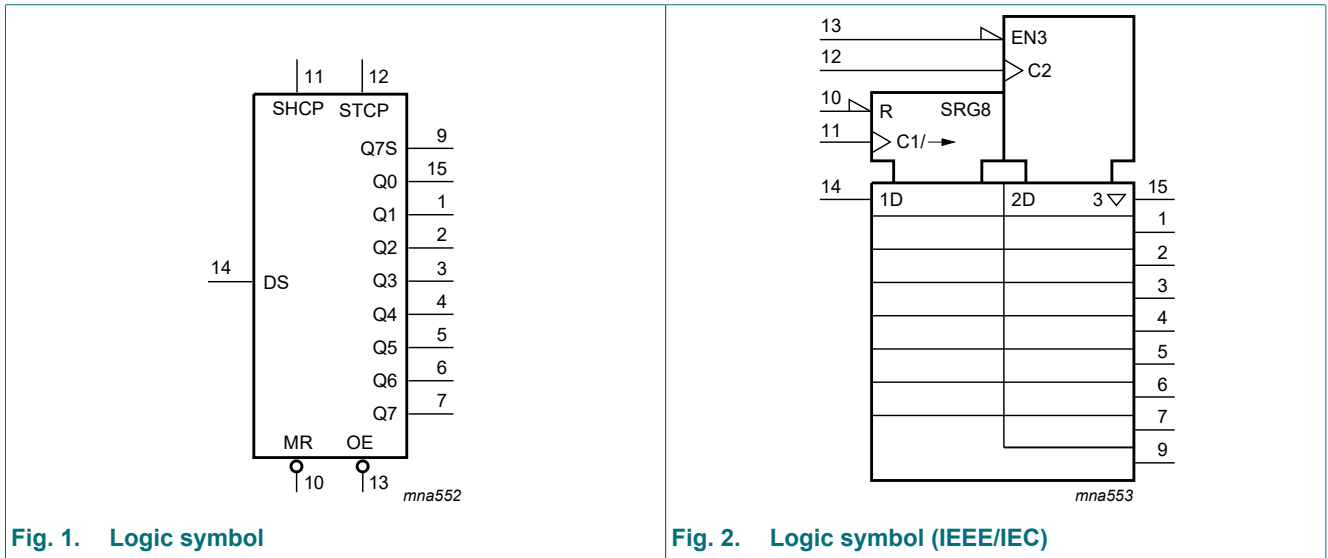


Fig. 1. Logic symbol

Fig. 2. Logic symbol (IEEE/IEC)

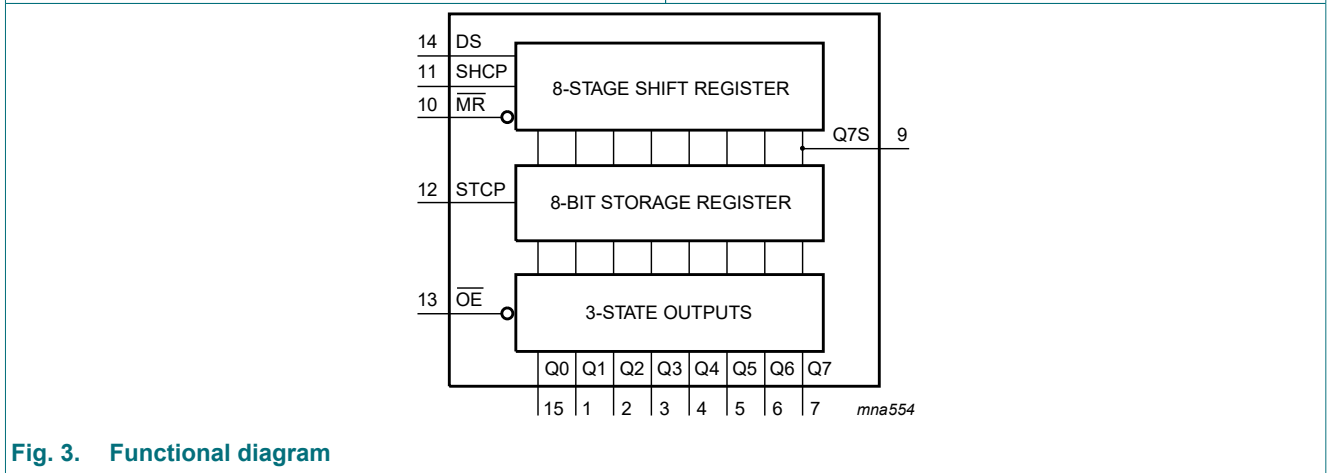


Fig. 3. Functional diagram

8-bit serial-in/serial-out or parallel-out shift register; 3-state

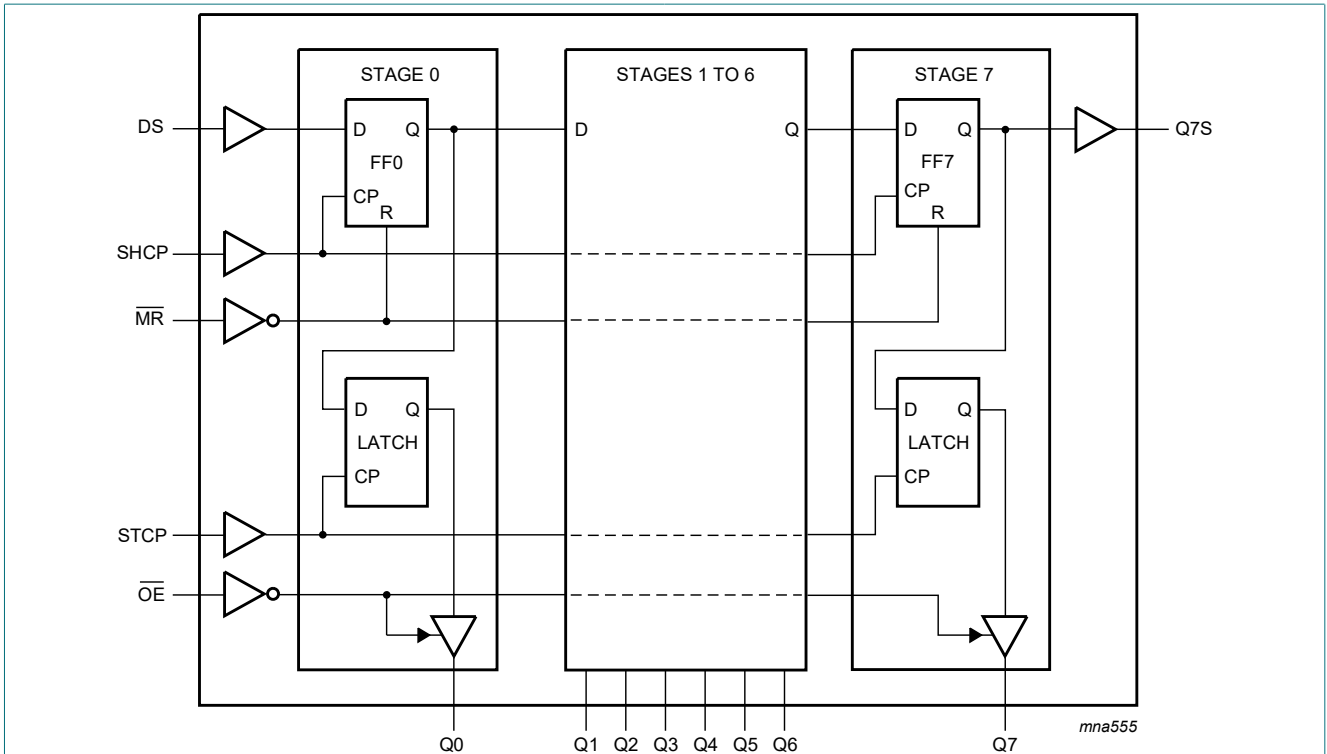


Fig. 4. Logic diagram

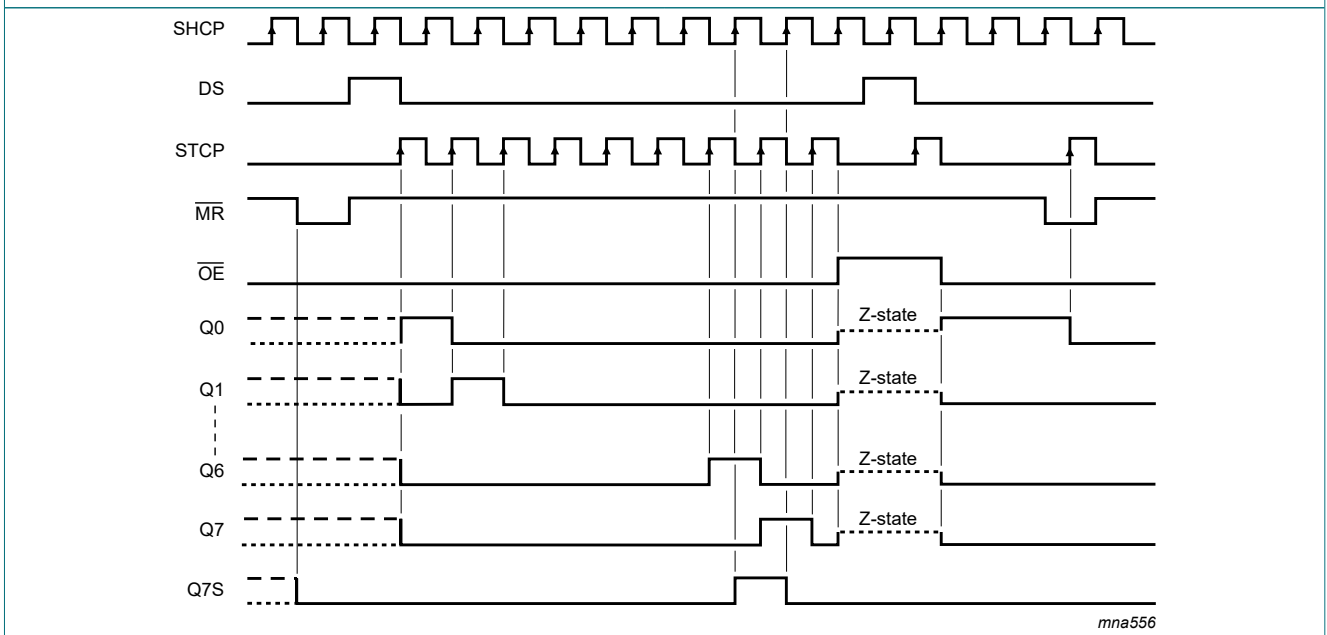


Fig. 5. Timing diagram

## 6. Pinning information

### 6.1. Pinning

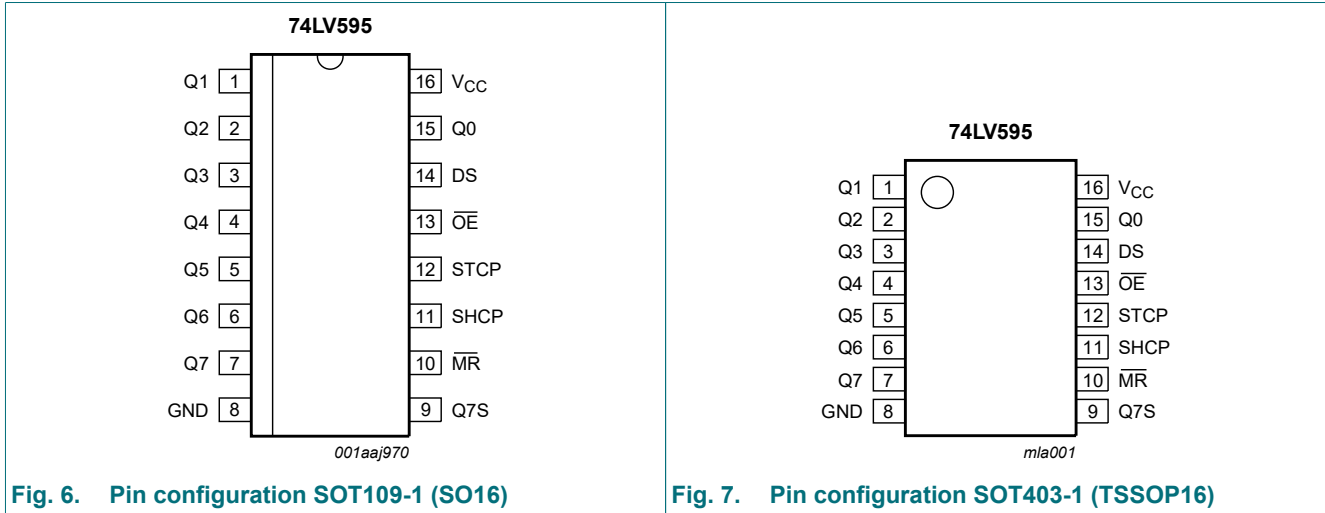


Fig. 6. Pin configuration SOT109-1 (SO16)

Fig. 7. Pin configuration SOT403-1 (TSSOP16)

### 6.2. Pin description

Table 2. Pin description

| Symbol                         | Pin                     | Description                      |
|--------------------------------|-------------------------|----------------------------------|
| Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 | 15, 1, 2, 3, 4, 5, 6, 7 | parallel data output             |
| GND                            | 8                       | ground (0 V)                     |
| Q7S                            | 9                       | serial data output               |
| MR                             | 10                      | master reset (active LOW)        |
| SHCP                           | 11                      | shift register clock input       |
| STCP                           | 12                      | storage register clock input     |
| OE                             | 13                      | output enable input (active LOW) |
| DS                             | 14                      | serial data input                |
| V <sub>CC</sub>                | 16                      | supply voltage                   |

## 7. Functional description

**Table 3. Function table**

*H = HIGH voltage state; L = LOW voltage state; ↑ = LOW-to-HIGH transition; X = don't care; NC = no change; Z = high-impedance OFF-state.*

| Input |      |    |    |    | Output |     | Function   |
|-------|------|----|----|----|--------|-----|--|
| SHCP  | STCP | OE | MR | DS | Q7S    | Qn  |  |
| X     | X    | L  | L  | X  | L      | NC  | a LOW-state on $\overline{MR}$ only affects the shift register   |
| X     | ↑    | L  | L  | X  | L      | L   | empty shift register loaded into storage register  |
| X     | X    | H  | L  | X  | L      | Z   | shift register clear; parallel outputs in high-impedance OFF-state   |
| ↑     | X    | L  | H  | H  | Q6S    | NC  | logic HIGH-state shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S). |
| X     | ↑    | L  | H  | X  | NC     | QnS | contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages  |
| ↑     | ↑    | L  | H  | X  | Q6S    | QnS | contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages                                      |

## 8. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol    | Parameter               | Conditions   | Min  | Max  | Unit |
|-----------|-------------------------|--|------|------|------|
| $V_{CC}$  | supply voltage          |  | -0.5 | +4.6 | V    |
| $I_{IK}$  | input clamping current  | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | -    | ±20  | mA   |
| $I_{OK}$  | output clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | -    | ±50  | mA   |
| $I_O$     | output current          | $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$          | -    |      |      |
|           |                         | standard driver outputs                                |      | 25   | mA   |
|           |                         | bus driver outputs                                     |      | 35   | mA   |
| $I_{CC}$  | supply current          | standard driver outputs                                |      | 50   | mA   |
|           |                         | bus driver outputs                                     |      | 70   | mA   |
| $I_{GND}$ | ground current          | standard driver outputs                                | -50  |      | mA   |
|           |                         | bus driver outputs                                     | -70  |      | mA   |
| $T_{stg}$ | storage temperature     |  | -65  | +150 | °C   |
| $P_{tot}$ | total power dissipation | $T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [1]      | -    | 500  | mW   |

- [1] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V).

| Symbol              | Parameter                           | Conditions                              | Min | Typ | Max      | Unit |
|---------------------|-------------------------------------|---|-----|-----|----------|------|
| $V_{CC}$            | supply voltage                      |   | 1.0 | 3.3 | 3.6      | V    |
| $V_I$               | input voltage                       |   | 0   | -   | $V_{CC}$ | V    |
| $V_O$               | output voltage                      |   | 0   | -   | $V_{CC}$ | V    |
| $T_{amb}$           | ambient temperature                 |   | -40 | -   | +125     | °C   |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.0\text{ V to }2.0\text{ V}$ | -   | -   | 500      | ns/V |
|                     |                                     | $V_{CC} = 2.0\text{ V to }2.7\text{ V}$ | -   | -   | 200      | ns/V |
|                     |                                     | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ | -   | -   | 100      | ns/V |

## 10. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol  | Parameter                 | Conditions   | -40 °C to +85 °C |         |     | -40 °C to +125 °C |     | Unit          |
|---|---------------------------|--|------------------|---------|-----|-------------------|-----|---------------|
|   |                           |  | Min              | Typ [1] | Max | Min               | Max |               |
| $V_{IH}$  | HIGH-level input voltage  | $V_{CC} = 1.2\text{ V}$  | 0.9              | -       | -   | 0.9               | -   | V             |
|   |                           | $V_{CC} = 2.0\text{ V}$  | 1.4              | -       | -   | 1.4               | -   | V             |
|   |                           | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$  | 2.0              | -       | -   | 2.0               | -   | V             |
| $V_{IL}$  | LOW-level input voltage   | $V_{CC} = 1.2\text{ V}$  | -                | -       | 0.3 | -                 | 0.3 | V             |
|   |                           | $V_{CC} = 2.0\text{ V}$  | -                | -       | 0.6 | -                 | 0.6 | V             |
|   |                           | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$  | -                | -       | 0.8 | -                 | 0.8 | V             |
| $V_{OH}$  | HIGH-level output voltage | all outputs; $V_I = V_{IH}$ or $V_{IL}$ ;<br>$I_O = -100\ \mu\text{A}$                           |                  |         |     |                   |     |               |
|   |                           | $V_{CC} = 1.2\text{ V}$  | -                | 1.2     | -   | -                 | -   | V             |
|   |                           | $V_{CC} = 2.0\text{ V}$  | 1.8              | 2.0     | -   | 1.8               | -   | V             |
|   |                           | $V_{CC} = 2.7\text{ V}$  | 2.5              | 2.7     | -   | 2.5               | -   | V             |
|   |                           | $V_{CC} = 3.0\text{ V}$  | 2.8              | 3.0     | -   | 2.8               | -   | V             |
|   |                           | standard outputs; $V_I = V_{IH}$ or $V_{IL}$ ;<br>$I_O = -6\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$ | 2.4              | 2.82    | -   | 2.2               | -   | V             |
| bus outputs; $V_I = V_{IH}$ or $V_{IL}$ ;<br>$I_O = -8\text{ mA}$ ; $V_{CC} = 3.0\text{ V}$ | 2.4                       | 2.82   | -                | 2.2     | -   | V                 |     |               |
| $V_{OL}$  | LOW-level output voltage  | all outputs; $V_I = V_{IH}$ or $V_{IL}$ ;<br>$I_O = 100\ \mu\text{A}$                            |                  |         |     |                   |     |               |
|   |                           | $V_{CC} = 1.2\text{ V}$  | -                | 0       | -   | -                 | -   | V             |
|   |                           | $V_{CC} = 2.0\text{ V}$  | -                | 0       | 0.2 | -                 | 0.2 | V             |
|   |                           | $V_{CC} = 2.7\text{ V}$  | -                | 0       | 0.2 | -                 | 0.2 | V             |
|   |                           | $V_{CC} = 3.0\text{ V}$  | -                | 0       | 0.2 | -                 | 0.2 | V             |
|   |                           | standard driver outputs $V_{CC} = 3.0\text{ V}$ ;<br>$I_O = 6\text{ mA}$                         | -                | 0.25    | 0.4 | -                 | 0.5 | V             |
| bus driver outputs $V_{CC} = 3.0\text{ V}$ ;<br>$I_O = 8\text{ mA}$                         | -                         | 0.20   | 0.4              | -       | 0.5 | V                 |     |               |
| $I_I$   | input leakage current     | $V_{CC} = 3.6\text{ V}$ ; $V_I = 5.5\text{ V}$ or GND  | -                | -       | 1.0 | -                 | 1.0 | $\mu\text{A}$ |

## 8-bit serial-in/serial-out or parallel-out shift register; 3-state

| Symbol           | Parameter                 | Conditions   | -40 °C to +85 °C |         |     | -40 °C to +125 °C |     | Unit |
|------------------|---------------------------|--|------------------|---------|-----|-------------------|-----|------|
|                  |                           |  | Min              | Typ [1] | Max | Min               | Max |      |
| I <sub>OZ</sub>  | OFF-state output current  | V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 3.6 V | -                | -       | 5   | -                 | 10  | μA   |
| I <sub>CC</sub>  | supply current            | V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A                                 | -                | -       | 20  | -                 | 160 | μA   |
| ΔI <sub>CC</sub> | additional supply current | per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> - 0.6 V                              | -                | -       | 500 | -                 | 850 | μA   |
| C <sub>I</sub>   | input capacitance         |  | -                | 3.5     | -   | -                 | -   | pF   |

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 13.

| Symbol  | Parameter         | Conditions                                      | -40 °C to +85 °C |         |     | -40 °C to +125 °C |     | Unit |
|---|-------------------|---|------------------|---------|-----|-------------------|-----|------|
|   |                   |   | Min              | Typ [1] | Max | Min               | Max |      |
| t <sub>pd</sub>                                 | propagation delay | SHCP to Q7S; see Fig. 8 [2]                     |                  |         |     |                   |     |      |
|   |                   | V <sub>CC</sub> = 1.2 V                         | -                | 95      | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 2.0 V                         | -                | 32      | 61  | -                 | 75  | ns   |
|   |                   | V <sub>CC</sub> = 2.7 V                         | -                | 24      | 45  | -                 | 55  | ns   |
|   |                   | V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF | -                | 15      | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | -                | 18      | 36  | -                 | 44  | ns   |
|   |                   | STCP to Qn; see Fig. 9 [2]                      |                  |         |     |                   |     |      |
|   |                   | V <sub>CC</sub> = 1.2 V                         | -                | 100     | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 2.0 V                         | -                | 34      | 65  | -                 | 77  | ns   |
|   |                   | V <sub>CC</sub> = 2.7 V                         | -                | 25      | 48  | -                 | 56  | ns   |
|   |                   | V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF | -                | 16      | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | -                | 19      | 38  | -                 | 45  | ns   |
|   |                   | MR to Q7S; see Fig. 11                          |                  |         |     |                   |     |      |
|   |                   | V <sub>CC</sub> = 1.2 V                         | -                | 85      | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 2.0 V                         | -                | 29      | 56  | -                 | 66  | ns   |
|   |                   | V <sub>CC</sub> = 2.7 V                         | -                | 21      | 41  | -                 | 49  | ns   |
| V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF | -                 | 14  | -                | -       | -   | ns                |     |      |
| V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | -                 | 16  | 33               | -       | 33  | ns                |     |      |
| t <sub>en</sub>                                 | enable time       | OE to Qn; see Fig. 12 [4]                       |                  |         |     |                   |     |      |
|   |                   | V <sub>CC</sub> = 1.2 V                         | -                | 85      | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 2.0 V                         | -                | 29      | 56  | -                 | 66  | ns   |
|   |                   | V <sub>CC</sub> = 2.7 V                         | -                | 21      | 41  | -                 | 49  | ns   |
|   |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | -                | 16      | 33  | -                 | 39  | ns   |
| t <sub>dis</sub>                                | disable time      | OE to Qn; see Fig. 12 [5]                       |                  |         |     |                   |     |      |
|   |                   | V <sub>CC</sub> = 1.2 V                         | -                | 65      | -   | -                 | -   | ns   |
|   |                   | V <sub>CC</sub> = 2.0 V                         | -                | 24      | 40  | -                 | 49  | ns   |
|   |                   | V <sub>CC</sub> = 2.7 V                         | -                | 18      | 32  | -                 | 37  | ns   |
|   |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | -                | 14      | 26  | -                 | 30  | ns   |

## 8-bit serial-in/serial-out or parallel-out shift register; 3-state

| Symbol           | Parameter         | Conditions                                      | -40 °C to +85 °C |         |     | -40 °C to +125 °C |     | Unit |
|------------------|-------------------|---|------------------|---------|-----|-------------------|-----|------|
|                  |                   |   | Min              | Typ [1] | Max | Min               | Max |      |
| t <sub>w</sub>   | pulse width       | SHCP, HIGH or LOW; see Fig. 8                   |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 34               | 10      | -   | 41                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 25               | 8       | -   | 30                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 20               | 6       | -   | 24                | -   | ns   |
|                  |                   | STCP, HIGH or LOW; see Fig. 9                   |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 34               | 7       | -   | 41                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 25               | 5       | -   | 30                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 20               | 4       | -   | 24                | -   | ns   |
|                  |                   | MR LOW; see Fig. 11                             |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 34               | 10      | -   | 41                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 25               | 8       | -   | 30                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 20               | 6       | -   | 24                | -   | ns   |
| t <sub>su</sub>  | set-up time       | DS to SHCP; see Fig. 10                         |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 1.2 V                         | -                | 40      | -   | -                 | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 26               | 14      | -   | 31                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 19               | 10      | -   | 23                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 15               | 8       | -   | 18                | -   | ns   |
|                  |                   | SHCP to STCP; see Fig. 9                        |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 1.2 V                         | -                | 40      | -   | -                 | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 26               | 14      | -   | 31                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 19               | 10      | -   | 23                | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 15               | 8       | -   | 18                | -   | ns   |
| t <sub>h</sub>   | hold time         | DS to SHCP; see Fig. 10                         |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 1.2 V                         | -                | -10.0   | -   | -                 | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 5.0              | -4.0    | -   | 5.0               | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 5.0              | -3.0    | -   | 5.0               | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 5.0              | -2.0    | -   | 5.0               | -   | ns   |
| t <sub>rec</sub> | recovery time     | MR to SHCP; see Fig. 11                         |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 1.2 V                         | -                | -35     | -   | -                 | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 5.0              | -12.0   | -   | 5.0               | -   | ns   |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 5.0              | -9.0    | -   | 5.0               | -   | ns   |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 5.0              | -7.0    | -   | 5.0               | -   | ns   |
| f <sub>max</sub> | maximum frequency | SHCP or STCP; see Fig. 8 and Fig. 9             |                  |         |     |                   |     |      |
|                  |                   | V <sub>CC</sub> = 2.0 V                         | 14.0             | 40.0    | -   | 12                | -   | MHz  |
|                  |                   | V <sub>CC</sub> = 2.7 V                         | 19.0             | 58.0    | -   | 16                | -   | MHz  |
|                  |                   | V <sub>CC</sub> = 3.3 V; C <sub>L</sub> = 15 pF | -                | 77      | -   | -                 | -   | MHz  |
|                  |                   | V <sub>CC</sub> = 3.0 V to 3.6 V [3]            | 24.0             | 70.0    | -   | 20                | -   | MHz  |

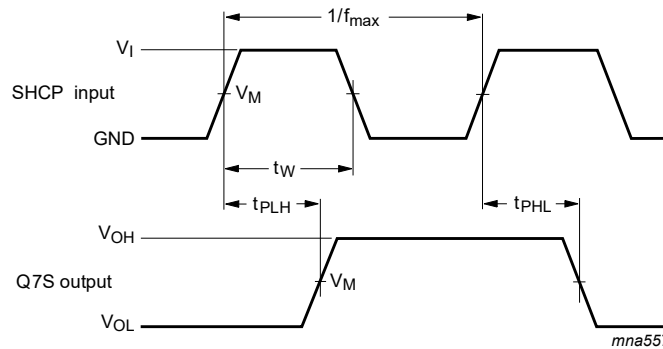


8-bit serial-in/serial-out or parallel-out shift register; 3-state

| Symbol          | Parameter                     | Conditions  | -40 °C to +85 °C |         |     | -40 °C to +125 °C |     | Unit |
|-----------------|-------------------------------|---|------------------|---------|-----|-------------------|-----|------|
|                 |                               |   | Min              | Typ [1] | Max | Min               | Max |      |
| C <sub>PD</sub> | power dissipation capacitance | V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 3.0 V [6] | -                | 115     | -   | -                 | -   | pF   |

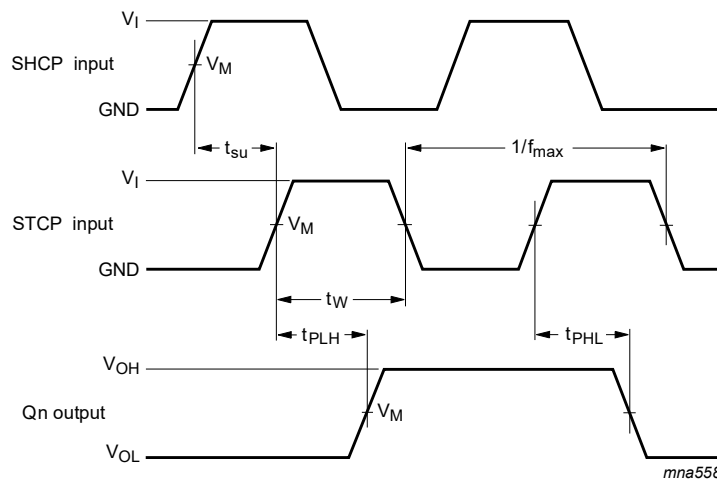
- [1] Typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.
- [3] Typical value measured at V<sub>CC</sub> = 3.3 V.
- [4] t<sub>en</sub> is the same as t<sub>PZH</sub> and t<sub>PZL</sub>.
- [5] t<sub>dis</sub> is the same as t<sub>PHZ</sub> and t<sub>PLZ</sub>.
- [6] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\sum(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.

11.1. Waveforms and test circuit



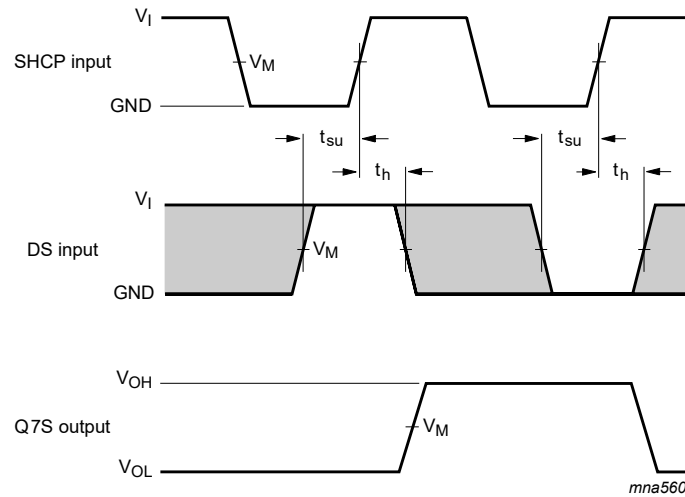
Measurement points are given in [Table 8](#).  
 V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drops that occur with the output load.

**Fig. 8. The shift clock (SHCP) to serial data output (Q7S) propagation delays, the shift clock pulse width and maximum shift clock frequency**



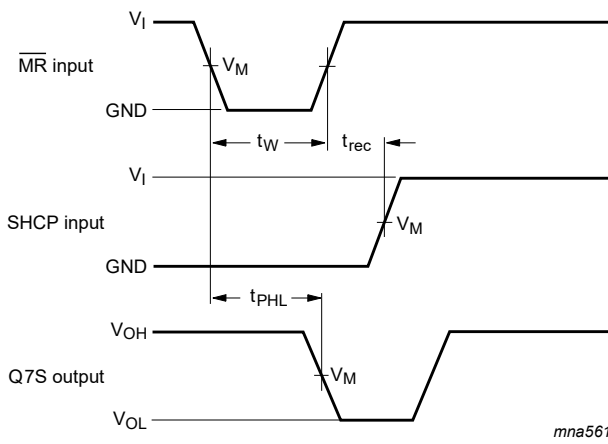
Measurement points are given in [Table 8](#).  
 V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drops that occur with the output load.

**Fig. 9. The storage clock (STCP) to parallel data output (Qn) propagation delays, the storage clock pulse width and the shift clock to storage clock set-up time**



Measurement points are given in [Table 8](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig. 10. The data set-up and hold times for the serial data input (DS)**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig. 11. The master reset ( $\overline{MR}$ ) pulse width, the master reset to serial data output (Q7S) propagation delays and the master reset to shift clock (SHCP) recovery time**

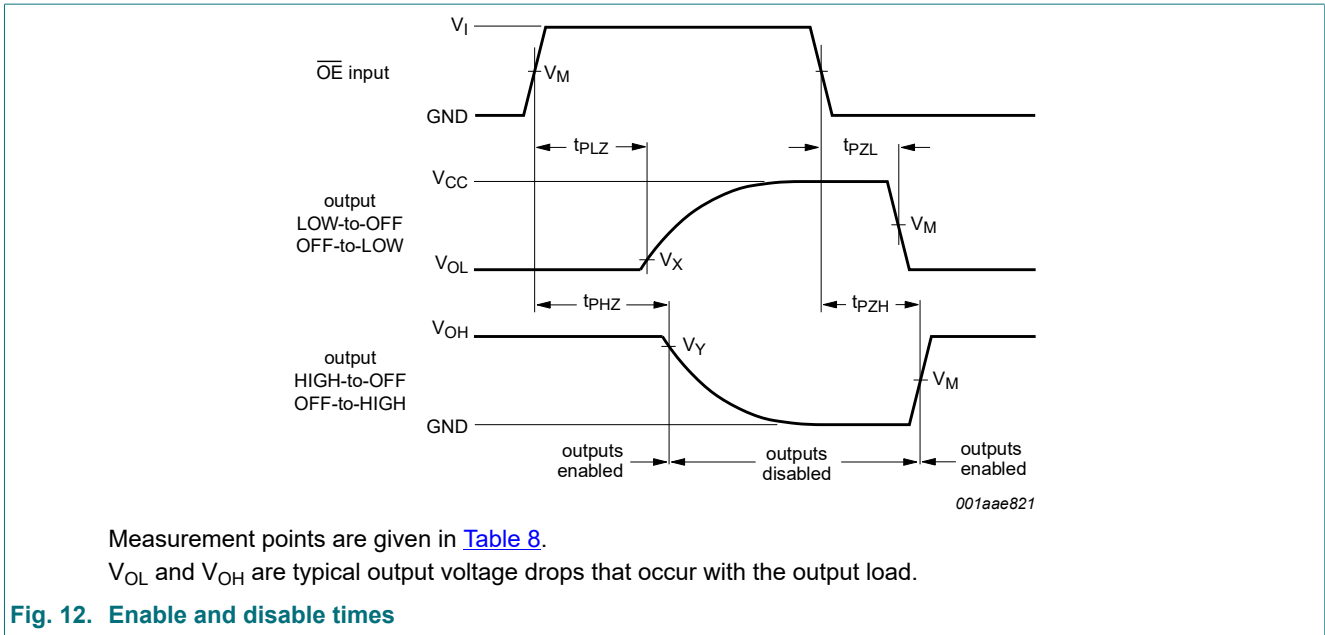
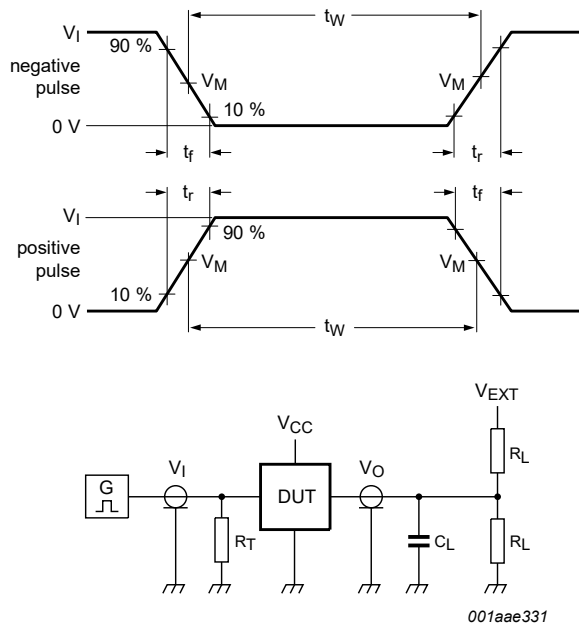


Table 8. Measurement points

| Supply voltage             | Input       | Output      |                         |                         |
|----------------------------|-------------|-------------|-------------------------|-------------------------|
| $V_{CC}$                   | $V_M$       | $V_M$       | $V_X$                   | $V_Y$                   |
| $V_{CC} < 2.7\text{ V}$    | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL} + 0.1V_{CC}$    | $V_{OH} - 0.1V_{CC}$    |
| $V_{CC} \geq 2.7\text{ V}$ | 1.5 V       | 1.5 V       | $V_{OL} + 0.3\text{ V}$ | $V_{OH} - 0.3\text{ V}$ |

8-bit serial-in/serial-out or parallel-out shift register; 3-state



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 13. Test circuit for measuring switching times**

**Table 9. Test data**

| Supply voltage | Input    |               | Load  |              | $V_{EXT}$          |                    |                    |
|----------------|----------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| $V_{CC}$       | $V_I$    | $t_r, t_f$    | $C_L$ | $R_L$        | $t_{PLH}, t_{PHL}$ | $t_{PLZ}, t_{PZL}$ | $t_{PHZ}, t_{PZH}$ |
| < 2.7 V        | $V_{CC}$ | $\leq 2.5$ ns | 50 pF | 1 k $\Omega$ | open               | $2V_{CC}$          | GND                |
| 2.7 V to 3.6 V | 2.7 V    | $\leq 2.5$ ns | 50 pF | 1 k $\Omega$ | open               | $2V_{CC}$          | GND                |

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig. 14. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



Fig. 15. Package outline SOT403-1 (TSSOP16)

## 13. Abbreviations

Table 10. Abbreviations

| Acronym | Description                             |
|---------|---|
| CMOS    | Complementary Metal Oxide Semiconductor |
| DUT     | Device Under Test                       |
| ESD     | ElectroStatic Discharge                 |
| HBM     | Human Body Model                        |
| MM      | Machine Model                           |
| TTL     | Transistor-Transistor Logic             |

## 14. Revision history

Table 11. Revision history

| Document ID    | Release date  | Data sheet status  | Change notice | Supersedes  |
|----------------|---|--------------------|---------------|-------------|
| 74LV595 v.5    | 20210929  | Product data sheet | -             | 74LV595 v.4 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type number 74LV595DB (SOT338-1/SSOP16) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> <li><a href="#">Section 8</a>: Derating values for <math>P_{tot}</math> total power dissipation updated.</li> </ul> |                    |               |             |
| 74LV595 v.4    | 20160318  | Product data sheet | -             | 74LV595 v.3 |
| Modifications: | <ul style="list-style-type: none"> <li>Type number 74LV595N (SOT38-4) removed.</li> </ul>   |                    |               |             |
| 74LV595 v.3    | 20090421  | Product data sheet | -             | 74LV595 v.2 |
| Modifications: | <ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>   |                    |               |             |
| 74LV595 v.2    | 980402  | Product data sheet | -             | 74LV595 v.1 |
| 74LV595 v.1    | 970606  | Product data sheet | -             | -           |

## 15. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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## Contents

|  |           |
|--|-----------|
| <b>1. General description</b> .....              | <b>1</b>  |
| <b>2. Features and benefits</b> .....            | <b>1</b>  |
| <b>3. Applications</b> .....                     | <b>1</b>  |
| <b>4. Ordering information</b> .....             | <b>2</b>  |
| <b>5. Functional diagram</b> .....               | <b>2</b>  |
| <b>6. Pinning information</b> .....              | <b>4</b>  |
| 6.1. Pinning.....                                | 4         |
| 6.2. Pin description.....                        | 4         |
| <b>7. Functional description</b> .....           | <b>5</b>  |
| <b>8. Limiting values</b> .....                  | <b>5</b>  |
| <b>9. Recommended operating conditions</b> ..... | <b>6</b>  |
| <b>10. Static characteristics</b> .....          | <b>6</b>  |
| <b>11. Dynamic characteristics</b> .....         | <b>7</b>  |
| 11.1. Waveforms and test circuit.....            | 9         |
| <b>12. Package outline</b> .....                 | <b>13</b> |
| <b>13. Abbreviations</b> .....                   | <b>15</b> |
| <b>14. Revision history</b> .....                | <b>15</b> |
| <b>15. Legal information</b> .....               | <b>16</b> |

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