CD74FCT240, CD74FCT240AT, CD74FCT244, CD74FCT244AT

BiCMOS FCT Interface Logic, Octal Buffers/Line Drivers, Three-State

January 1997

NOT RECOMMENDED FOR NEW DESIGNS
Use CMOS Technology

Features

- Buffered Inputs
- Typical Propagation Delay: 4.1ns at V_{CC} = 5V, T_A = 25°C
- CD74FCT240, CD74FCT240AT
  - Inverting
- CD74FCT244, CD74FCT244AT
  - Noninverting
- SCR Latchup Resistant BiCMOS Process and Circuit Design
- CD74FCTXXX Types - Speed of Bipolar FAST™/AS/S
- CD74FCTXXXAT Types - 30% Faster Than FAST™/AS/S with Significantly Reduced Power Consumption
- 64mA Output Sink Current
- Output Voltage Swing Limited to 3.7V at V_{CC} = 5V
- Controlled Output Edge Rates
- Input/Output Isolation to V_{CC}
- BiCMOS Technology with Low Quiescent Power

Description

The CD74FCT240, CD74FCT240AT, CD74FCT244, and CD74FCT244AT three-state octal buffers/line drivers use a small geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output HIGH level to two diode drops below V_{CC}. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes V_{CC} bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capabile of sinking 64mA.

The CD74FCT240, CD74FCT240AT, CD74FCT244, and CD74FCT244AT have active LOW output enables ($\overline{1OE}$, $\overline{2OE}$).

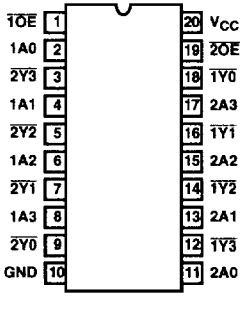
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT240E	0 to 70	20 Ld PDIP	E20.3
CD74FCT240ATE	0 to 70	20 Ld PDIP	E20.3
CD74FCT244E	0 to 70	20 Ld PDIP	E20.3
CD74FCT244ATE	0 to 70	20 Ld PDIP	E20.3
CD74FCT240M	0 to 70	20 Ld SOIC	M20.3
CD74FCT244M	0 to 70	20 Ld SOIC	M20.3
CD74FCT240SM	0 to 70	20 Ld SSOP	M20.209
CD74FCT244SM	0 to 70	20 Ld SSOP	M20.209

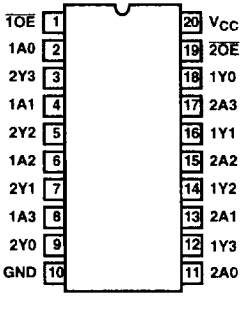
NOTE: When ordering the suffix M and SM packages, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Pinouts

CD74FCT240, CD74FCT240AT
(PDIP, SOIC, SSOP)
TOP VIEW



CD74FCT244, CD74FCT244AT
(PDIP, SOIC, SSOP)
TOP VIEW



8 BiCMOS FCT PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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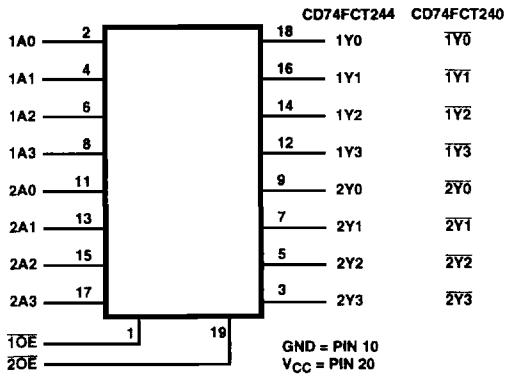
File Number **2227.4**

Functional Diagram



CD74FCT240, CD74FCT240AT TRUTH TABLE

CD74FCT240, CD74FCT240AT		
INPUT	INPUT	OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	$\overline{Y}$
L	L	H
L	H	L
H	X	Z

CD74FCT244, CD74FCT244AT TRUTH TABLE

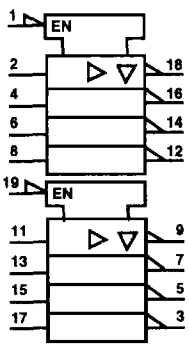
CD74FCT244, CD74FCT244AT		
INPUT	INPUT	OUTPUT
$\overline{1OE}$, $\overline{2OE}$	A	Y
L	L	L
L	H	H
H	X	Z

NOTE:

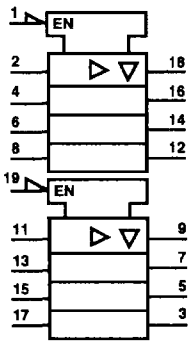
1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = HIGH Impedance

IEC Logic Symbols

CD74FCT240, CD74FCT240AT



CD74FCT244, CD74FCT244AT



Absolute Maximum Ratings

DC Supply Voltage (V_{CC}) . . . . . -0.5V to 6.0V
DC Input Diode Current, I_{IK} (for V_I < -0.5V) . . . . . -20mA
DC Output Diode Current, I_{OK} (for V_O < -0.5V) . . . . . -50mA
DC Output Sink Current per Output Pin, I_O 70mA
DC Output Source Current per Output Pin, I_O . . . . . -30mA
DC V_{CC} Current (I_{CC}) 140mA
DC Ground Current (I_{GND}) 528mA

Operating Conditions

Operating Temperature Range . . . . . 0 to 70°C
Supply Voltage Range, V_{CC} . . . . . 4.75V to 5.25V
DC Input Voltage, V_I . . . . . 0 to V_{CC}
DC Output Voltage, V_O . . . . . 0 to ≤ V_{CC}
Input Rise and Fall Slew Rate, dt/dv . . . . . 0 to 10ns/V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
PDIP Package	135
SOIC Package	125
SSOP Package	130

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC and SSOP-Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications Temperature Range, 0°C to 70°C, V_{CC} Max = 5.25V, V_{CC} Min = 4.75V

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	AMBIENT TEMPERATURE (T_A)						UNITS
					25°C		0°C to 70°C		(244E ONLY) -55°C to 125°C		
		V_I	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	V_{IH}			4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V_{IL}			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-15	Min	2.4	-	2.4	-	-	-	V
Low Level Output Voltage	V_{OL}	V_{IH} or V_{IL}	64	Min	-	0.55	-	0.55	-	-	V
High Level Input Current	I_{IH}	V_{CC}		Max	-	0.1	-	1	-	1	µA
Low Level Input Current	I_{IL}	GND		Max	-	-0.1	-	-1	-	-1	µA
Three-State Leakage Current	I_{OZH}	V_{CC}		Max	-	0.5	-	10	-	10	µA
	I_{OZL}	GND		Max	-	-0.5	-	-10	-	-10	µA
Short Circuit Output Current (Note 3)	I_{OS}	V_{CC} or GND V_O = 0		Max	-60	-	-60	-	-60	-	mA
Input Clamp Voltage	V_{IK}	V_{CC} or GND	-18	Min	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MSI	I_{CC}	V_{CC} or GND	0	Max	-	8	-	80	-	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔI_{CC}	3.4V (Note 4)		Max	-	1.6	-	1.6	-	2	mA

NOTES:

3. Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
4. Inputs that are not measured are at V_{CC} or GND.
5. FCT Input Loading: All inputs are 1 unit load. Unit load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 1.6mA max at 70°C.

Switching Specifications t_r, t_f = 2.5ns, C_L = 50pF, R_L - See Figure 2

PARAMETER	SYMBOL	V_{CC} (V)	CD74FCT240, CD74FCT244			CD74FCT240AT, CD74FCT244AT			UNITS
			25°C	0°C to 70°C		25°C	0°C to 70°C		
			TYP	MIN	MAX	TYP	MIN	MAX	
Propagation Delays Data to Outputs	t_{PLH}, t_{PHL}								
CD74FCT240/AT		5 (Note 6)	5	1.5	8	4.4	1.5	5.6	ns
CD74FCT244/AT		5	4.5	1.5	6.5	3.8	1.5	5.3	µs
Output Enable Times	t_{PZL}, t_{PZH}								
CD74FCT240/AT		5	7	1.5	10	4.7	1.5	6.2	µs
CD74FCT244/AT		5	6	1.5	8	4.8	1.5	6.5	ns
Output Disable Times	t_{PLZ}, t_{PHZ}								
CD74FCT240/AT		5	6	1.5	9.5	4	1.5	5.6	µs
CD74FCT244/AT		5	5	1.5	7	4.5	1.5	5.8	µs
Power Dissipation Capacitance (Note 7)	C_{PD}								
CD74FCT240/AT		-	38 Typical			38 Typical			pF
CD74FCT244/AT		-	35 Typical			35 Typical			pF
Min (Valley) V_{OHV} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OHV} (Figure 1)	5	0.5	-	-	0.5	-	-	V
Max (Peak) V_{OLP} During Switching of Other Outputs (Output Under Test Not Switching)	V_{OLP} (Figure 1)	5	1	-	-	1			V
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Three-State Output Capacitance	C_O	-	-	-	15	-	-	15	pF

NOTES:

6. 5V: Min is at 5.25V for 0°C to 70°C, Max is at 4.75V for 0°C to 70°C, Typ is at 5V.
7. C_{PD}, measured per function, is used to determine the dynamic power consumption. P_D (per package) = $V_{CC} I_{CC} + \Sigma (V_{CC}^2 f_i C_{PD} + V_O^2 f_O C_L + V_{CC} \Delta I_{CC} D)$ where:
   V_{CC} = Supply Voltage
   ΔI_{CC} = Flow Through Current X Unit Load
   C_L = Output Load Capacitance
   D = Duty Cycle of Input High
   f_O = Output Frequency
   f_i = Input Frequency

Test Circuits and Waveforms

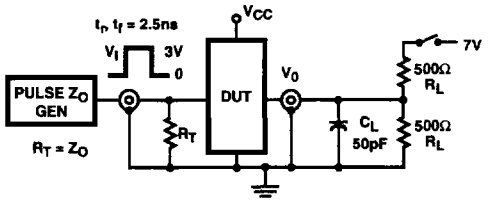


FIGURE 1. TEST CIRCUIT

SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}, Open Drain	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

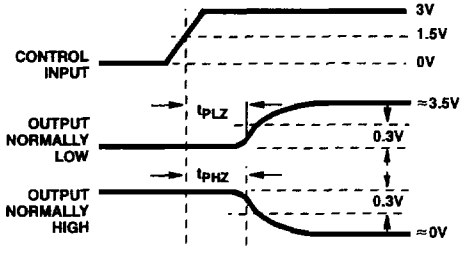


FIGURE 2. OUTPUT DISABLE TIMES

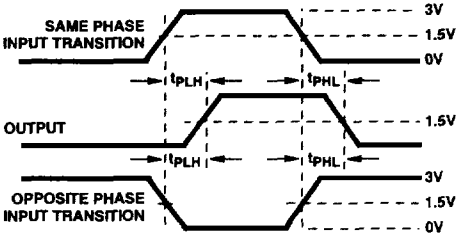


FIGURE 3. PROPAGATION DELAY TIMES