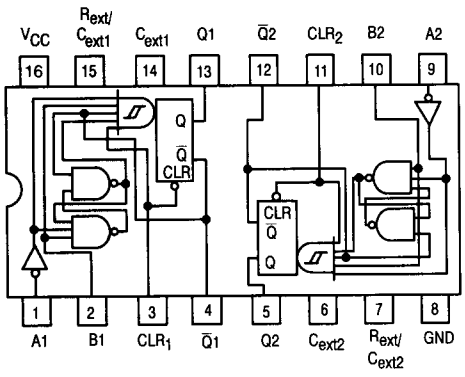
MOTOROLA

Dual Monostable Multivibrator, Schmitt Trigger Inputs With Enable

ELECTRICALLY TESTED PER:
MIL-M-38510/31402

- 54LS221 is a Dual Highly Stable One-Shot
- Overriding Clear Terminates Output Pulse
- Pin Out is Identical to 54LS123

CONNECTION DIAGRAM



Type	Typical Power Dissipation	Maximum Output Pulse Length
54LS221	23 mW	49 s

(Each Monostable)

FUNCTION TABLE

Inputs			Outputs	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⊓	⊓
H	↓	H	⊓	⊓
↑	L	H	⊓	⊓

Military 54LS221

MPO

AVAILABLE AS:

1) JAN: JM38510/31402BXA
2) SMD: 7604201
3) 883: 54LS221/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
A1	1	1	1	VCC
B1	2	2	2	VCC
CLR1	3	3	3	GND
Q̄1	4	4	4	VCC
Q2	5	5	5	OPEN
Cext2	6	6	6	OPEN
Rext2	7	7	7	GND
GND	8	8	8	GND
A2	9	9	9	VCC
B2	10	10	10	VCC
CLR2	11	11	11	GND
Q̄2	12	12	12	VCC
Q1	13	13	13	OPEN
Cext1	14	14	14	OPEN
Rext1	15	15	15	GND
VCC	16	16	16	VCC

BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX

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FUNCTIONAL DESCRIPTION

Each multivibrator of the 'LS221 features a negative-transition triggered input and a positive-transition triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a voltage level and is not related to the transition time of the input pulse. Schmitt-trigger input circuitry for B input allows jitter-free triggering for inputs as slow as 1.0 volt/second, providing the circuit with excellent noise immunity. A high immunity to V_{CC} noise is also provided by internal latching circuitry.

Once triggered, the outputs are independent of further transitions of the inputs and are a function of the timing components. The output pulses can be terminated by the overriding clear. Input pulse width may be of any duration relative to the output pulse width. Output pulse width may be varied from 35 nanoseconds to a maximum of 70 s by choosing appropriate timing components. With $R_{ext} = 2.0\ k\Omega$ and $C_{ext} = 0$, a typical output pulse of 30 nanoseconds is achieved. Output rise and fall times are independent of the pulse length.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

Jitter-free operation is maintained over the full temperature and V_{CC} ranges for greater than six decades of timing capacitance (10 pF to 10 μF), and greater than one decade of timing resistance (2.0 to 70 kΩ for the 54LS221). Pulse width is defined by the relationship: $t_{W(out)} = C_{ext}R_{ext} \ln 2.0 \approx 0.7\, C_{ext}R_{ext}$. If pulse cutoff is not critical, capacitance up to 1000 μF and resistance as low as 1.4 kΩ may be used. The range of jitter-free pulse width is extended if V_{CC} is 5.0 V and 25°C temperature.

Once in the pulse trigger mode, the output pulse width is determined by $t_W = R_{ext}C_{ext} \ln 2$, as long as R_{ext} and C_{ext} are within their minimum and maximum values and the duty is less than 50%. This pulse width is essentially independent of V_{CC} and temperature variations. Output pulse widths varies typically no more than ± 0.5% from device to device.

If the duty cycle, defined as being 100 * t_W/T where T is the period of the input pulses, rises above 50%, the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes the output pulse width to vary in length, or jitter. To reduce jitter to a minimum, R_{ext} should be as long as possible. (Jitter is independent of C_{ext}.) With $R_{ext} = 100$ k, jitter is not appreciable until the duty cycle approaches 90%.

Although the 'LS221 is pin-for-pin compatible with the 'LS123, it should be remembered that they are not functionally identical. The 'LS123 is retriggerable so that the output is dependent upon the input transitions once it is high. This is not the case for the 'LS221. Also note that it is recommended to externally ground the 'LS123 C_{ext} pin. However, this cannot be done on the 'LS221.

The 54LS221 is a dual, monolithic, non-retriggerable, high-stability one shot. The output pulse width, t_W can be varied over 9 decades of timing by proper selection of the external timing components, R_{ext} and C_{ext}.

Pulse triggering occurs at a voltage level and is, therefore, independent of the input slew rate. Although all three inputs have this Schmitt-trigger effect, only the B input should be used for very long transition triggers (≥ 1.0 μ V/s). High immunity to V_{CC} noise (typically 1.5 V) is achieved by internal latching circuitry. However, standard V_{CC} bypassing is strongly recommended.

The 'LS221 has four basic modes of operation.

Clear Mode:	If the clear input is held low, regardless of the previous output state and other input states, the Q output is low.
Inhibit Mode:	If either the A input is high or the B input is low, once the Q output goes low, it cannot be retriggered by other inputs.
Pulse Trigger Mode:	This occurs when none of the other modes are in effect and the Q output is low, A proper transition by either the CLR, A or B input, as shown in the truth table, will cause the Q output to go high and remain high for the pulse time t_W. Once triggered, as long as the output remains high, all input transitions (except for Clear) are ignored.
Overriding Clear Mode:	If the Q output is high, it may be forced low by bringing the clear input low.

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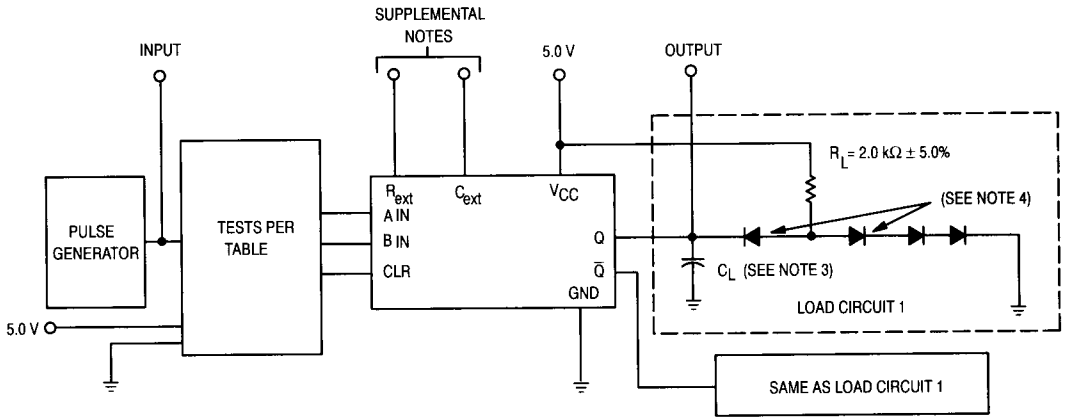
AC TEST CIRCUIT



SUPPLEMENTAL NOTES:

1. R_{ext} = 1.4 kΩ minimum to 70 kΩ maximum, connected to V_{CC}; $C_{ext} \leq$ 1,000 µF, connected to R_{ext} terminal.
2. R_{ext} = 2.0 kΩ ± 10%, connected to V_{CC}; C_{ext} = 80 pF ± 10%, connected to R_{ext} terminal.
3. R_{ext} = 10 kΩ ± 10%, connected to V_{CC}; C_{ext} = 100 pF ± R_{ext} terminal.
4. R_{ext} = 10 k Ω ±10%, connected to V_{CC}; C_{ext} = 1.0 µF ± 10%, connected to R_{ext} terminal.
5. R_{ext} = 2.0 kΩ ± 10%, connected to V_{CC}.
6. R_{ext} = 10 kΩ ± 10%, connected to V_{CC}; $C_{ext} \geq$ 45 pF connected to R_{ext} terminal.

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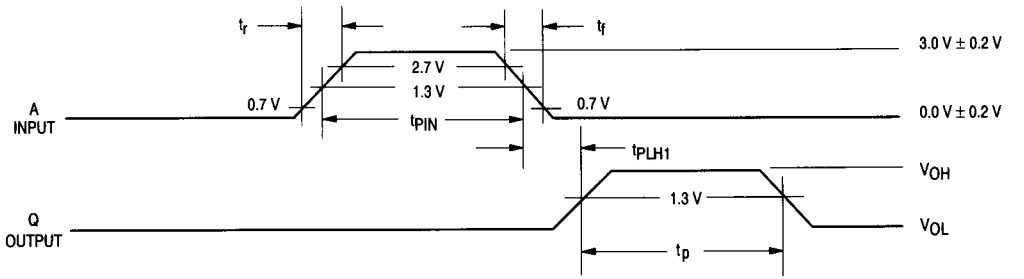
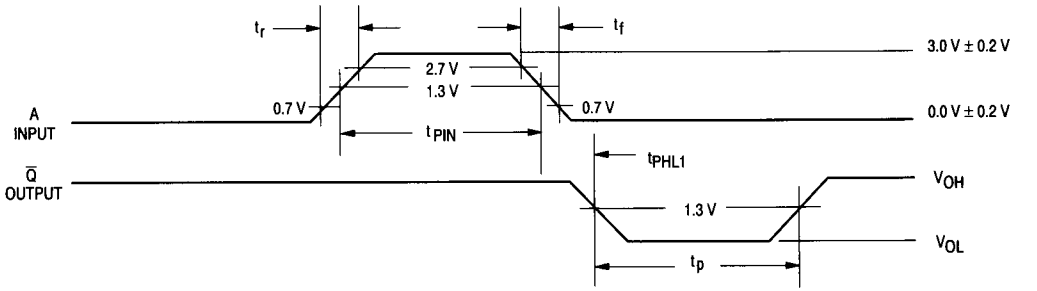
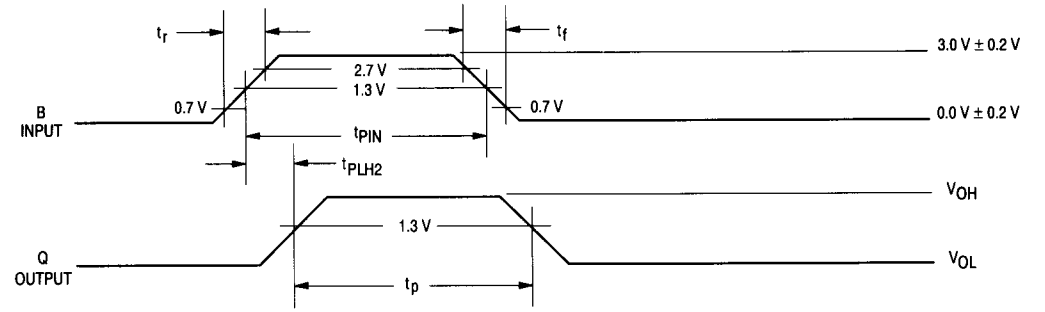
t_{PLH1} AND t_p WAVEFORMS



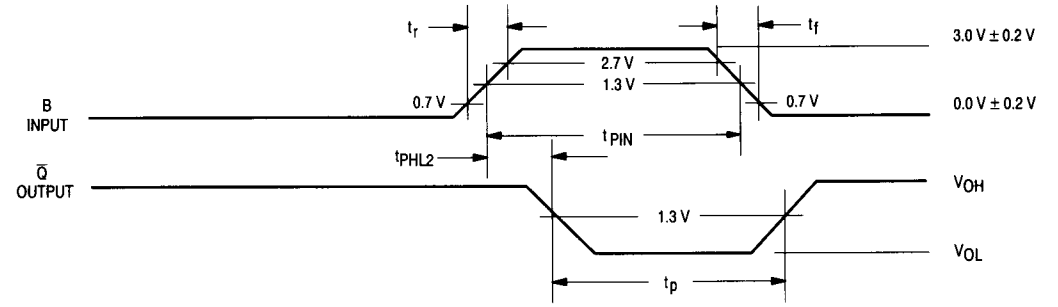
t_p AND t_{PHL1} WAVEFORMS



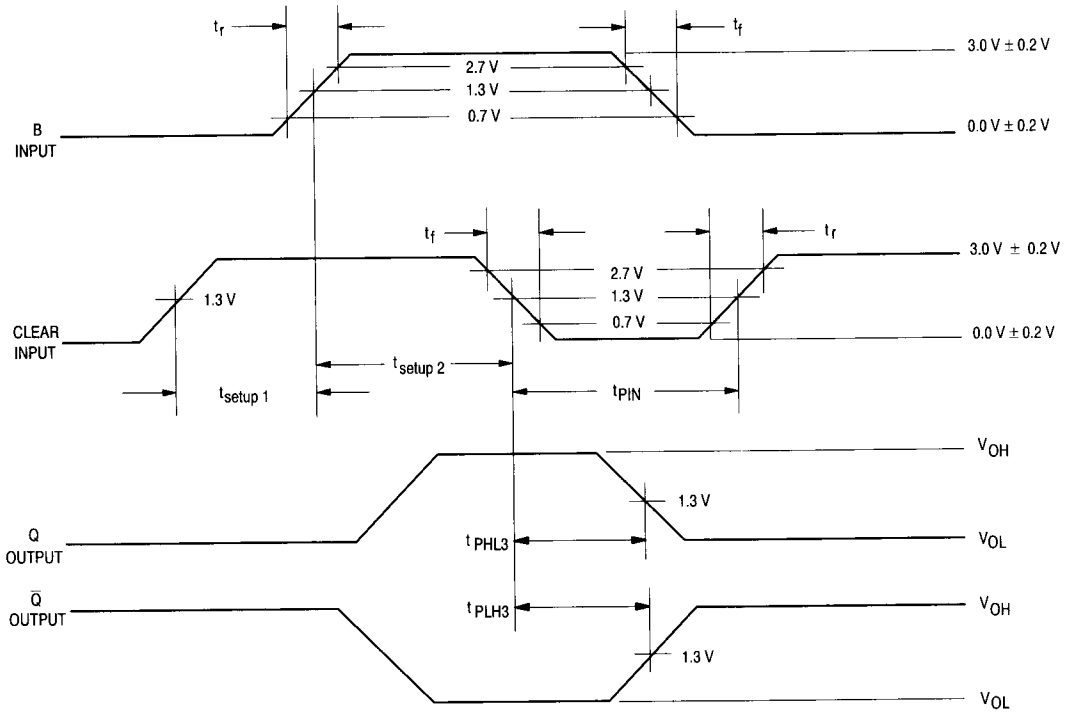
t_{PLH2} AND t_p WAVEFORMS



t_p AND t_{PHL2} WAVEFORMS



t_{PLH3} AND t_{PHL3} WAVEFORMS



NOTES:

1. Pulse generator has the following characteristics: PRR ≤ 1.0 MHz, $t_{pin} \geq 40$ ns, $t_f \leq 6.0$ ns, $t_r \leq 15$ ns, t_{setup} (clear inactive) = 15 ns and Z_{OUT} = 50 Ω.
2. See table notes for R_{ext}, C_{ext} values.
3. C_L = 50 pF ± 10%, including scope probe, wiring and stray capacitance, without package in test fixture.
4. R_L = 2.0 kΩ ± 5.0%. All diodes are 1N3064 or 1N916.
5. Load circuit on a given output is only required where the specific test in table indicates "OUT" on that output.
6. t_{setup} (max) shall be (≤ 50% of the typical output pulse width for the actual C_{ext} used).
7. Voltage measurements are to be made with respect to network ground terminal.

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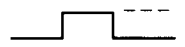
Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		− 55°C			
	Static Parameters:	Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V_{CC} = 4.5 V, I_{OH} = − 0.4 mA, V_{IH} = 2.0 V, B = 0.7 V, A = (See Note 1), CLR = 2.0 V, R_{ext}/C_{ext} = open.
V_{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V_{CC} = 4.5 V, I_{OH} = 4.0 mA, V_{IH} = 2.0 V, B = 0.7 V, A = (See Note 1), CLR = 2.0 V, R_{ext}/C_{ext} = open.
V_{IC}	Input Clamping Voltage		− 1.5					V	V_{CC} = 4.5 V, I_{IN} = − 18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, A = 2.7 V or 4.5 V, CLR = GND or 2.7 V, B = 2.7 V or GND.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 5.5 V, A = 5.5 V or 4.5 V, B = 5.5 V or GND, CLR = GND or 5.5 V.
$I_{IL(A)}$	Logical "0" Input Current	− 100	− 340	− 100	− 340	− 100	− 340	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input = 4.5 V, CLR = 4.5 V.
$I_{IL(B)}$	Logical "0" Input Current	− 160	− 440	− 160	− 440	− 160	− 440	µA	V_{CC} = 5.5 V, V_{IN} = 0.4 V, other input = GND, CLR = 4.5 V.
$I_{IL(CLR)}$	Logical "0" Input Current	− 200	− 680	− 200	− 680	− 200	− 680	µA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other input = GND, CLR = GND.
I_{OS}	Output Short Circuit Current	− 15	− 100	− 15	− 100	− 15	− 100	mA	V_{CC} = 5.5 V, A = (See Note 1) or GND, V_{OUT} = GND, B & CLR = 4.5 V.
I_{CCH}	Power Supply Current		11		11		11	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, B = GND.
I_{CCL}	Power Supply Current		27		27		27	mA	V_{CC} = 5.5 V, V_{IN} = 5.5 V, A = (See Note 1).
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V_{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V_{CC} = 5.0 V, V_{INL} = 0.4 V, and V_{INH} = 2.5 V.

NOTE:

1. Apply input pulse  2.5 V min/5.5 V max, 0.0 V

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1} t_{PHL1}	Propagation Delay /Data-Output A_n to Q_n or $\overline{Q}_n$	5.0 —	85 80	5.0 —	128 123	5.0 —	128 123	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH1} t_{PLH1}	Propagation Delay /Data-Output A_n to Q_n or $\overline{Q}_n$	5.0 —	75 70	5.0 —	113 108	5.0 —	113 108	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL2} t_{PHL2}	Propagation Delay /Data-Output B_n to Q_n or $\overline{Q}_n$	5.0 —	70 65	5.0 —	105 100	5.0 —	105 100	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH2} t_{PLH2}	Propagation Delay /Data-Output B_n to Q_n or $\overline{Q}_n$	5.0 —	60 55	5.0 —	90 85	5.0 —	90 85	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PHL3} t_{PHL3}	Propagation Delay /Data-Output Clear to Q_n or $\overline{Q}_n$	5.0 —	60 55	5.0 —	90 85	5.0 —	90 85	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_{PLH3} t_{PLH3}	Propagation Delay /Data-Output Clear to Q_n or $\overline{Q}_n$	5.0 —	70 65	5.0 —	105 100	5.0 —	105 100	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ. V_{CC} = 5.0 V, C_L = 15 pF, R_L = 2.0 kΩ
t_p1	Pulse Width	20	75	20	91	20	91	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_p2	Pulse Width	70	160	70	195	70	195	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_p3	Pulse Width	600	775	600	850	600	850	ns	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.
t_p5	Pulse Width	5.7	8.0	5.5	8.5	5.5	8.5	ms	V_{CC} = 5.0 V, C_L = 50 pF, R_L = 2.0 kΩ.

NOTE:
1. The limits specified for C_L = 15 pF are guaranteed but not tested.

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