



FXMAR2102 Dual-Supply, 2-Bit Voltage Translator / Isolator for I²C Applications

Features

- Bi-Directional Interface between Any Two Levels: 1.65 V to 5.5 V
- No Direction Control Needed
- Internal 10 KΩ Pull-Up Resistors
- System GPIO Resources Not Required when OE Tied to V_{CCA}
- I²C-Bus[®] Isolation
- A/B Port V_{OL} = 175 mV (Typical), V_{IL} = 150 mV, I_{OL} = 6 mA
- Open-Drain Inputs / Outputs
- Works in Push Pull Environment
- Accommodates Standard-Mode and Fast-Mode I²C-Bus Devices
- Supports I²C Clock Stretching & Multi-Master
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Non-Preferential Power-Up; Either V_{CC} Can Power-Up First
- Outputs Switch to 3-State if Either V_{CC} is at GND
- Tolerant Output Enable: 5 V
- Packaged in 8-Terminal Leadless MicroPak™ (1.6 mm x 1.6 mm) and Ultrathin MLP (1.2 mm x 1.4 mm)
- ESD Protection Exceeds:
 - B Port: 8 kV HBM ESD (vs. GND & vs. V_{CCB})
 - All Pins: 4 kV HBM ESD (per JESD22-A114)
 - 2 kV CDM (per JESD22-C101)

Description

The FXMAR2102 is a high-performance configurable dual-voltage-supply translator for bi-directional voltage translation over a wide range of input and output voltages levels. The FXMAR2102 also works in a push-pull environment.

It is intended for use as a voltage translator between I²C-Bus[®] compliant masters and slaves. Internal 10 KΩ pull-up resistors are provided.

The device is designed so the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi-directional A/B-port voltage translation between any two levels from 1.65 V to 5.5 V. V_{CCA} can equal V_{CCB} from 1.65 V to 5.5 V. Either V_{CC} can be powered-up first. Internal power-down control circuits place the device in 3-state if either V_{CC} is removed.

The two ports of the device have automatic direction-sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package | Packing Method |
|--------------|-----------------------------|----------|---------------------------------------|-----------------------------|
| FXMAR2102L8X | -40 to +85°C | BU | 8-Lead MicroPak™, 1.6 mm Wide | 5000 Units on Tape and Reel |
| FXMAR2102UMX | | | 8-Lead Ultrathin MLP, 1.2 mm x 1.4 mm | |

Block Diagram

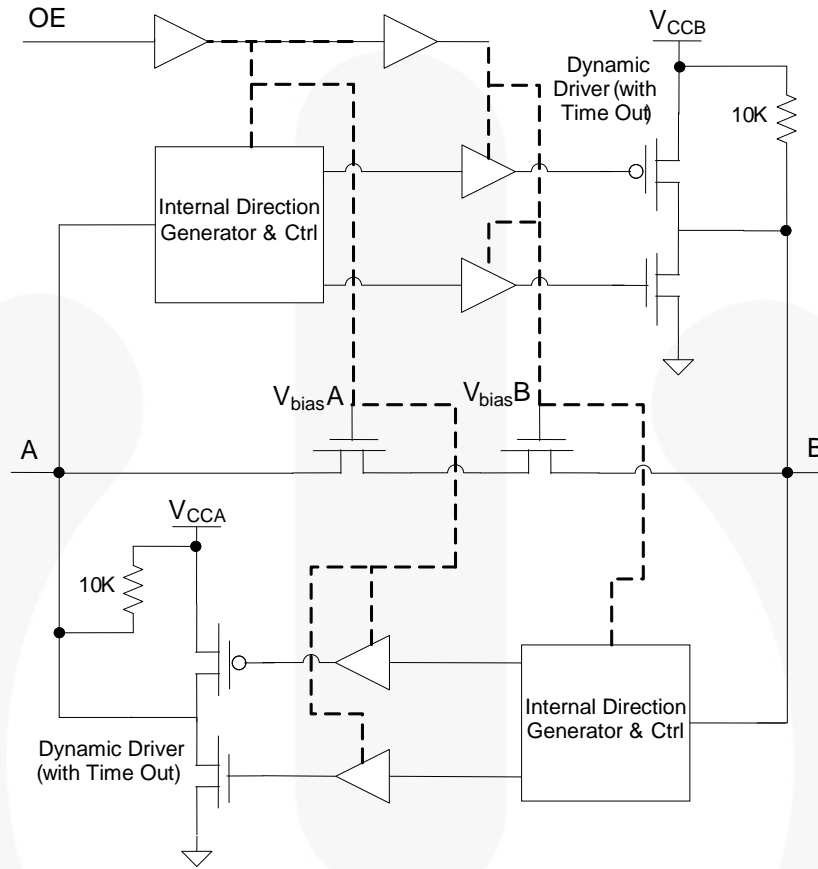


Figure 1. Block Diagram, 1 of 2 Channels



Pin Configuration

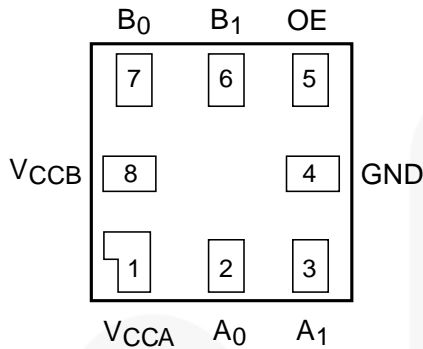


Figure 2. MicroPak™ (Top-Through View)

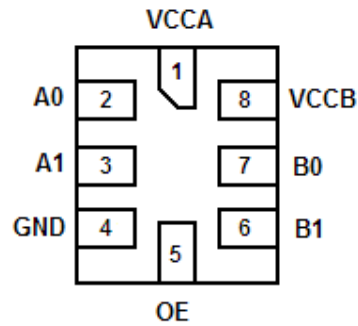


Figure 3. UMLP (Top-Through View)

Pin Definitions

| Pin # | Name | Description |
|-------|---------------------------------|----------------------------------|
| 1 | V _{CCA} | A-Side Power Supply |
| 2, 3 | A ₀ , A ₁ | A-Side Inputs or 3-State Outputs |
| 4 | GND | Ground |
| 5 | OE | Output Enable Input |
| 6, 7 | B ₁ , B ₀ | B-Side Inputs or 3-State Outputs |
| 8 | V _{CCB} | B-Side Power Supply |

Truth Table

| Control | Outputs |
|-------------------|------------------|
| OE ⁽¹⁾ | |
| LOW Logic Level | 3-State |
| HIGH Logic Level | Normal Operation |

Note:

1. If the OE pin is driven LOW, the FXMAR2102 is disabled and the A₀, A₁, B₀, and B₁ pins (including dynamic drivers) are forced into 3-state and all four 10 KΩ internal pull-up resistors are decoupled from their respective V_{CC}.

Absolute Maximum Ratings

Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Units |
|--------------------|--|--|------|------------------|-------|
| V_{CCA}, V_{CCB} | Supply Voltage | | -0.5 | 7.0 | V |
| V_{IN} | DC Input Voltage | A Port | -0.5 | 7.0 | |
| | | B Port | -0.5 | 7.0 | |
| | | Control Input (OE) | -0.5 | 7.0 | |
| V_O | Output Voltage ⁽²⁾ | A_n Outputs 3-State | -0.5 | 7.0 | V |
| | | B_n Outputs 3-State | -0.5 | 7.0 | |
| | | A_n Outputs Active | -0.5 | $V_{CCA} + 0.5V$ | |
| | | B_n Outputs Active | -0.5 | $V_{CCB} + 0.5V$ | |
| I_{IK} | DC Input Diode Current | At $V_{IN} < 0V$ | | -50 | mA |
| I_{OK} | DC Output Diode Current | At $V_O < 0V$ | | -50 | mA |
| | | At $V_O > V_{CC}$ | | +50 | |
| I_{OH} / I_{OL} | DC Output Source/Sink Current | | -50 | +50 | mA |
| I_{CC} | DC V_{CC} or Ground Current per Supply Pin | | | ±100 | mA |
| P_D | Power Dissipation | At 400 KHz | | 0.129 | mW |
| T_{STG} | Storage Temperature Range | | -65 | +150 | °C |
| ESD | Electrostatic Discharge Capability | Human Body Model, B-Port Pins | | 8 | kV |
| | | Human Body Model, All Pins (JESD22-A114) | | 4 | |
| | | Charged Device Mode, JESD22-C101 | | 2 | |

Note:

2. I_O absolute maximum rating must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | | Min. | Max. | Units |
|--------------------|--------------------------------|----------------------|------|-----------|-------|
| V_{CCA}, V_{CCB} | Power Supply Operating | | 1.65 | 5.50 | V |
| V_{IN} | Input Voltage ⁽³⁾ | A-Port | 0 | 5.5 | V |
| | | B-Port | 0 | 5.5 | |
| | | Control Input (OE) | 0 | V_{CCA} | |
| Θ_{JA} | Thermal Resistance | 8-Lead MicroPak™ | | 279 | C°/W |
| | | 8-Lead Ultrathin MLP | | 302 | |
| T_A | Free Air Operating Temperature | | -40 | +85 | °C |

Note:

3. All unused inputs and I/O pins must be held at V_{CCI} or GND. V_{CCI} is the V_{CC} associated with the input side.

Functional Description

Power-Up / Power-Down Sequencing

FXM translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high-impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull-down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power-up/-down. The size of the pull-down resistor is based upon the current-sinking capability of the device driving the OE pin.

The recommended power-up sequence is:

1. Apply power to the first V_{CC} .
2. Apply power to the second V_{CC} .
3. Drive the OE input HIGH to enable the device.

The recommended power-down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V_{CC} .
3. Remove power from the other V_{CC} .

Note:

4. Alternatively, the OE pin can be hardwired to V_{CCA} to save GPIO pins. If OE is hardwired to V_{CCA} , either V_{CC} can be powered up or down first.

Application Circuit

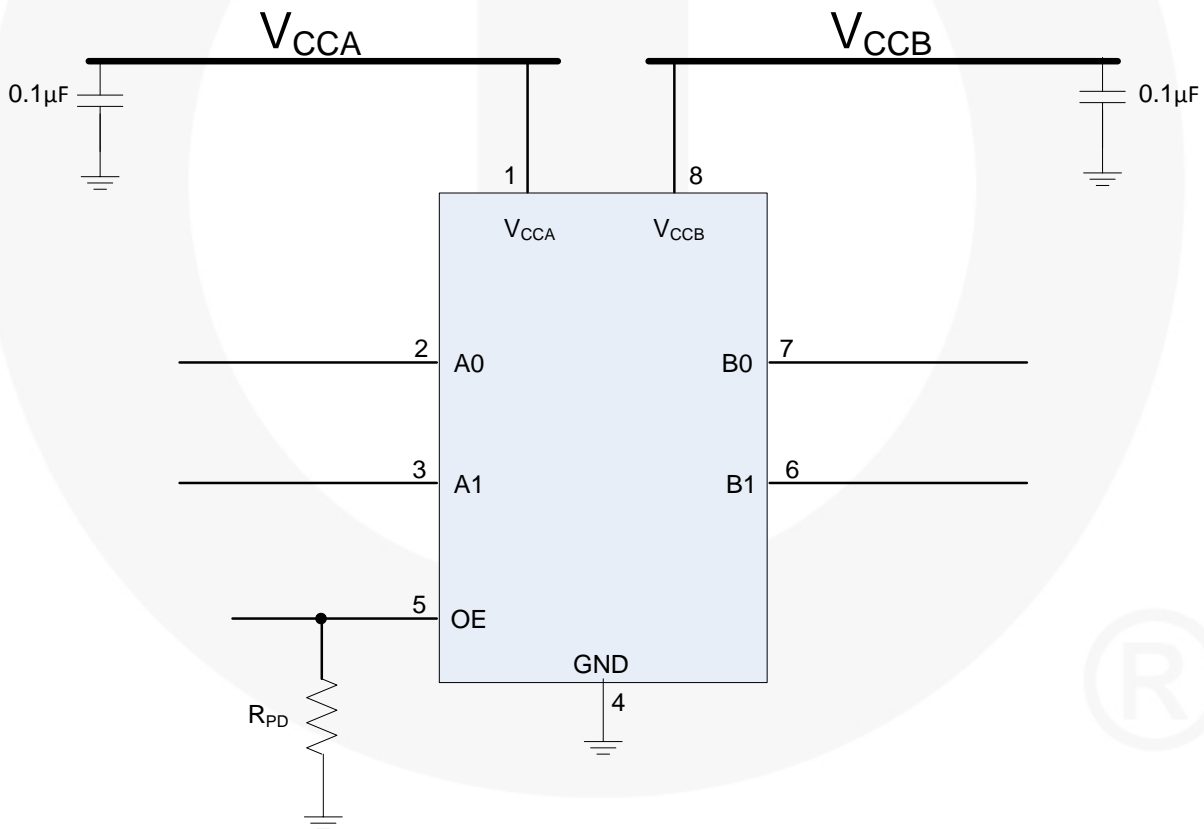


Figure 4. Application Circuit

Application Information

The FXMAR2102 has open-drain I/Os and includes a total of four 10 K Ω internal pull-up resistors (R_{PU}) on each of the four data I/O pins, as shown in Figure 4. If a pair of data I/O pins (A_n/B_n) is not used, both pins should be disconnected, eliminating unwanted current flow through the internal RPU's. External RPU's can be added to the I/Os to reduce the total RPU value, depending on the total bus capacitance. The designer is free to lower the total pull-up resistor value to meet the maximum I²C edge rate per the I²C specification (UM10204 rev. 03, June 19, 2007). For example, according to the I²C specification, the maximum edge rate (30% - 70%) during Fast Mode (400 kbit/s) is 300 ns. If the bus capacitance is approaching the maximum 400 pF, a lower total R_{PU} value helps keep the rise time below 300 ns (Fast Mode). Likewise, the I²C specification also specifies a minimum Serial Clock Line High Time of 600 ns during Fast Mode (400 KHz). Lowering the total RPU also helps increase the SCL High Time. If the bus capacitance approaches 400 pF, it may make sense to use the FXMA2102, which does not contain internal RPU's. Then calculate the ideal external R_{PU} value.

Note:

- Section 7.1 of the I²C specification provides an excellent guideline for pull-up resistor sizing.

Theory of Operation

The FXMAR2102 is designed for high-performance level shifting and buffer / repeating in an I²C application. Figure 1 shows that each bi-directional channel contains two series-Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I²C application where auto-direction is a necessity.

For example, during the following three I²C protocol events:

- Clock Stretching
- Slave's ACK Bit (9th bit = 0) following a Master's Write Bit (8th bit = 0)
- Clock Synchronization and Multi-Master Arbitration

the bus direction needs to change from master-to-slave to slave-to-master without the occurrence of an edge. If there is an I²C translator between the master and slave in these examples, the I²C translator must change direction when both A and B ports are LOW. The Npassgates can accomplish this task very efficiently because, when both A and B ports are LOW, the Npassgates act as a low-resistive short between the A and B ports.

Due to I²C's open-drain topology, I²C masters and slaves are not push/pull drivers. Logic LOWs are "pulled down" (I_{sink}), while logic HIGHs are "let go" (3-state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where $R = R_{PU}$ and $C =$ the bus capacitance. If the FXMAR2102 is attached to the master [on the A port] and there is a slave on the B port, the Npassgates act as a low-resistive short between both ports until either of the port's $V_{CC}/2$ thresholds are reached. After the RC time constant has reached the $V_{CC}/2$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW-to-HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot in Figure 5. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high-impedance path exists between the A and B ports because both the Npassgates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port $V_{CC}/2$ threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH-to-LOW (HL) direction, accelerating the falling edge.

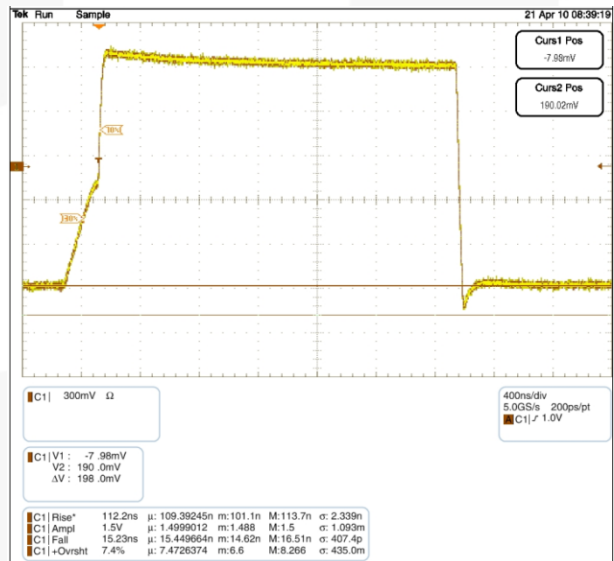


Figure 5. Waveform C: 600 pF, Total R_{PU} : 2.2 K Ω

V_{OL} vs. I_{OL}

The I²C specification mandates a maximum V_{IL} (I_{OL} of 3 mA) of V_{CC} • 0.3 and a maximum V_{OL} of 0.4 V. If there is a master on the A port of an I²C translator with a V_{CC} of 1.65 V and a slave on the I²C translator B port with a V_{CC} of 3.3 V, the maximum V_{IL} of the master is (1.65 V x 0.3) 495 mV. The slave could legally transmit a valid logic LOW of 0.4 V to the master.

If the I²C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to the master greater than 495 mV. To complicate matters, the I²C specification states that 6 mA of I_{OL} is recommended for bus capacitances approaching 400 pF. More I_{OL} increases the voltage drop across the I²C translator. The I²C application benefits when I²C translators exhibit low V_{OL} performance. Figure 6 depicts typical FXMAR2102 V_{OL} performance vs. the competition, given a 0.4 V V_{IL}.

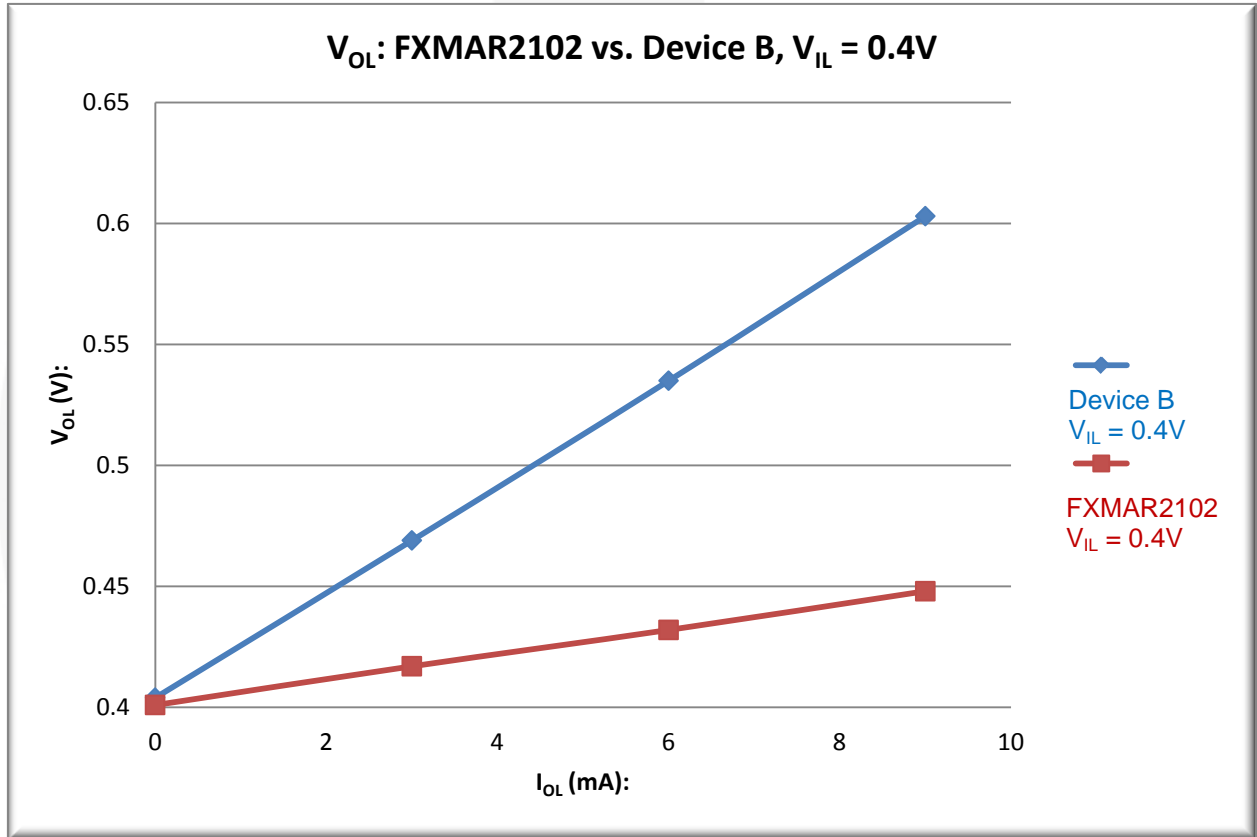


Figure 6. Device Comparison

I²C Bus Isolation

The FXMAR2102 supports I²C-Bus[®] isolation for the following conditions:

- Bus isolation if bus clear
- Bus isolation if either V_{CC} goes to ground

Bus Clear

Because the I²C specification defines the minimum SCL frequency of DC, the SCL signal can be held LOW forever; however. This condition shuts down the I²C bus. The I²C specification refers to this condition as “Bus Clear.” In Figure 7; if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the FXMAR2102 passes the SCL stuck-LOW condition from slave #2 to slave #1 and as the master.

However, if the OE pin is pulled LOW (disabled), both ports (A and B) are 3-stated. This results in the FXMAR2102 isolating slave #2 from the master and slave #1, allowing full communication between the master and slave #1.

V_{CC} to GND

If slave #2 is a camera that is suddenly removed from the I²C bus, resulting in V_{CCB} transitioning from a valid V_{CC} (1.65 V – 5.5 V) to 0 V; the FXMAR2102 automatically forces SCL and SDA on both its A and B ports into 3-state. Once V_{CCB} has reached 0 V, full I²C communication between the master and slave #1 remains undisturbed.

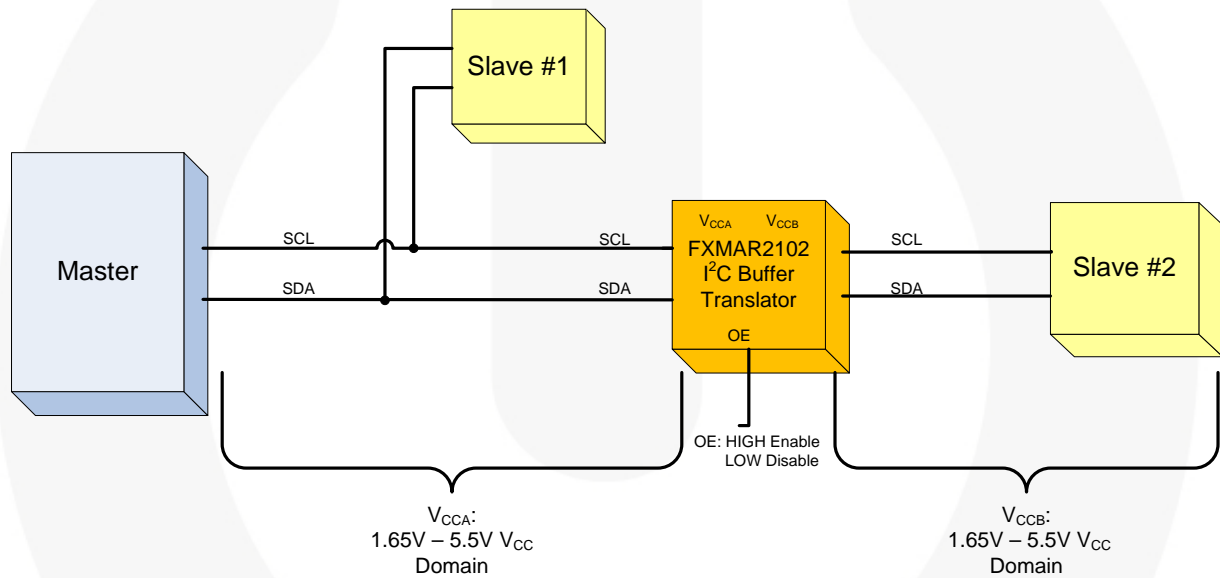


Figure 7. Bus Isolation

DC Electrical Characteristics

T_A = -40°C to +85°C.

| Symbol | Parameter | Conditions | V _{CCA} (V) | V _{CCB} (V) | Min. | Typ. | Max. | Units |
|--------------------|---|---|----------------------|----------------------|------------------------|------|------------------------|-------|
| V _{IHA} | High Level Input Voltage A | Data Inputs A _n | 1.65–5.50 | 1.65–5.50 | V _{CCA} – 0.4 | | | V |
| | | Control Input OE | 1.65–5.50 | 1.65–5.50 | 0.7 × V _{CCA} | | | |
| V _{IHB} | High Level Input Voltage B | Data Inputs B _n | 1.65–5.50 | 1.65–5.50 | V _{CCB} – 0.4 | | | V |
| V _{ILA} | Low Level Input Voltage A | Data Inputs A _n | 1.65–5.50 | 1.65–5.50 | | | 0.4 | V |
| | | Control Input OE | 1.65–5.50 | 1.65–5.50 | | | 0.3 × V _{CCA} | |
| V _{ILB} | Low Level Input Voltage B | Data Inputs B _n | 1.65–5.50 | 1.65–5.50 | | | 0.4 | V |
| V _{OL} | Low Level Output Voltage | V _{IL} = 0.15 V | 1.65–5.50 | 1.65–5.50 | | | 0.4 | V |
| | | I _{OL} = 6 mA | | | | | | |
| I _L | Input Leakage Current | Control Input OE, V _{IN} = V _{CCA} or GND | 1.65–5.50 | 1.65–5.50 | | | ±1.0 | μA |
| I _{OFF} | Power-Off Leakage Current | A _n V _{IN} or V _O = 0 V to 5.5 V | 0 | 5.50 | | | ±2.0 | μA |
| | | B _n V _{IN} or V _O = 0 V to 5.5 V | 5.50 | 0 | | | ±2.0 | |
| I _{OZ} | 3-State Output Leakage ⁽⁷⁾ | A _n , B _n V _O = 0 V to 5.5 V, OE = V _{IL} | 5.50 | 5.50 | | | ±2.0 | μA |
| | | A _n V _O = 0 V to 5.5 V, OE = Don't Care | 5.50 | 0 | | | ±2.0 | |
| | | B _n V _O = 0 V to 5.5 V, OE = Don't Care | 0 | 5.50 | | | ±2.0 | |
| I _{CCA/B} | Quiescent Supply Current ^(8,9) | V _{IN} = V _{CCi} or Floating, I _O = 0 | 1.65–5.50 | 1.65–5.50 | | | 5.0 | μA |
| I _{CCZ} | Quiescent Supply Current ⁽⁸⁾ | V _{IN} = V _{CCi} or GND, I _O = 0, OE = V _{IL} | 1.65–5.50 | 1.65–5.50 | | | 5.0 | μA |
| I _{CCA} | Quiescent Supply Current ⁽⁷⁾ | V _{IN} = 5.5 V or GND, I _O = 0, OE = Don't Care, B _n to A _n | 0 | 1.65–5.50 | | | -2.0 | μA |
| | | | 1.65–5.50 | 0 | | | 2.0 | |
| I _{CCB} | Quiescent Supply Current ⁽⁷⁾ | V _{IN} = 5.5 V or GND, I _O = 0, OE = Don't Care, A _n to B _n | 1.65–5.50 | 0 | | | -2.0 | μA |
| | | | 0 | 1.65–5.50 | | | 2.0 | |
| R _{PU} | Resistor Pull-up Value | VCCA & VCCB Sides | 1.65–5.50 | 1.65–5.50 | | 10 | | Ω |

Notes:

- This table contains the output voltage for static conditions. Dynamic drive specifications are given in Dynamic Output Electrical Characteristics.
- "Don't Care" indicates any valid logic level.
- V_{CCi} is the V_{CC} associated with the input side.
- Reflects current per supply, V_{CCA} or V_{CCB}.

Dynamic Output Electrical Characteristics

Output Rise / Fall Time⁽¹⁰⁾

Output load: $C_L = 50$ pF, $R_{PU} = NC$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | $V_{CCO}^{(11)}$ | | | | Unit |
|------------|--|------------------|--------------|--------------|----------------|------|
| | | 4.5 to 5.5 V | 3.0 to 3.6 V | 2.3 to 2.7 V | 1.65 to 1.95 V | |
| | | Typ. | Typ. | Typ. | Typ. | |
| t_{rise} | Output Rise Time; A Port, B Port ⁽¹²⁾ | 3 | 4 | 5 | 7 | ns |
| t_{fall} | Output Fall Time; A Port, B Port ⁽¹³⁾ | 1 | 1 | 1 | 1 | ns |

Notes:

- 10. Output rise and fall times guaranteed by design simulation and characterization; not production tested.
- 11. V_{CCO} is the V_{CC} associated with the output side.
- 12. See Figure 12.
- 13. See Figure 13.

Maximum Data Rate⁽¹⁴⁾

Output load: $C_L = 50$ pF, $R_{PU} = NC$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| V_{CCA} | Direction | V_{CCB} | | | | Unit |
|------------------|-----------|--------------|--------------|--------------|----------------|------|
| | | 4.5 to 5.5 V | 3.0 to 3.6 V | 2.3 to 2.7 V | 1.65 to 1.95 V | |
| | | Minimums | | | | |
| 4.5 V to 5.5 V | A to B | 50 | 50 | 40 | 30 | MHz |
| | B to A | 50 | 50 | 40 | 40 | |
| 3.0 V to 3.6 V | A to B | 50 | 50 | 40 | 19 | MHz |
| | B to A | 50 | 50 | 40 | 40 | |
| 2.3 V to 2.7 V | A to B | 40 | 40 | 30 | 19 | MHz |
| | B to A | 40 | 40 | 30 | 30 | |
| 1.65 V to 1.95 V | A to B | 40 | 40 | 30 | 19 | MHz |
| | B to A | 30 | 30 | 19 | 19 | |

Note:

- 14. F-toggle guaranteed by design simulation; not production tested.

AC Characteristics⁽¹⁵⁾

 Output Load: $C_L = 50$ pF, $R_{PU} = NC$, push / pull driver, and $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

| Symbol | Parameter | V_{CCB} | | | | | | | | Unit |
|---|--------------------------------|--------------|------|--------------|------|--------------|------|----------------|------|------|
| | | 4.5 to 5.5 V | | 3.0 to 3.6 V | | 2.3 to 2.7 V | | 1.65 to 1.95 V | | |
| | | Typ. | Max. | Typ. | Max. | Typ. | Max. | Typ. | Max. | |
| $V_{CCA} = 4.5$ to 5.5 V | | | | | | | | | | |
| t_{PLH} | A to B | 1 | 3 | 1 | 3 | 1 | 3 | 1 | 3 | ns |
| | B to A | 1 | 3 | 2 | 4 | 3 | 5 | 4 | 7 | |
| t_{PHL} | A to B | 2 | 4 | 3 | 5 | 4 | 6 | 5 | 7 | ns |
| | B to A | 2 | 4 | 2 | 5 | 2 | 6 | 5 | 7 | |
| t_{PZL} | OE to A | 4 | 5 | 6 | 10 | 5 | 9 | 7 | 15 | ns |
| | OE to B | 3 | 5 | 4 | 7 | 5 | 8 | 10 | 15 | |
| t_{PLZ} | OE to A | 65 | 100 | 65 | 105 | 65 | 105 | 65 | 105 | ns |
| | OE to B | 5 | 9 | 6 | 10 | 7 | 12 | 9 | 16 | |
| t_{skew} | A Port, B Port ⁽¹⁶⁾ | 0.50 | 1.50 | 0.50 | 1.00 | 0.50 | 1.00 | 0.50 | 1.00 | ns |
| $V_{CCA} = 3.0$ to 3.6 V | | | | | | | | | | |
| t_{PLH} | A to B | 2.0 | 5.0 | 1.5 | 3.0 | 1.5 | 3.0 | 1.5 | 3.0 | ns |
| | B to A | 1.5 | 3.0 | 1.5 | 4.0 | 2.0 | 6.0 | 3.0 | 9.0 | |
| t_{PHL} | A to B | 2.0 | 4.0 | 2.0 | 4.0 | 2.0 | 5.0 | 3.0 | 5.0 | ns |
| | B to A | 2.0 | 4.0 | 2.0 | 4.0 | 2.0 | 5.0 | 3.0 | 5.0 | |
| t_{PZL} | OE to A | 4.0 | 8.0 | 5.0 | 9.0 | 6.0 | 11.0 | 7.0 | 15.0 | ns |
| | OE to B | 4.0 | 8.0 | 6.0 | 9.0 | 8.0 | 11.0 | 10.0 | 14.0 | |
| t_{PLZ} | OE to A | 100 | 115 | 100 | 115 | 100 | 115 | 100 | 115 | ns |
| | OE to B | 5 | 10 | 4 | 8 | 5 | 10 | 9 | 15 | |
| t_{skew} | A Port, B Port ⁽¹⁶⁾ | 0.5 | 1.5 | 0.5 | 1.0 | 0.5 | 1.0 | 0.5 | 1.0 | ns |
| $V_{CCA} = 2.3$ to 2.7 V | | | | | | | | | | |
| t_{PLH} | A to B | 2.5 | 5.0 | 2.5 | 5.0 | 2.0 | 4.0 | 1.0 | 3.0 | ns |
| | B to A | 1.5 | 3.0 | 2.0 | 4.0 | 3.0 | 6.0 | 5.0 | 10.0 | |
| t_{PHL} | A to B | 2.0 | 5.0 | 2.0 | 5.0 | 2.0 | 5.0 | 3.0 | 6.0 | ns |
| | B to A | 2.0 | 5.0 | 2.0 | 5.0 | 2.0 | 5.0 | 3.0 | 6.0 | |
| t_{PZL} | OE to A | 5.0 | 10.0 | 5.0 | 10.0 | 6.0 | 12.0 | 9.0 | 18.0 | ns |
| | OE to B | 4.0 | 8.0 | 4.5 | 9.0 | 5.0 | 10.0 | 9.0 | 18.0 | |
| t_{PLZ} | OE to A | 100 | 115 | 100 | 115 | 100 | 115 | 100 | 115 | ns |
| | OE to B | 65 | 110 | 65 | 110 | 65 | 115 | 12 | 25 | |
| t_{skew} | A Port, B Port ⁽¹⁶⁾ | 0.5 | 1.5 | 0.5 | 1.0 | 0.5 | 1.0 | 0.5 | 1.0 | ns |
| $V_{CCA} = 1.65$ to 1.95 V | | | | | | | | | | |
| t_{PLH} | A to B | 4 | 7 | 4 | 7 | 5 | 8 | 5 | 10 | ns |
| | B to A | 1.0 | 2.0 | 1.0 | 2.0 | 1.5 | 3.0 | 5.0 | 10.0 | |
| t_{PHL} | A to B | 5 | 8 | 3 | 7 | 3 | 7 | 3 | 7 | ns |
| | B to A | 4 | 8 | 3 | 7 | 3 | 7 | 3 | 7 | |
| t_{PZL} | OE to A | 11 | 15 | 11 | 14 | 14 | 28 | 14 | 23 | ns |
| | OE to B | 6 | 14 | 6 | 14 | 6 | 14 | 9 | 16 | |
| t_{PLZ} | OE to A | 75 | 115 | 75 | 115 | 75 | 115 | 75 | 115 | ns |
| | OE to B | 75 | 115 | 75 | 115 | 75 | 115 | 75 | 115 | |
| t_{skew} | A Port, B Port ⁽¹⁶⁾ | 0.5 | 1.5 | 0.5 | 1.0 | 0.5 | 1.0 | 0.5 | 1.0 | ns |

Notes:

15. AC characteristics are guaranteed by design and characterization.
16. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW-to-HIGH or HIGH-to-LOW) (see Figure 15). Skew is guaranteed; not production tested.

Capacitance

T_A = +25°C.

| Symbol | Parameter | Conditions | Typical | Units |
|------------------|---|---|---------|-------|
| C _{IN} | Input Capacitance Control Pin (OE) | V _{CCA} = V _{CCB} = GND | 2.2 | pF |
| C _{I/O} | Input/Output Capacitance, A _n , B _n | V _{CCA} = V _{CCB} = 5.0 V, OE = GND | 13 | pF |

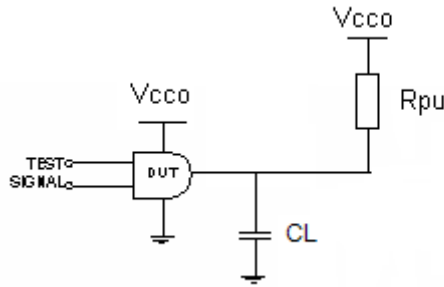


Figure 8. AC Test Circuit

Table 1. Propagation Delay Table⁽¹⁷⁾

| Test | Input Signal | Output Enable Control |
|---|--------------|-----------------------|
| t _{PLH} , t _{PHL} | Data Pulses | V _{CCA} |
| t _{PZL} (OE to A _n , B _n) | 0 V | LOW to HIGH Switch |
| t _{PLZ} (OE to A _n , B _n) | 0 V | HIGH to LOW Switch |

Note:

17. For t_{PZL} and t_{PLZ} testing, an external 2.2 KΩ pull-up resistor to V_{CCO} is required in order to force the I/O pins high while OE is Low because when OE is low, the internal 10KΩ RPU's are decoupled from their respective VCC's.

Table 2. AC Load Table

| V _{CCO} | C _L | R _L |
|------------------|----------------|----------------|
| 1.8 ±0.15 V | 50 pF | NC |
| 2.5 ±0.2 V | 50 pF | NC |
| 3.3 ±0.3 V | 50 pF | NC |
| 5.0 ±0.5 V | 50 pF | NC |

Timing Diagrams

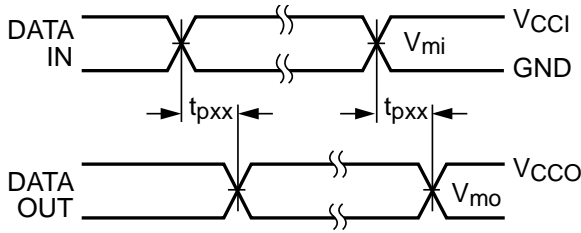


Figure 9. Waveform for Inverting and Non-Inverting Functions⁽¹⁸⁾

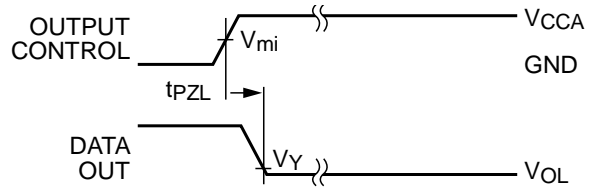


Figure 10.3-STATE Output Low Enable Time⁽¹⁸⁾

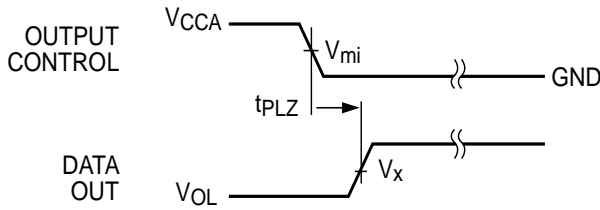


Figure 11.3-STATE Output High Enable Time⁽¹⁸⁾

| Symbol | V _{CC} |
|---------------------------------|------------------------|
| V _{mi} ⁽¹⁹⁾ | V _{CC1} / 2 |
| V _{mo} | V _{CC0} / 2 |
| V _x | 0.5 x V _{CC0} |
| V _y | 0.1 x V _{CC0} |

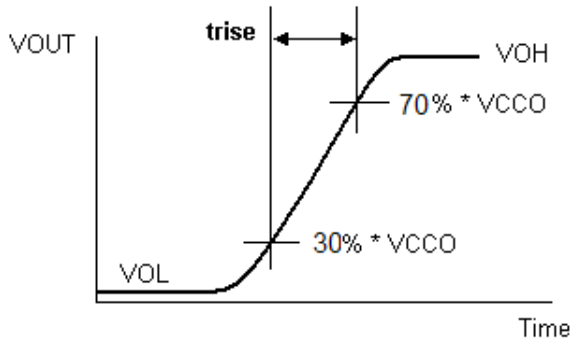


Figure 12.Active Output Rise Time

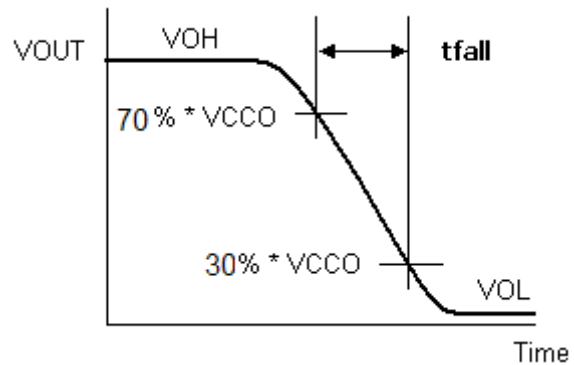


Figure 13.Active Output Fall Time

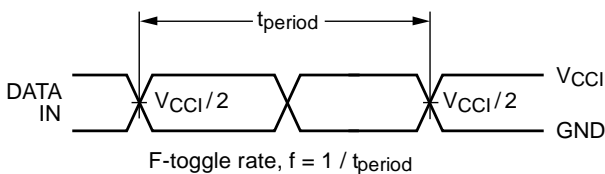
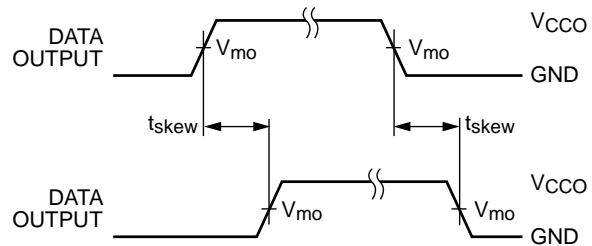


Figure 14.F-Toggle Rate



$$t_{skew} = (t_{pHLmax} - t_{pHLmin}) \text{ or } (t_{pLHmax} - t_{pLHmin})$$

Figure 15.Output Skew Time

Notes:

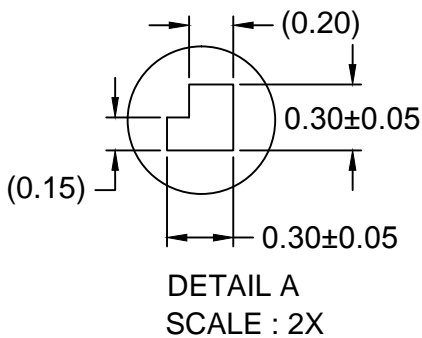
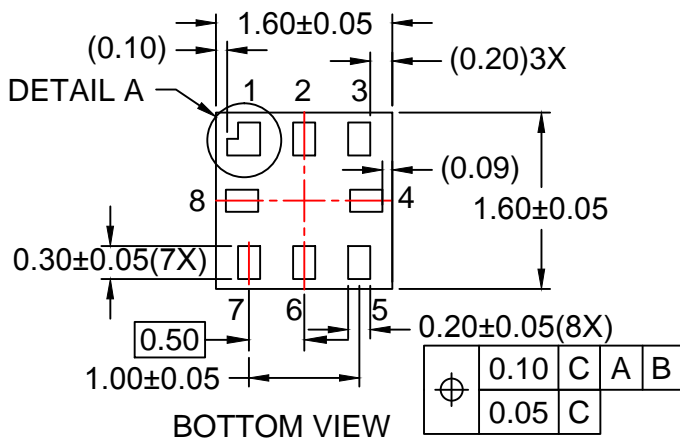
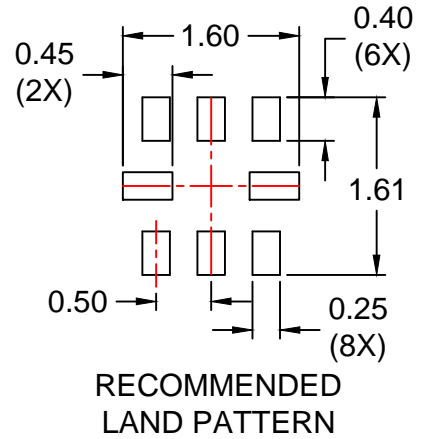
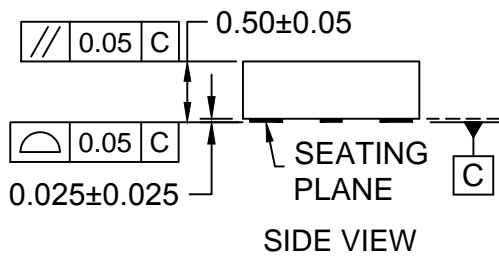
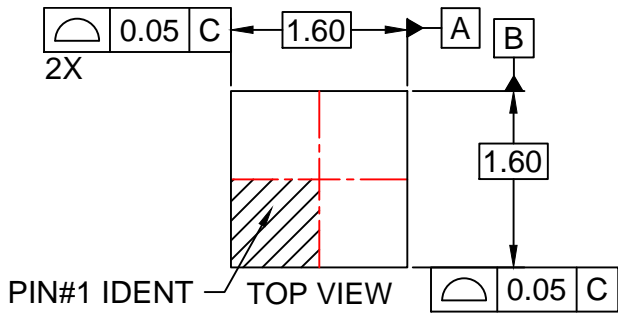
- 18. Input $t_R = t_F = 2.0$ ns, 10% to 90% at $V_{IN} = 1.65$ V to 1.95 V;
 Input $t_R = t_F = 2.0$ ns, 10% to 90% at $V_{IN} = 2.3$ to 2.7 V;
 Input $t_R = t_F = 2.5$ ns, 10% to 90%, at $V_{IN} = 3.0$ V to 3.6 V only;
 Input $t_R = t_F = 2.5$ ns, 10% to 90%, at $V_{IN} = 4.5$ V to 5.5 only.
- 19. $V_{CC1} = V_{CCA}$ for control pin OE or $V_{mi} = (V_{CCA} / 2)$.

Product-Specific Dimensions

| Symbol from JEDEC MO-220 | Description | NOM Value |
|--------------------------|-----------------|-----------|
| A | Overall Height | 0.55 |
| A1 | PKG Standoff | 0.012 |
| A3 | Lead Thickness | 0.15 |
| b | Lead Width | 0.2 |
| D | Body Length (X) | 1.4 |
| E | Body Width (Y) | 1.2 |
| L | Lead Length | 0.3 |
| e | Lead Pitch | 0.4 |

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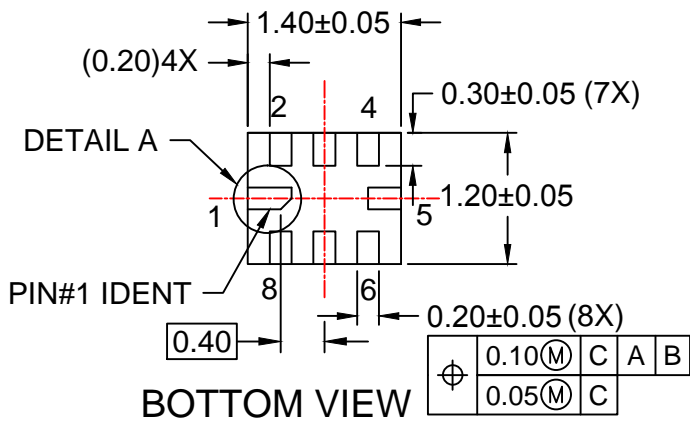
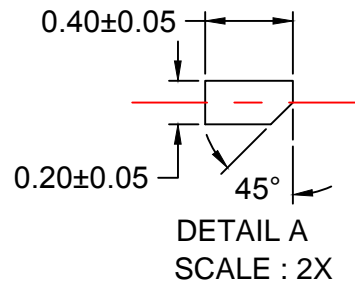
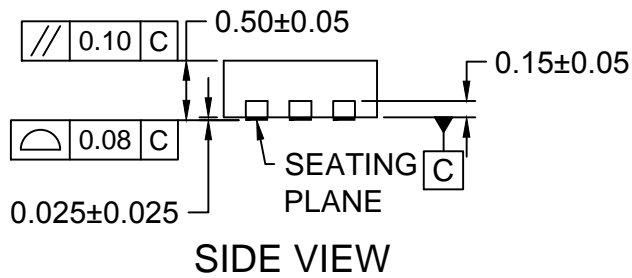
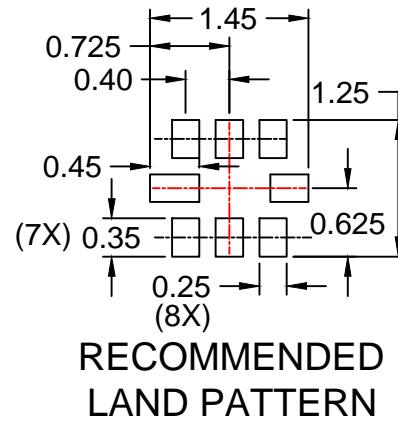
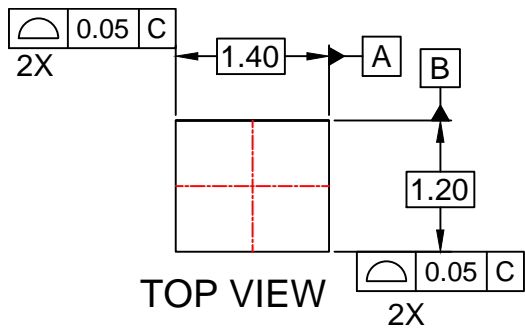
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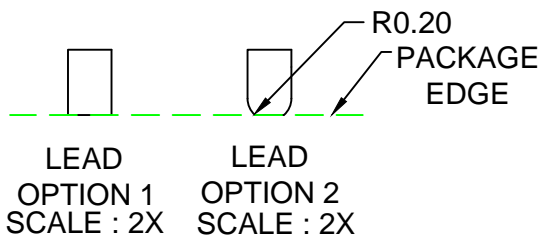




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