

74F377 Octal D Flip-Flop with Clock Enable

General Description

The 'F377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

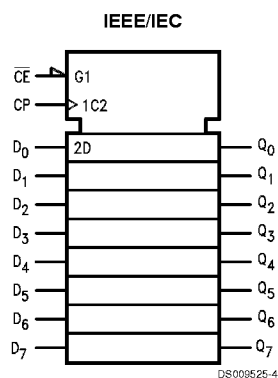
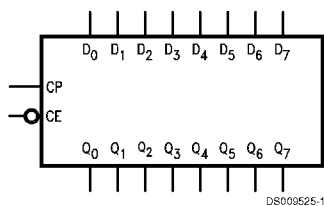
- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- See 'F273 for master reset version
- See 'F373 for transparent latch version
- See 'F374 for 3-STATE version
- Guaranteed 4000V minimum ESD protection

Ordering Code:

Commercial	Military	Package Number	Package Description
74F377PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F377DM (QB)	J20A	20-Lead Ceramic Dual-In-Line
74F377SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F377SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F377FM (QB)	W20A	20-Lead Cerpack
	54F377LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

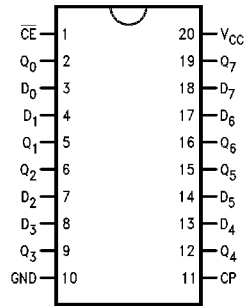
Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols

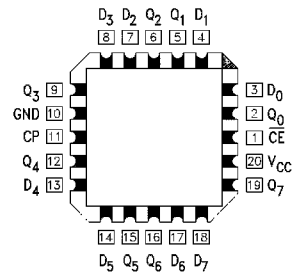


Connection Diagrams

Pin Assignment for
DIP, SOIC and Flatpak



Pin Assignment
for LCC



Unit Loading/Fan Out

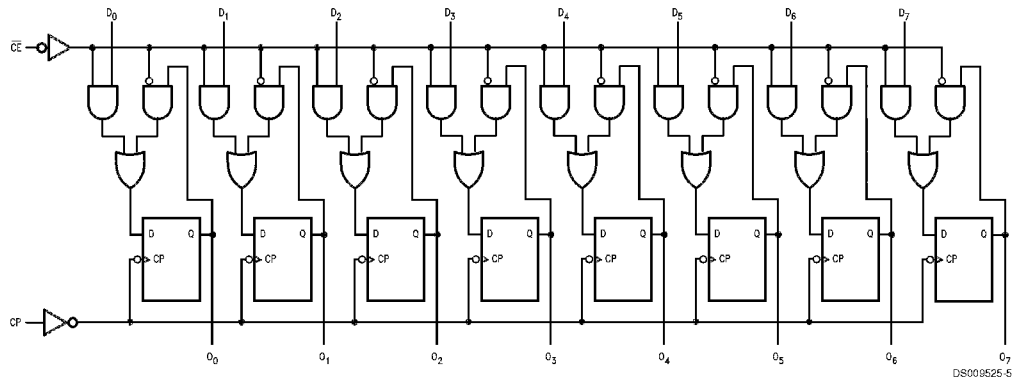
Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0 – D_7	Data Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{CE}	Clock Enable (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
CP	Clock Pulse Input	1.0/1.0	20 μ A/–0.6 mA
Q_0 – Q_7	Data Outputs	50/33.3	–1 mA/20 mA

Mode Select-Function Table

Operating Mode	Inputs			Output
	CP	\overline{CE}	D_n	Q_n
Load "1"	↗	l	h	H
Load "0"	↗	l	l	L
Hold	↗	h	X	No Change
(Do Nothing)	X	H	X	No Change

H = HIGH Voltage Level
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
L = LOW Voltage Level
l = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

ESD Last Passing Voltage (Min)

4000V

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		74F 10% V _{CC}	2.5				I _{OH} = -1 mA
		74F 5% V _{CC}	2.7				I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
		74F 10% V _{CC}		0.5			I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{CCCH}	Power Supply Current		35	46	mA	Max	CP = $\overline{\text{CP}}$ D _n = $\overline{\text{MR}}$ = HIGH
I _{CCL}			44	56			

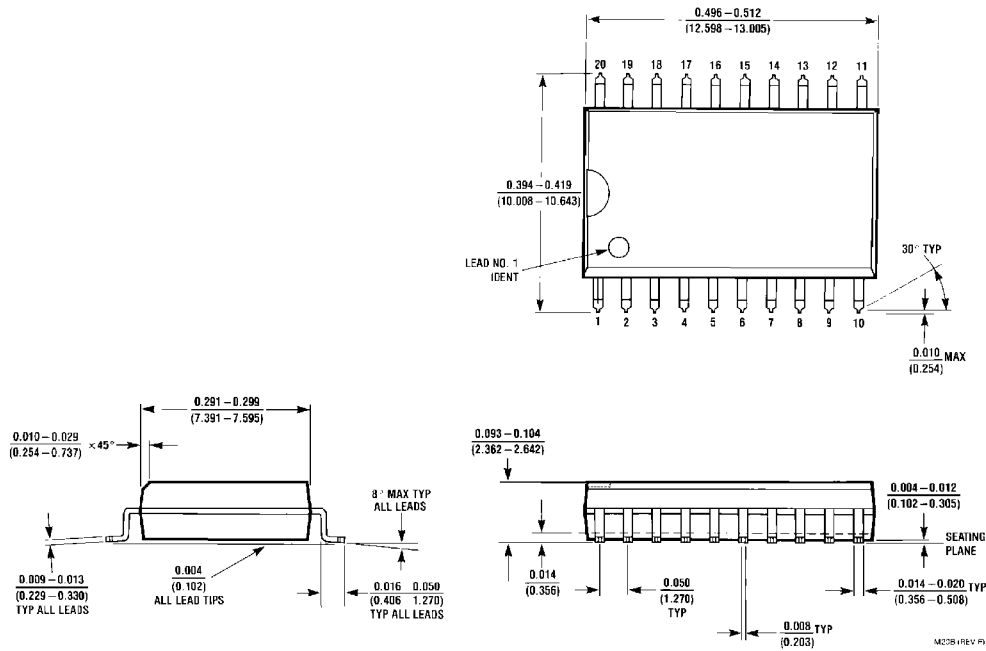
AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{MII}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{Max}	Maximum Clock Frequency	130			85		105		MHz
t_{PLH}	Propagation Delay	3.0			2.0	8.5	2.5	7.5	ns
t_{PHL}	CP to Q_n	4.0			3.0	10.5	3.5	9.0	

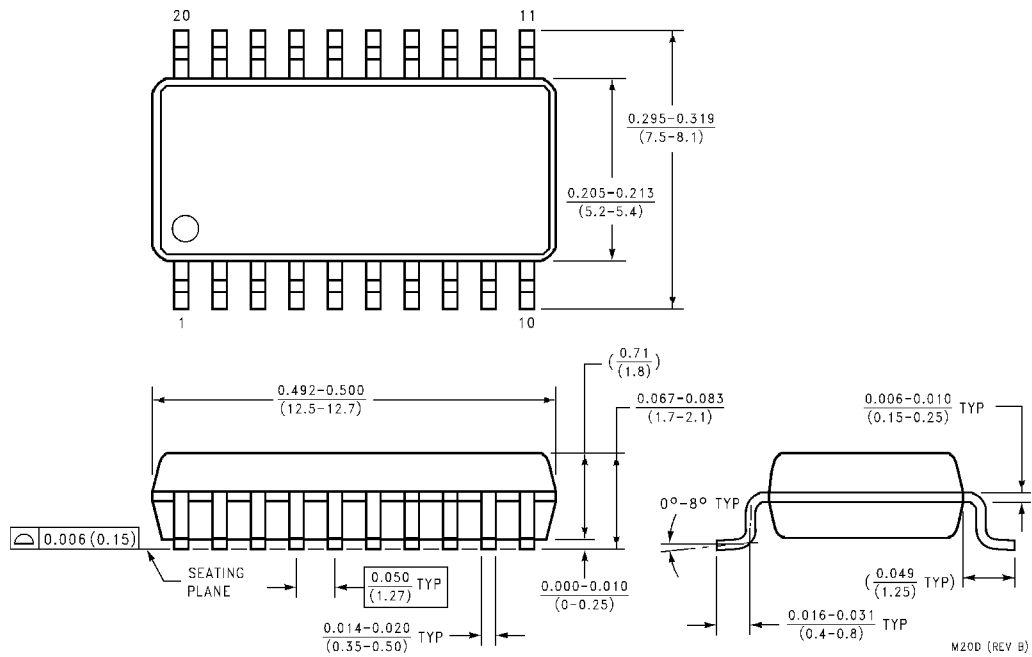
AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{MII}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW	3.0		3.5		3.0		ns
$t_s(\text{L})$	D_n to CP	3.5		4.0		3.5		
$t_h(\text{H})$	Hold Time, HIGH or LOW	0.5		1.0		0.5		ns
$t_h(\text{L})$	D_n to CP	1.0		1.0		1.0		
$t_s(\text{H})$	Setup Time, HIGH or LOW	4.1		4.0		4.1		ns
$t_s(\text{L})$	$\overline{\text{CE}}$ to CP	3.5		5.0		4.0		
$t_h(\text{H})$	Hold Time, HIGH to LOW	0.5		1.5		0.5		ns
$t_h(\text{L})$	$\overline{\text{CE}}$ to CP	2.0		2.5		2.0		
$t_w(\text{H})$	Clock Pulse Width, HIGH or LOW	6.0		5.0		6.0		ns
$t_w(\text{L})$		6.0		5.0		6.0		

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

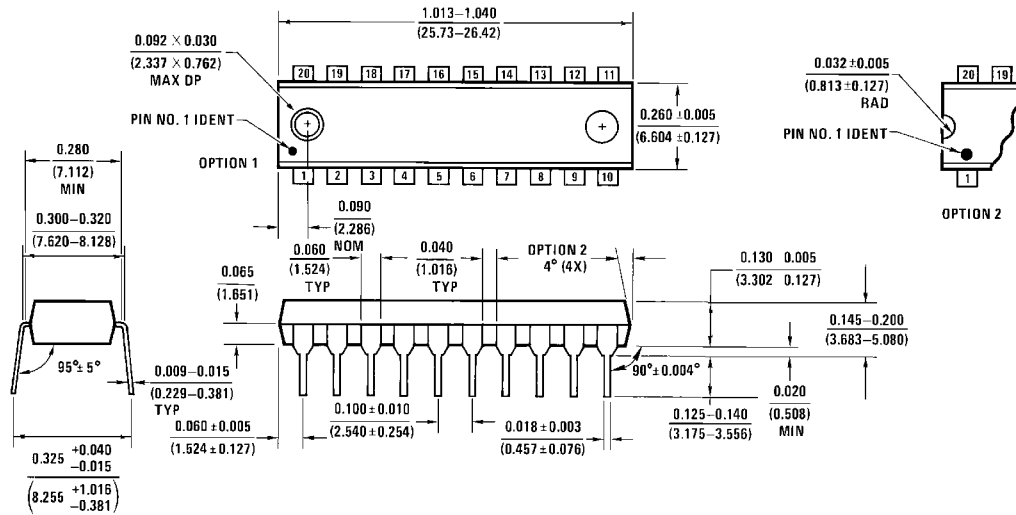


**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
Package Number M20B**



**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
Package Number M20D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
Package Number N20A**

N20A (REV G)

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

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