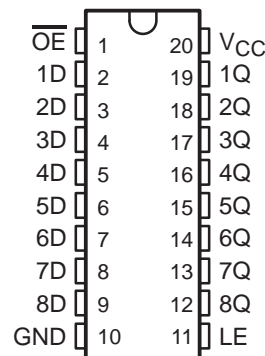


# SN74LVC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

SCAS300A – JANUARY 1993 – REVISED NOVEMBER 1994

- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**DB, DW, OR PW PACKAGE  
(TOP VIEW)**



## description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V  $V_{CC}$  operation.

The SN74LVC573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, input/output (I/O) ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels at the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without the need for interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC573 is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

**FUNCTION TABLE  
(each latch)**

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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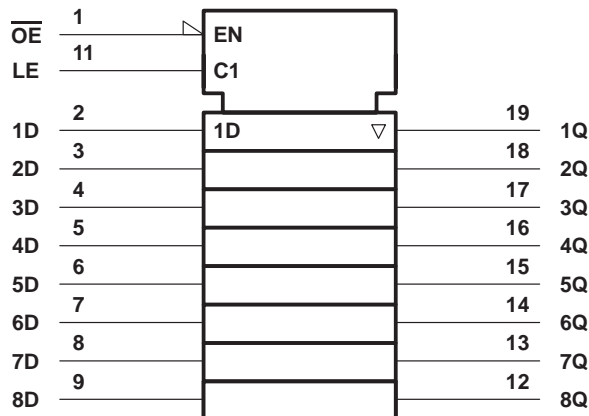
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# SN74LVC573

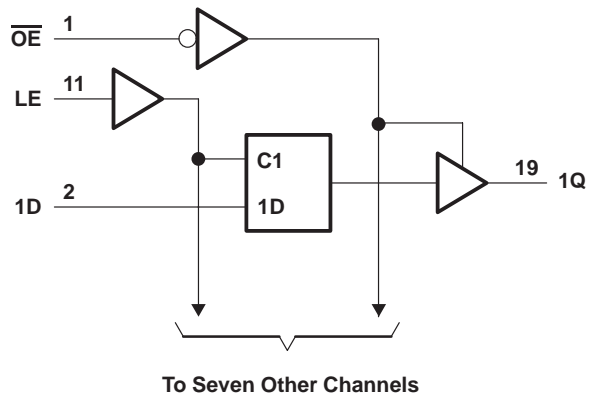
## OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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### logic symbol†



### logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 4.6 V
Input voltage range, $V_I$ .....	-0.5 V to 4.6 V
Output voltage range, $V_O$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 100$ mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2):	
DB package .....	0.6 W
DW package .....	1.6 W
PW package .....	0.7 W
Operating free-air temperature range, $T_A$ .....	$-40^\circ\text{C}$ to $85^\circ\text{C}$
Storage temperature range .....	$-65^\circ\text{C}$ to $150^\circ\text{C}$

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This value is limited to 4.6 V maximum.

2. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2.7	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$		V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2.7\text{ V}$	-12	mA
		$V_{CC} = 3\text{ V}$	-24	
$I_{OL}$	Low-level output current	$V_{CC} = 2.7\text{ V}$	12	mA
		$V_{CC} = 3\text{ V}$	24	
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_A$	Operating free-air temperature	-40	85	°C

NOTE 3: Unused or floating inputs must be held high or low.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	$V_{CC}^\dagger$	$T_A = -40^\circ\text{C to }85^\circ\text{C}$		UNIT
			MIN	MAX	
$V_{OH}$	$I_{OH} = -100\ \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$		V
	$I_{OH} = -12\ \text{mA}$	2.7 V	2.2		
		3 V	2.4		
	$I_{OH} = -24\ \text{mA}$	3 V	2		
$V_{OL}$	$I_{OL} = 100\ \mu\text{A}$	MIN to MAX	0.2		V
	$I_{OL} = 12\ \text{mA}$	2.7 V	0.4		
	$I_{OL} = 24\ \text{mA}$	3 V	0.55		
$I_I$	$V_I = V_{CC}$ or GND	3.6 V	$\pm 5$		$\mu\text{A}$
$I_{OZ}$	$V_O = V_{CC}$ or GND	3.6 V	$\pm 10$		$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V	20		$\mu\text{A}$
$\Delta I_{CC}$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , Other inputs at $V_{CC}$ or GND		500		$\mu\text{A}$
$C_i$	$V_I = V_{CC}$ or GND	3.3 V			pF
$C_o$	$V_O = V_{CC}$ or GND	3.3 V			pF

<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CC} = 2.7\text{ V}$		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, LE high	4		5		ns
$t_{su}$	Setup time, data before LE $\downarrow$	2		3		ns
$t_h$	Hold time, data after LE $\downarrow$	2		3		ns



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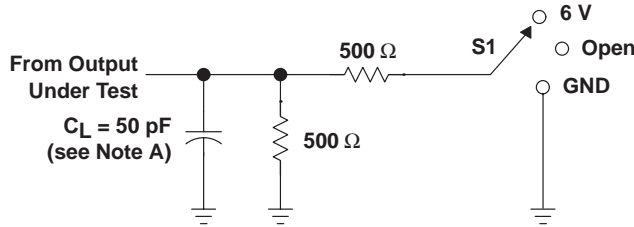
switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			$V_{CC} = 2.7 \text{ V}$		UNIT
			MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	D	Q	1.5	4.2	8	1.5	9	ns
	LE		1.5	5	9	1.5	10	
$t_{en}$	$\overline{OE}$	Q	1.5	4	8.5	1.5	9.5	ns
$t_{dis}$	$\overline{OE}$	Q	1.5	3.7	7.5	1.5	8.5	ns

operating characteristics,  $V_{CC} = 3.3 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

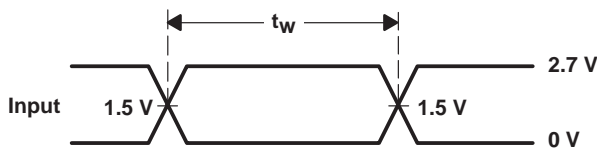
PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	Outputs enabled	20	pF
		Outputs disabled	3.5	

PARAMETER MEASUREMENT INFORMATION

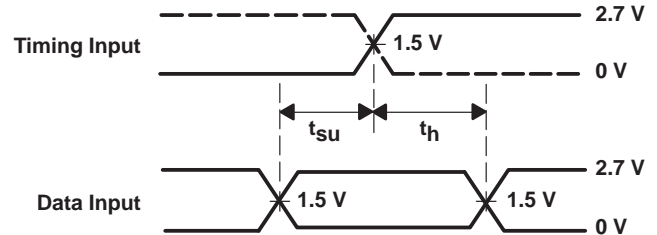


LOAD CIRCUIT FOR OUTPUTS

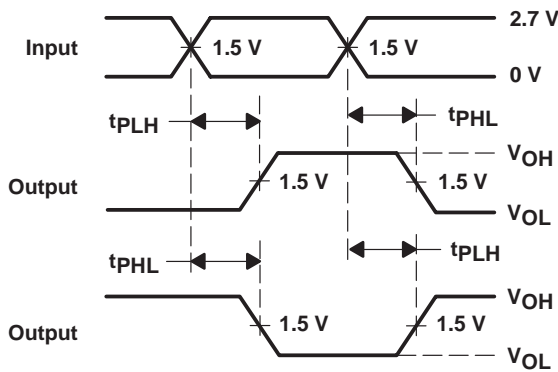
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



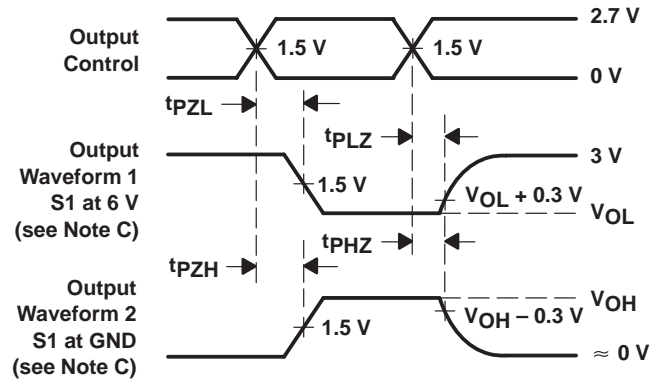
VOLTAGE WAVEFORMS  
 PULSE DURATION



VOLTAGE WAVEFORMS  
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
 PROPAGATION DELAY TIMES  
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
 ENABLE AND DISABLE TIMES  
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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