National Semiconductor

# DM54S138/DM74S138, DM54S139/DM74S139 Decoders/Demultiplexers

## General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The S138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The S139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

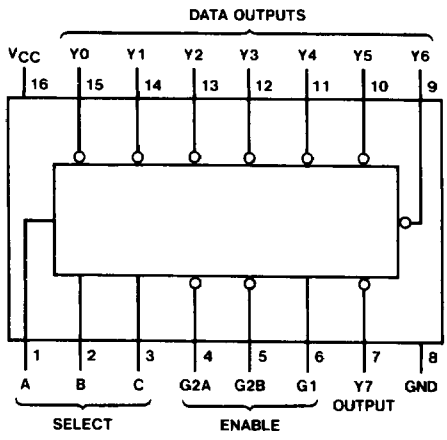
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

## Features

- Designed specifically for high speed:
  Memory decoders
  Data transmission systems
- S138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- S139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay time (3 levels of logic)
  S138 8 ns
  S139 7.5 ns
- Typical power dissipation
  S138 245 mW
  S139 300 mW

## Connection Diagrams

**Dual-In-Line Package**

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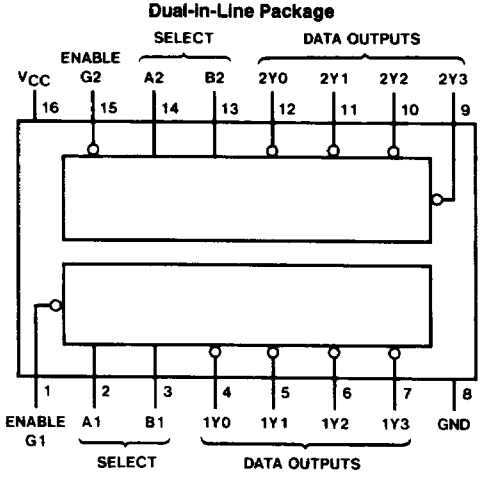
**Dual-In-Line Package**

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**Order Number DM54S138J, DM54S139J, DM54S138W, DM54139W, DM74S138N or DM74S139N**
**See NS Package Number J16A, N16E or W16A**

## Absolute Maximum Ratings (Note)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | |
| DM54S | −55° C to +125°C |
| DM74S | 0° C to +70°C |
| Storage Temperature Range | −65° C to +150° C |

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

## Recommended Operating Conditions

| Symbol | Parameter | DM54S138,S139 | | | DM74S138,S139 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Nom | Max | Min | Nom | Max | |
| $V_{CC}$ | Supply Voltage | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High Level Input Voltage | 2 | | | 2 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High Level Output Current | | | −1 | | | −1 | mA |
| $I_{OL}$ | Low Level Output Current | | | 20 | | | 20 | mA |
| $T_A$ | Free Air Operating Temperature | −55 | | 125 | 0 | | 70 | °C |

## Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

| Symbol | Parameter | Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −18 mA | | | | −1.2 | V |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max, $V_{IH}$ = Min | DM54 | 2.5 | 3.4 | | V |
| | | | DM74 | 2.7 | 3.4 | | |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IH}$ = Min, $V_{IL}$ = Max | | | | 0.5 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5V | | | | 1 | mA |
| $I_{IH}$ | High Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.7V | | | | 50 | μA |
| $I_{IL}$ | Low Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.5V | | | | −2 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 2) | DM54 | −40 | | −100 | mA |
| | | | DM74 | −40 | | −100 | |
| $I_{CC}$ | Supply Current (S138) | $V_{CC}$ = Max (Note 3) | | | 49 | 74 | mA |
| $I_{CC}$ | Supply Current (S139) | $V_{CC}$ = Max (Note 3) | | | 60 | 90 | mA |

**Note 1:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 2:** Not more than one output should be shorted at a time, and the duration should not exceed one second.

**Note 3:** $I_{CC}$ is measured with all outputs enabled and open.

## 'S138 Switching Characteristics

at $V_{CC}$ = 5V and $T_A$ = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) to (Output) | Levels of Delay | $R_L$ = 280Ω | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Select to Output | 2 | | 7 | | 9 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Select to Output | 2 | | 10.5 | | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Select to Output | 3 | | 12 | | 14 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Select to Output | 3 | | 12 | | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Enable to Output | 2 | | 8 | | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Enable to Output | 2 | | 11 | | 14 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Enable to Output | 3 | | 11 | | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Enable to Output | 3 | | 11 | | 14 | ns |

## 'S139 Switching Characteristics

at $V_{CC}$ = 5V and $T_A$ = 25°C (See Section 1 for Test Waveforms and Output Load)

| Symbol | Parameter | From (Input) to (Output) | Levels of Delay | $R_L$ = 280Ω | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | $C_L$ = 15 pF | | $C_L$ = 50 pF | | |
| | | | | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Select to Output | 2 | | 7.5 | | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Select to Output | 2 | | 10 | | 13 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Select to Output | 3 | | 12 | | 13 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Select to Output | 3 | | 12 | | 15 | ns |
| $t_{PLH}$ | Propagation Delay Time Low to High Level Output | Enable to Output | 2 | | 8 | | 10 | ns |
| $t_{PHL}$ | Propagation Delay Time High to Low Level Output | Enable to Output | 2 | | 10 | | 13 | ns |

## Function Tables

**S138**

| Inputs | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Enable | | Select | | | | | | | | | | |
| G1 | G2* | C | B | A | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | H | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | H | H | H | H | L | H | H | H | H |
| H | L | H | L | L | H | H | H | H | L | H | H | H |
| H | L | H | L | H | H | H | H | H | H | L | H | H |
| H | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | H | H | H | H | H | H | H | H | H | H | L |

* G2 = G2A + G2B

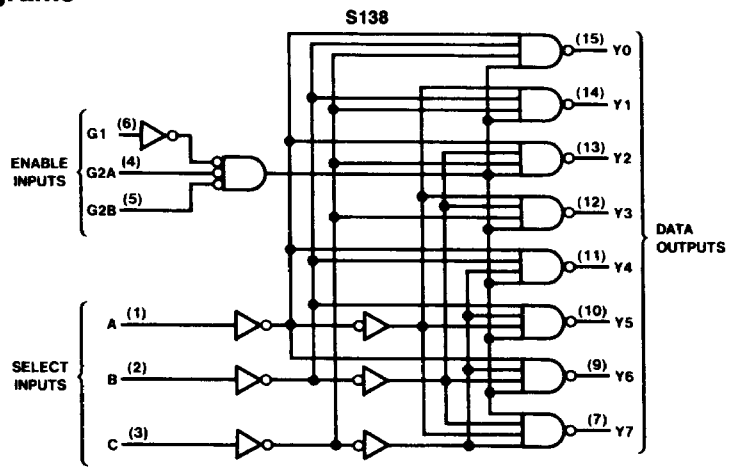
H = high level, L = low level, X = don't care (either low or high logic level)

**S139**

| Inputs | | | Outputs | | | |
|---|---|---|---|---|---|---|
| Enable | Select | | | | | |
| G | B | A | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

H = high level, L = low level, X = don't care (either low or high logic level)

## Logic Diagrams

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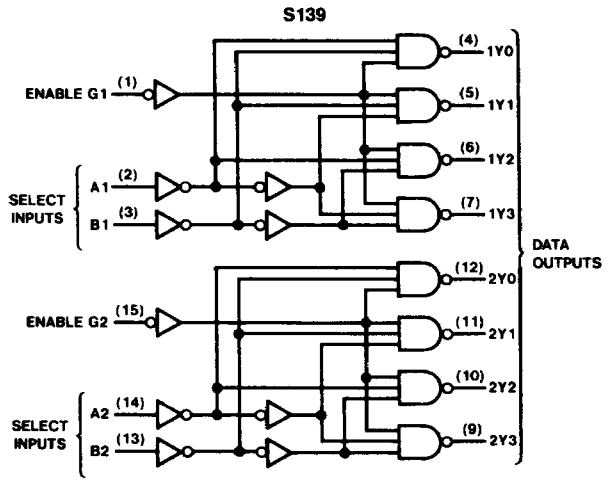


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