

# SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

SCBS232E – JANUARY 1991 – REVISED OCTOBER 1998

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required
- State-of-the-Art EPIC-IIB™ BiCMOS Design Significantly Reduces Power Dissipation
- Typical  $V_{OLP}$  (Output Ground Bounce) < 1 V at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), Plastic (N) and Ceramic (J) DIPs, and Ceramic Flat (W) Package

## description

These octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. Together with the 'ABT2241 and 'ABT2244A, these devices provide combinations of inverting and noninverting outputs, symmetrical active-low output-enable ( $\overline{OE}$ ) inputs, and complementary OE and  $\overline{OE}$  inputs. These devices feature high fan-out and improved fan-in.

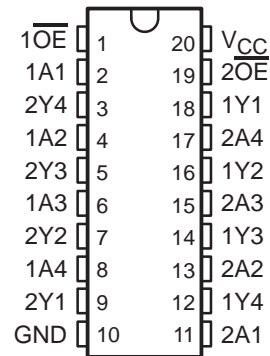
These devices are organized as two 4-bit line drivers with separate  $\overline{OE}$  inputs. When  $\overline{OE}$  is low, the devices pass inverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

The outputs, which are designed to sink up to 12 mA, include equivalent 25-Ω series resistors to reduce overshoot and undershoot.

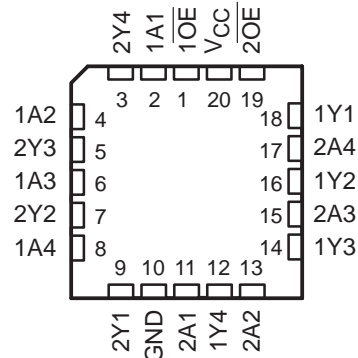
To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN54ABT2240A is characterized for operation over the full military temperature range of  $-55^\circ\text{C}$  to  $125^\circ\text{C}$ . The SN74ABT2240A is characterized for operation from  $-40^\circ\text{C}$  to  $85^\circ\text{C}$ .

SN54ABT2240A . . . J OR W PACKAGE  
SN74ABT2240A . . . DB, DW, N, OR PW PACKAGE  
(TOP VIEW)



SN54ABT2240A . . . FK PACKAGE  
(TOP VIEW)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

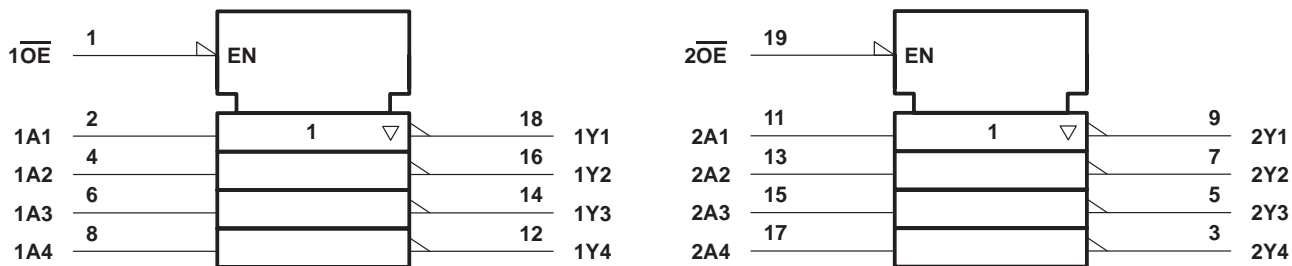
# SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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FUNCTION TABLE  
(each buffer)

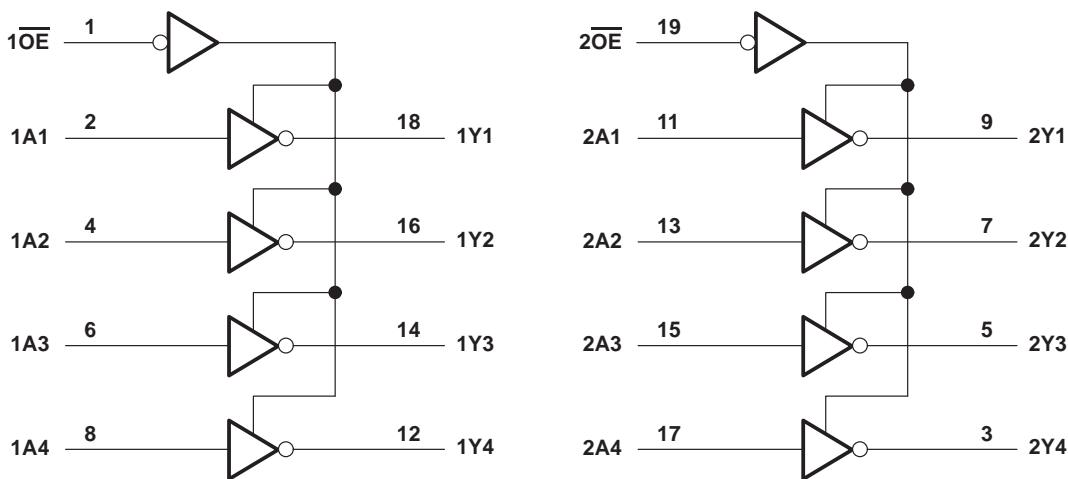
INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	L
L	L	H
H	X	Z

## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)







# SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ABT2240A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1	3	4	1	5	ns
$t_{PHL}$			2.1	4.8	5.8	2.1	6.3	
$t_{PZH}$	$\overline{OE}$	Y	1.5	3.7	4.7	1.5	6.1	ns
$t_{PZL}$			1.7	6.5	7.6	1.7	8.8	
$t_{PHZ}$	$\overline{OE}$	Y	1.8	3.8	6.4	1.5	6.8	ns
$t_{PLZ}$			1	4.7	5.8	1	6.9	

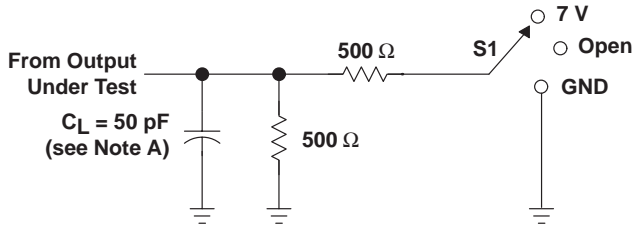
switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74ABT2240A				UNIT	
			$V_{CC} = 5$ V, $T_A = 25^\circ$ C			MIN		MAX
			MIN	TYP	MAX			
$t_{PLH}$	A	Y	1	3	4.1	1	4.8	ns
$t_{PHL}$			2.1	4.1	5.1	2.1	5.4	
$t_{PZH}$	$\overline{OE}$	Y	1.1	3.1	4.7	1.1	5.2	ns
$t_{PZL}$			1.7	4.5	6.4	1.7	6.8	
$t_{PHZ}$	$\overline{OE}$	Y	1.8	3.4	5.7	1.8	6.4	ns
$t_{PLZ}$			1.9	3.6	6	1.9	6.2	

# SN54ABT2240A, SN74ABT2240A OCTAL BUFFERS AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS

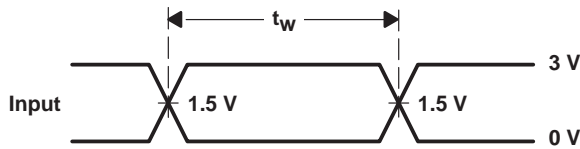
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## PARAMETER MEASUREMENT INFORMATION

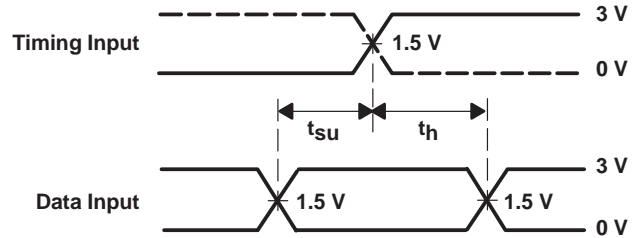


LOAD CIRCUIT

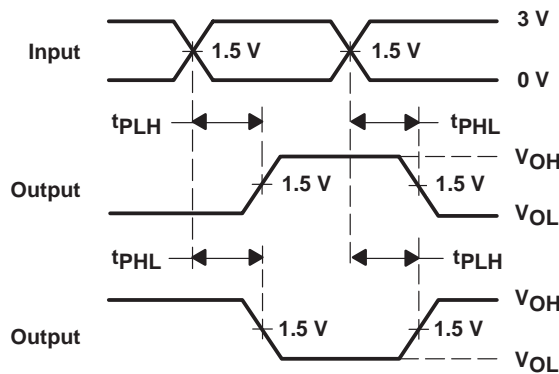
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



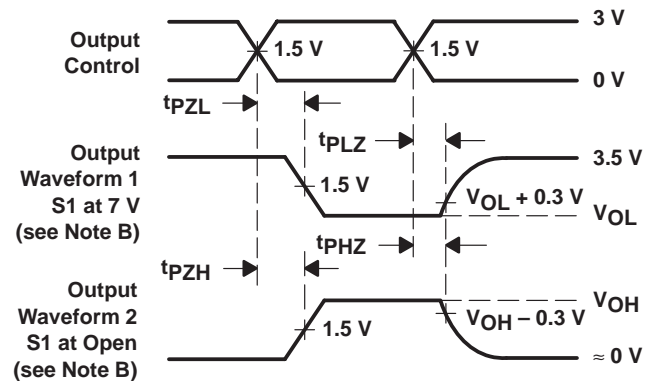
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9469701Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9469701Q2A SNJ54ABT 2240AFK	<a href="#">Samples</a>
5962-9469701QRA	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469701QR A SNJ54ABT2240AJ	<a href="#">Samples</a>
5962-9469701QSA	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469701QS A SNJ54ABT2240AW	<a href="#">Samples</a>
SN74ABT2240ADBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		
SN74ABT2240ADBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A	<a href="#">Samples</a>
SN74ABT2240ADBRE4	ACTIVE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240ADBRG4	ACTIVE	SSOP	DB	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240ADW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A	<a href="#">Samples</a>
SN74ABT2240ADWE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240ADWG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240ADWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A	<a href="#">Samples</a>
SN74ABT2240ADWRE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240ADWRG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240AN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT2240AN	<a href="#">Samples</a>
SN74ABT2240ANE4	ACTIVE	PDIP	N	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240ANSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT2240A	<a href="#">Samples</a>
SN74ABT2240ANSRE4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT2240ANSRG4	ACTIVE	SO	NS	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240APW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A	<a href="#">Samples</a>
SN74ABT2240APWE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240APWG4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240APWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		
SN74ABT2240APWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	AA240A	<a href="#">Samples</a>
SN74ABT2240APWRE4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SN74ABT2240APWRG4	ACTIVE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85		<a href="#">Samples</a>
SNJ54ABT2240AFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9469701Q2A SNJ54ABT 2240AFK	<a href="#">Samples</a>
SNJ54ABT2240AJ	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469701QR A SNJ54ABT2240AJ	<a href="#">Samples</a>
SNJ54ABT2240AW	ACTIVE	CFP	W	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9469701QS A SNJ54ABT2240AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.



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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54ABT2240A, SN74ABT2240A :**

● Catalog: [SN74ABT2240A](#)

● Military: [SN54ABT2240A](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT2240ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ABT2240ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1
SN74ABT2240ANSR	SO	NS	20	2000	330.0	24.4	8.2	13.0	2.5	12.0	24.0	Q1
SN74ABT2240APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT2240ADBR	SSOP	DB	20	2000	367.0	367.0	38.0
SN74ABT2240ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ABT2240ANSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ABT2240APWR	TSSOP	PW	20	2000	367.0	367.0	38.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AC.





PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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