

# 54F/74F374 Octal D-Type Flip-Flop with TRI-STATE® Outputs

## General Description

The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE) are common to all flip-flops.

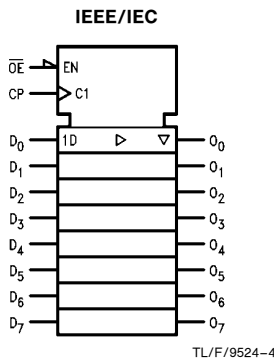
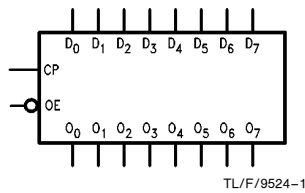
## Features

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F374PC		N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
	54F374DM (QB)	J20A	20-Lead Ceramic Dual-In-Line
74F374SC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F374SJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
74F374MSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54F374FM (QB)	W20A	20-Lead Cerpack
	54F374LM (QB)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

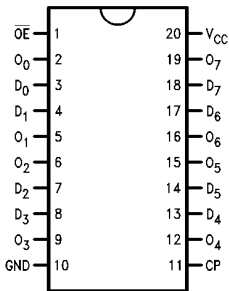
Note 1: Devices also available in 13" reel. Use suffix = SCX, SJX, and MSAX.

## Logic Symbols

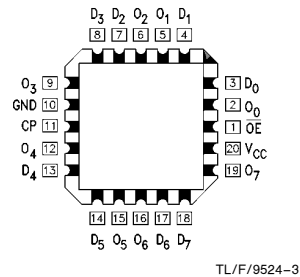


## Connection Diagrams

Pin Assignment for DIP, SOIC, SSOP and Flatpak



Pin Assignment for LCC



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## Unit Loading/Fan Out


Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
D <sub>0</sub> –D <sub>7</sub>	Data Inputs	1.0/1.0	20 $\mu$ A/ –0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/ –0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/ –0.6 mA
O <sub>0</sub> –O <sub>7</sub>	TRI-STATE Outputs	150/40 (33.3)	–3 mA/24 mA (20 mA)

## Functional Description

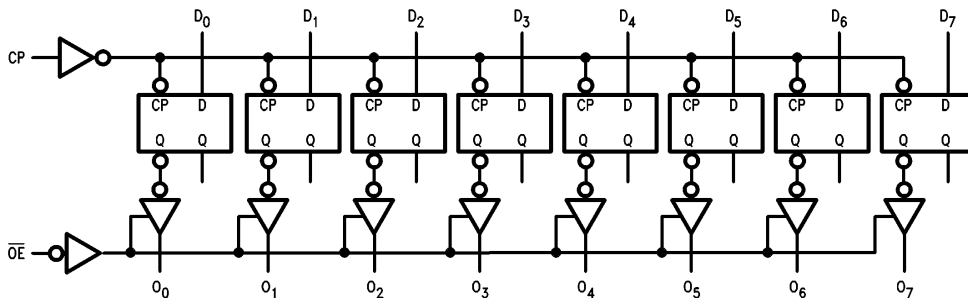
The 'F374 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs			Internal Register	Output
D <sub>n</sub>	CP	$\overline{OE}$		O <sub>n</sub>
H		L	H	H
L		L	L	L
X	X	H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 = LOW-to-HIGH Clock Transition

## Logic Diagram



TL/F/9524–5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

ESD Last Passing Voltage (Min) 4000V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

## DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54F 10% V <sub>CC</sub> 54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub> 74F 5% V <sub>CC</sub> 74F 5% V <sub>CC</sub>	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -1 mA I <sub>OH</sub> = -3 mA
V <sub>OL</sub>	Output LOW Voltage	54F 10% V <sub>CC</sub> 74F 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA I <sub>OL</sub> = 24 mA
I <sub>IH</sub>	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>CEX</sub>	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	74F	4.75		V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current	74F		3.75	μA	0.0	V <sub>ID</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V
I <sub>OZH</sub>	Output Leakage Current			50	μA	Max	V <sub>OUT</sub> = 2.7V
I <sub>OZL</sub>	Output Leakage Current			-50	μA	Max	V <sub>OUT</sub> = 0.5V
I <sub>OS</sub>	Output Short-Circuit Current			-60	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCZ</sub>	Power Supply Current		55	86	mA	Max	V <sub>O</sub> = HIGH Z

## AC Electrical Characteristics

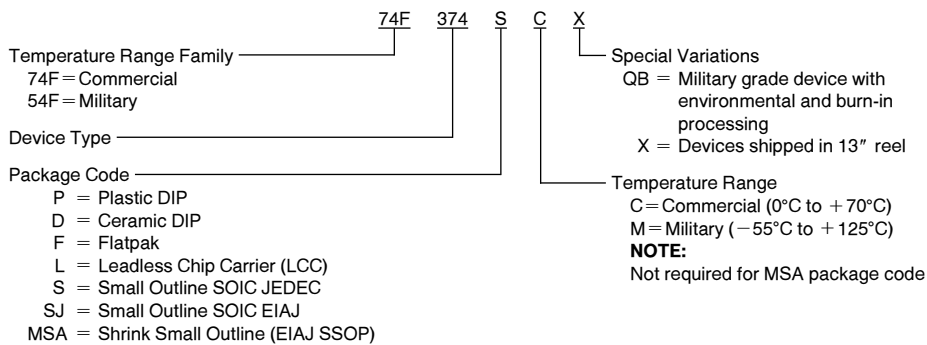
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{max}}$	Maximum Clock Frequency	100	140		60		70		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay CP to $O_n$	4.0	6.5	8.5	4.0	10.5	4.0	10.0	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output Enable Time	2.0	9.0	11.5	2.0	14.0	2.0	12.5	
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output Disable Time	2.0	5.3	7.0	2.0	8.0	2.0	8.0	ns
		1.5	4.3	5.5	1.5	7.5	1.5	6.5	

## AC Operating Requirements

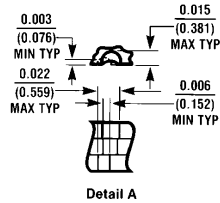
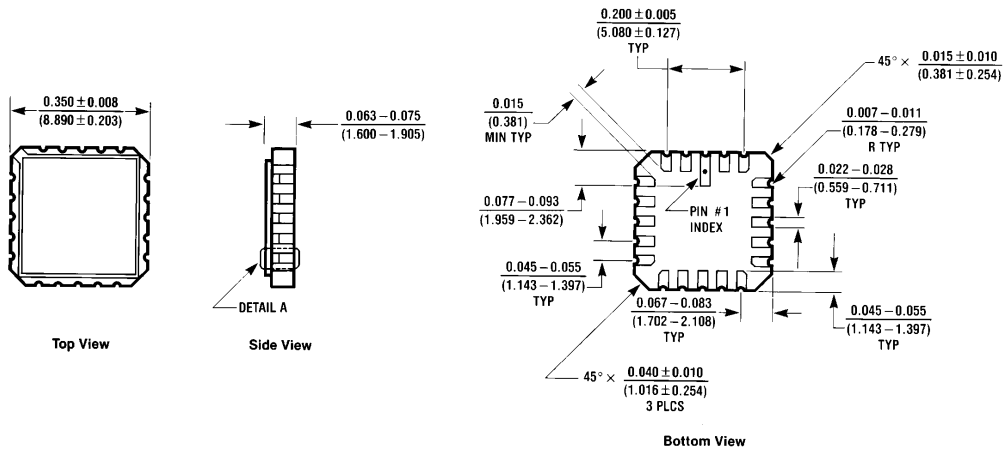
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $D_n$ to CP	2.0		2.5		2.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $D_n$ to CP	2.0		2.0		2.0		
$t_w(\text{H})$ $t_w(\text{L})$	CP Pulse Width HIGH or LOW	7.0		7.0		7.0		ns
		6.0		6.0		6.0		

## Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

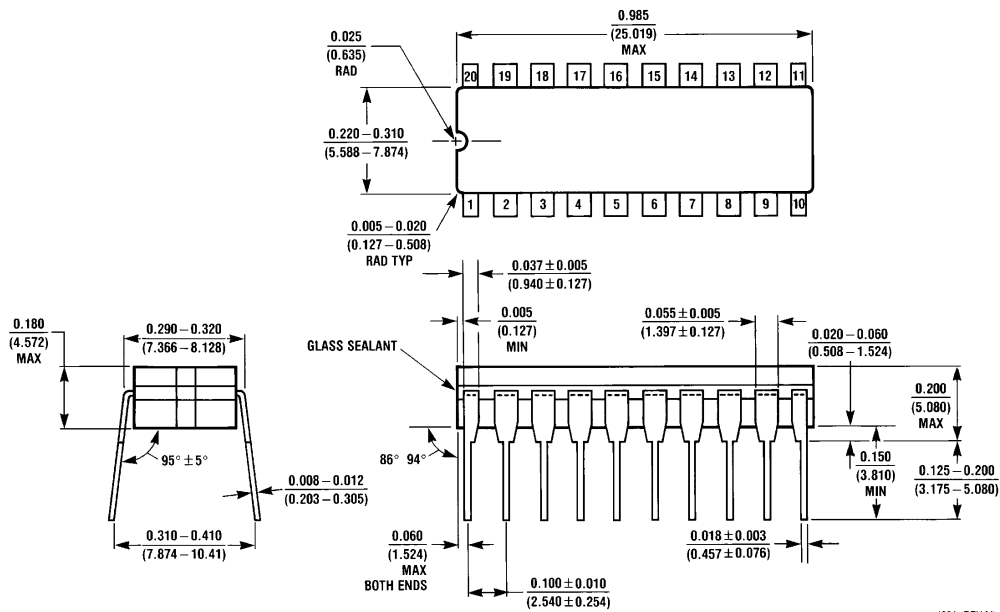


**Physical Dimensions** inches (millimeters)



**20-Lead Ceramic Leadless Chip Carrier (L)**  
 NS Package Number E20A

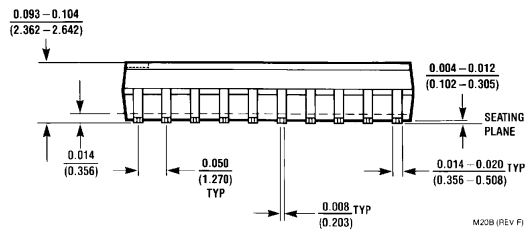
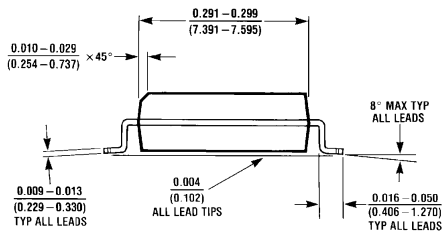
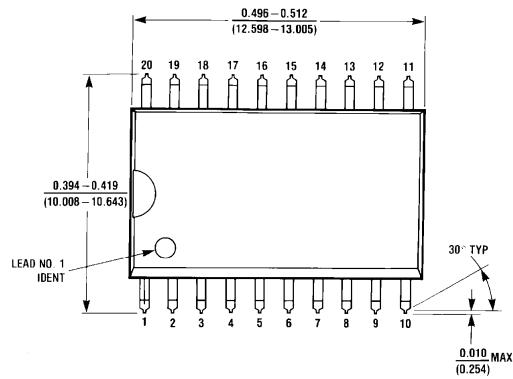
E20A (REV D)



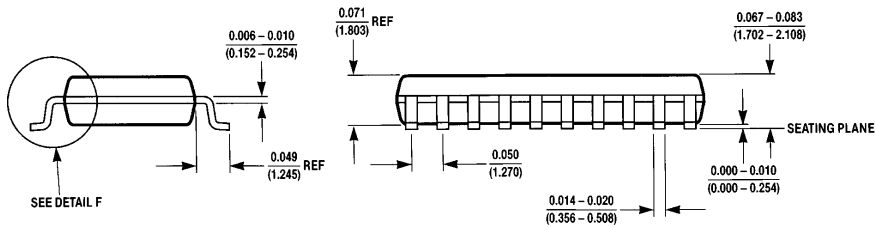
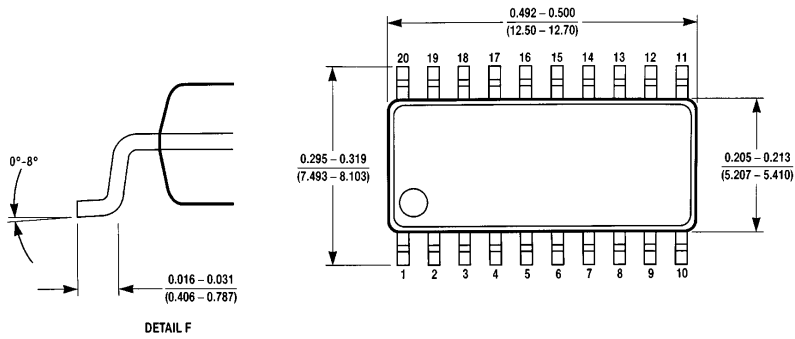
**20-Lead Ceramic Dual-In-Line Package (D)**  
 NS Package Number J20A

J20A (REV M)

**Physical Dimensions** inches (millimeters) (Continued)

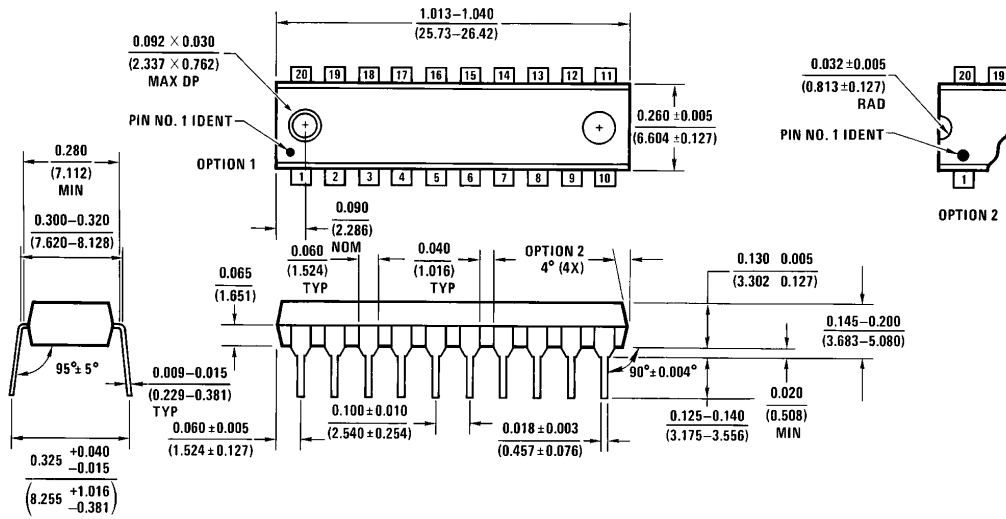
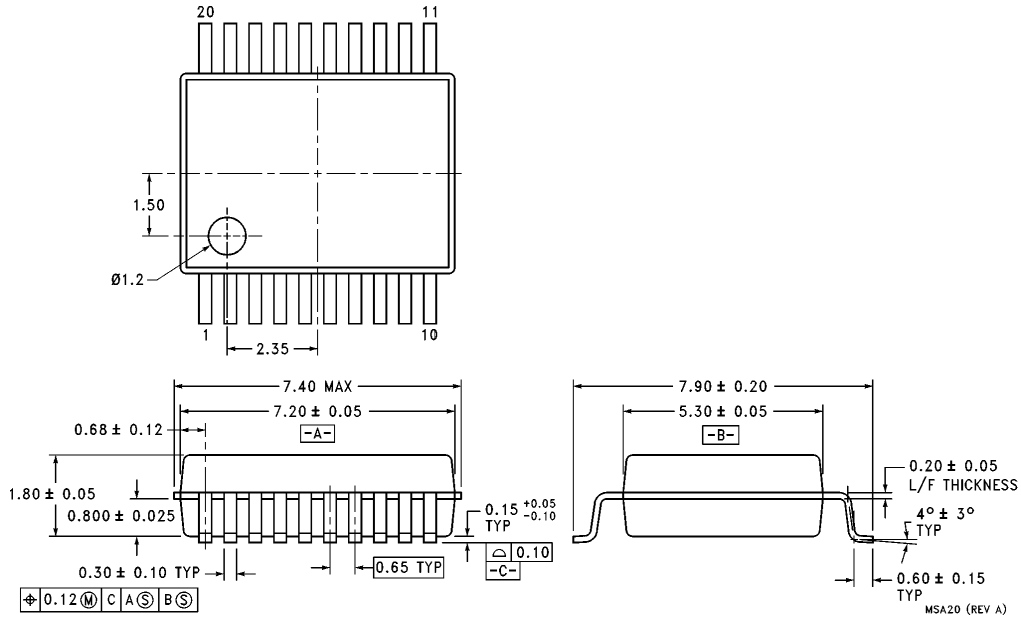


**20-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M20B**

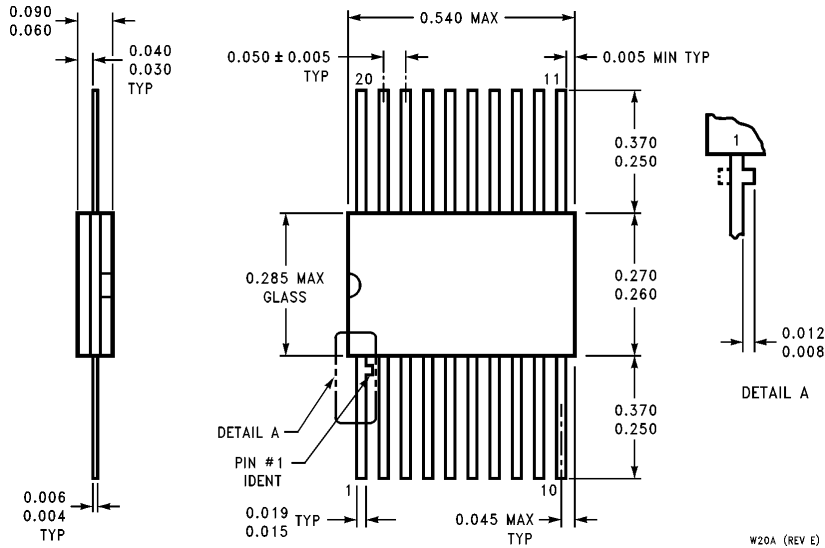


**20-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
NS Package Number M20D**

**Physical Dimensions** inches (millimeters) (Continued)



**Physical Dimensions** inches (millimeters) (Continued)



**20-Lead Ceramic Flatpak (F)  
NS Package Number W20A**

W20A (REV E)

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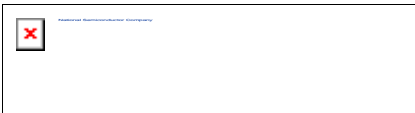
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## 54F374 Octal D Flip-Flop with Clock Enable

### Contents

- [General Description](#)
- [Features](#)
- [Datasheet](#)
- [Package Availability, Models, Samples & Pricing](#)

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### General Description




The 'F374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (OE#) are common to all flip-flops.

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### Features

- Edge-triggered D-type inputs
  - Buffered positive edge-triggered clock
  - TRI-STATE outputs for bus-oriented applications
  - Guaranteed 4000V minimum ESD protection
- 

### Datasheet

Title	Size (in Kbytes)	Date	 View Online	 Download	 Receive via Email
54F374 Octal D-Type Flip-Flop with TRI-STATE(RM) Outputs	175 Kbytes	9-Dec-97	<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>

54F374 Mil-Aero Datasheet MN54F374-X	23 Kbytes		<a href="#">View Online</a>	<a href="#">Download</a>	<a href="#">Receive via Email</a>
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## Package Availability, Models, Samples & Pricing

Part Number	Package		Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size
	Type	# pins		SPICE	IBIS		Quantity	\$US each	
54F374LMQB	LCC	20	Full production	N/A	N/A		50+	\$3.4000	tube of 50
54F374DM	Cerdip	20	Full production	N/A	N/A	.	50+	\$3.4000	tube of 20
54F374DMQB	Cerdip	20	Full production	N/A	N/A		50+	\$1.7000	tube of 20
54F374FMQB	Cerpack	20	Full production	N/A	N/A		50+	\$2.8000	tube of 19
54F374DC	Cerdip	20	Full production	N/A	N/A	.			tube of N/A
JM38510/34105B2	LCC	20	Full production	N/A	N/A	.	50+	\$4.5000	tube of 50
JM38510/34105BR	Cerdip	20	Full production	N/A	N/A	.	50+	\$1.9000	tube of 20
JM38510/34105BS	Cerpack	20	Full production	N/A	N/A	.	50+	\$4.5000	tube of 19
JD54F374SRA	Cerdip	20	Preliminary	N/A	N/A	.			tube of N/A
54F374 MW8	wafer		Full production	N/A	N/A	.			N/A

[Information as of 28-Jul-2000]

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