

CD4094BC 8-Bit Shift Register/Latch with 3-STATE Outputs

General Description

The CD4094BC consists of an 8-bit shift register and a 3-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_8) can be used to cascade several devices. Data on the Q_8 output is transferred to a second output, Q'_8 , on the following negative clock edge.

The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is HIGH, data propagates through the latch to 3-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken HIGH.

Features

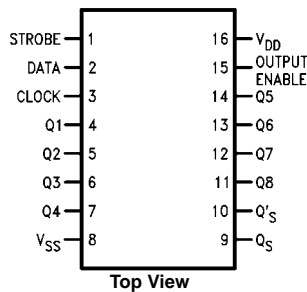
- Wide supply voltage range: 3.0V to 18V
- High noise immunity: $0.45 V_{DD}$ (typ.)
- Low power TTL compatibility:
 - Fan out of 2 driving 74L or 1 driving 74LS
- 3-STATE outputs

Ordering Code:

Order Number	Package Number	Package Description
CD4094BCWM	M16B	16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
CD4094BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Truth Table

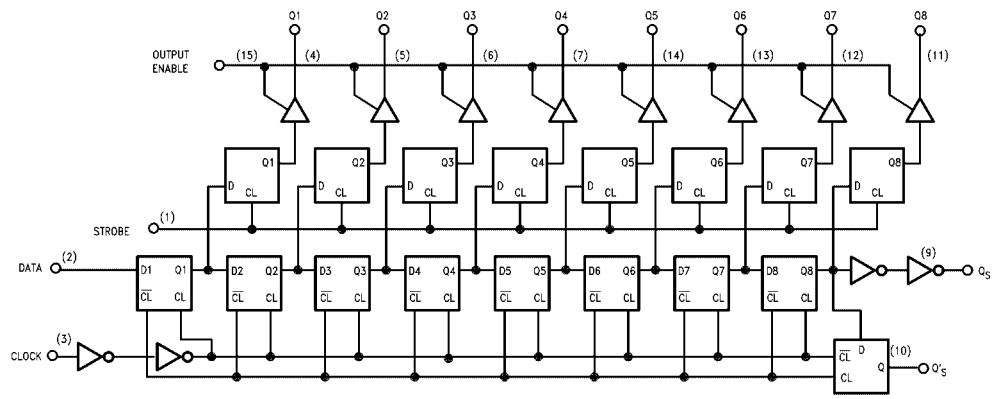
Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q_1	Q_N	Q_8 (Note 1)	Q'_8
~	0	X	X	Hi-Z	Hi-Z	Q7	No Change
~	0	X	X	Hi-Z	Hi-Z	No Change	Q7
~	1	0	X	No Change	No Change	Q7	No Change
~	1	1	0	0	Q_{N-1}	Q7	No Change
~	1	1	1	1	Q_{N-1}	Q7	No Change
~	1	1	1	No Change	No Change	No Change	Q7

X = Don't Care
~ = HIGH-to-LOW
~ = LOW-to-HIGH

Note 1: At the positive clock edge, information in the 7th shift register stage is transferred to Q_8 and Q'_8 .

CD4094BC

Block Diagram



Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 3)	
(Note 3)			
Supply Voltage (V_{DD})	-0.5 to +18 V_{DC}	DC Supply Voltage (V_{DD})	+3.0 to +15 V_{DC}
Input Voltage (V_{IN})	-0.5 to V_{DD} +0.5 V_{DC}	Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Storage Temperature Range (T_S)	-65°C to +150°C	Operating Temperature Range (T_A)	-55°C to +125°C
Power Dissipation (P_D)		Note 2: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.	
Dual-In-Line	700 mW	Note 3: $V_{SS} = 0V$ unless otherwise specified.	
Small Outline	500 mW		
Lead Temperature (T_L)			
(Soldering, 10 seconds)	260°C		

DC Electrical Characteristics (Note 3)

Symbol	Parameter	Conditions	55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$ $V_{DD} = 15V$		5.0 10 20				5.0 10 20		μA
V_{OL}	LOW Level Output Voltage	$V_{DD} = 5.0V$ $V_{DD} = 10V$ $ I_O \leq 1.0 \mu A$ $V_{DD} = 15V$		0.05 0.05 0.05		0 0 0		0.05 0.05 0.05		V
V_{OH}	HIGH Level Output Voltage	$V_{DD} = 5.0V$ $V_{DD} = 10V$ $ I_O \leq 1 \mu A$ $V_{DD} = 15V$	4.95 9.95 14.95		4.95 9.95 14.95	5.0 10.0 15.0		4.95 9.95 14.95		V
V_{IL}	LOW Level Input Voltage	$V_{DD} = 5.0V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1.0V$ or 9.0V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V		1.5 3.0 4.0				1.5 3.0 4.0		V
V_{IH}	HIGH Level Input Voltage	$V_{DD} = 5.0V, V_O = 0.5V$ or 4.5V $V_{DD} = 10V, V_O = 1.0V$ or 9.0V $V_{DD} = 15V, V_O = 1.5V$ or 13.5V	3.5 7.0 11.0		3.5 7.0 11.0			3.5 7.0 11.0		V
I_{OL}	LOW Level Output Current (Note 4)	$V_{DD} = 5.0V, V_O = 0.4V$ $V_{DD} = 10V, V_O = 0.5V$ $V_{DD} = 15V, V_O = 1.5V$	0.64 1.6 4.2		0.51 1.3 3.4	0.88 2.25 8.8		0.36 0.9 2.4		mA
I_{OH}	HIGH Level Output Current (Note 4)	$V_{DD} = 5.0V, V_O = 4.6V$ $V_{DD} = 10V, V_O = 9.5V$ $V_{DD} = 15V, V_O = 13.5V$	-0.64 -1.6 -4.2		-0.51 -1.3 -3.4	0.88 2.25 8.8		-0.36 -0.9 -2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V, V_{IN} = 0V$ $V_{DD} = 15V, V_{IN} = 15V$		-0.1 0.1				-0.1 0.1		μA
I_{OZ}	3-STATE Output Leakage Current	$V_{DD} = 15V, V_{IN} = 0V$ or 15V		0.3				± 0.3		μA

Note 4: I_{OH} and I_{OL} are tested one output at a time.

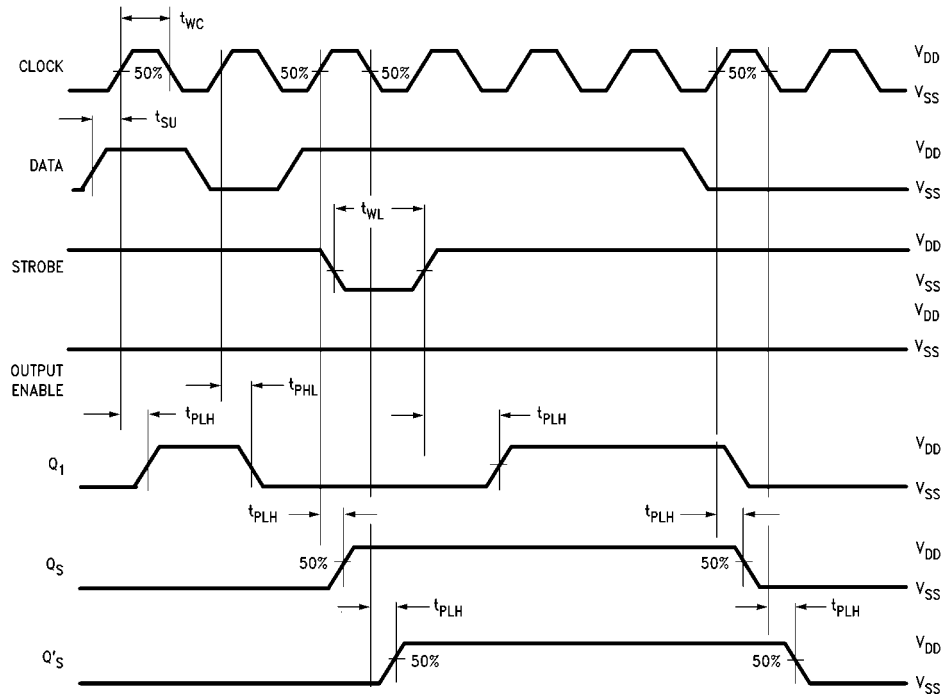
AC Electrical Characteristics (Note 5)

$T_A = 25^\circ\text{C}$, $C_L = 50\text{ pF}$

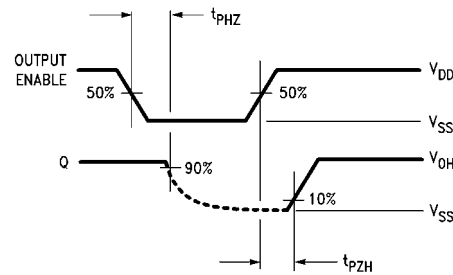
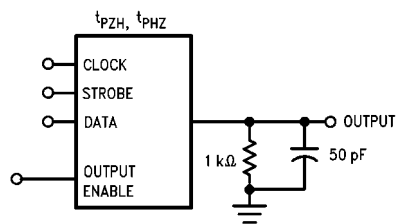
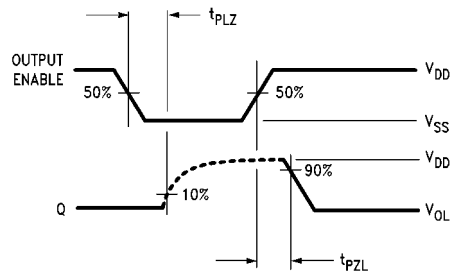
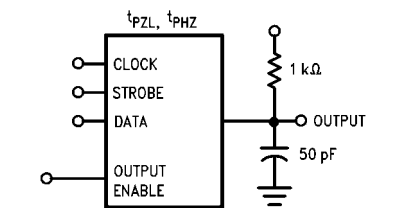
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL} , t_{PLH}	Propagation Delay Clock to Q_S	$V_{DD} = 5.0\text{V}$		300	600	ns
		$V_{DD} = 10\text{V}$		125	250	
		$V_{DD} = 15\text{V}$		95	190	
t_{PHL} , t_{PLH}	Propagation Delay Clock to Q'_S	$V_{DD} = 5.0\text{V}$		230	460	ns
		$V_{DD} = 10\text{V}$		110	220	
		$V_{DD} = 15\text{V}$		75	150	
t_{PHL} , t_{PLH}	Propagation Delay Clock to Parallel Out	$V_{DD} = 5.0\text{V}$		420	840	ns
		$V_{DD} = 10\text{V}$		195	390	
		$V_{DD} = 15\text{V}$		135	270	
t_{PHL} , t_{PLH}	Propagation Delay Strobe to Parallel Out	$V_{DD} = 5.0\text{V}$		290	580	ns
		$V_{DD} = 10\text{V}$		145	290	
		$V_{DD} = 15\text{V}$		100	200	
t_{PHZ}	Propagation Delay HIGH Level to HIGH Impedance	$V_{DD} = 5.0\text{V}$		140	280	ns
		$V_{DD} = 10\text{V}$		75	150	
		$V_{DD} = 15\text{V}$		55	110	
t_{PLZ}	Propagation Delay LOW Level to HIGH Impedance	$V_{DD} = 5.0\text{V}$		140	280	ns
		$V_{DD} = 10\text{V}$		75	150	
		$V_{DD} = 15\text{V}$		55	110	
t_{PZH}	Propagation Delay HIGH Impedance to HIGH Level	$V_{DD} = 5.0\text{V}$		140	280	ns
		$V_{DD} = 10\text{V}$		75	150	
		$V_{DD} = 15\text{V}$		55	110	
t_{PZL}	Propagation Delay HIGH Impedance to LOW Level	$V_{DD} = 5.0\text{V}$		140	280	ns
		$V_{DD} = 10\text{V}$		75	150	
		$V_{DD} = 15\text{V}$		55	110	
t_{THL} , t_{TLH}	Transition Time	$V_{DD} = 5.0\text{V}$		100	200	ns
		$V_{DD} = 10\text{V}$		50	100	
		$V_{DD} = 15\text{V}$		40	80	
t_{SU}	Set-Up Time Data to Clock	$V_{DD} = 5.0\text{V}$	80	40		ns
		$V_{DD} = 10\text{V}$	40	20		
		$V_{DD} = 15\text{V}$	20	10		
t_r , t_f	Maximum Clock Rise and Fall Time	$V_{DD} = 5.0\text{V}$	1			ms
		$V_{DD} = 10\text{V}$	1			
		$V_{DD} = 15\text{V}$	1			
t_{PC}	Minimum Clock Pulse Width	$V_{DD} = 5.0\text{V}$	200	100		ns
		$V_{DD} = 10\text{V}$	100	50		
		$V_{DD} = 15\text{V}$	83	40		
t_{PS}	Minimum Strobe Pulse Width	$V_{DD} = 5.0\text{V}$	200	100		ns
		$V_{DD} = 10\text{V}$	80	40		
		$V_{DD} = 15\text{V}$	70	35		
f_{max}	Maximum Clock Frequency	$V_{DD} = 5.0\text{V}$	1.5	3.0		MHz
		$V_{DD} = 10\text{V}$	3.0	6.0		
		$V_{DD} = 15\text{V}$	4.0	8.0		
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 5: AC Parameters are guaranteed by DC correlated testing.

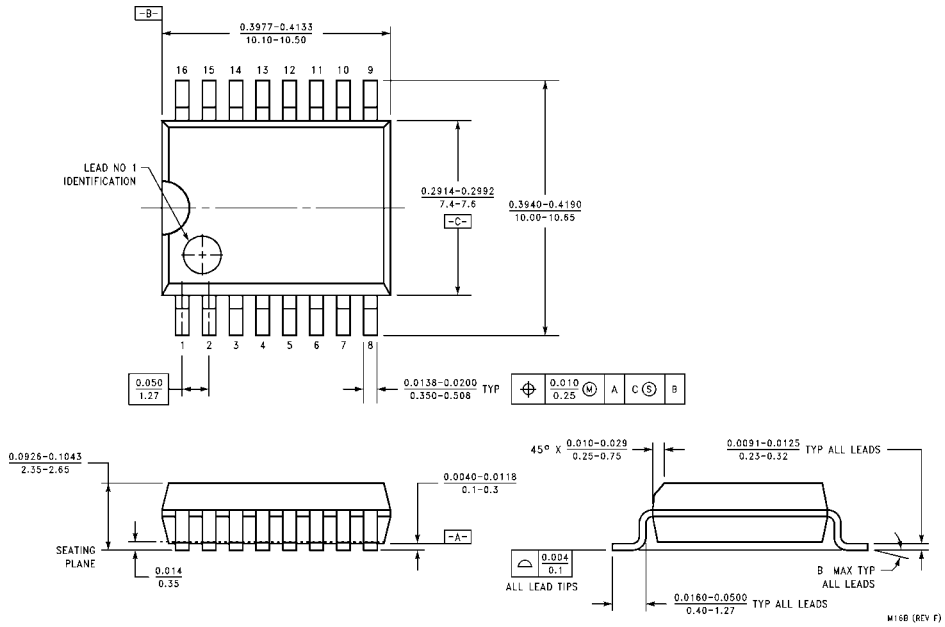
Timing Diagram



Test Circuits and Timing Diagrams for 3-STATE

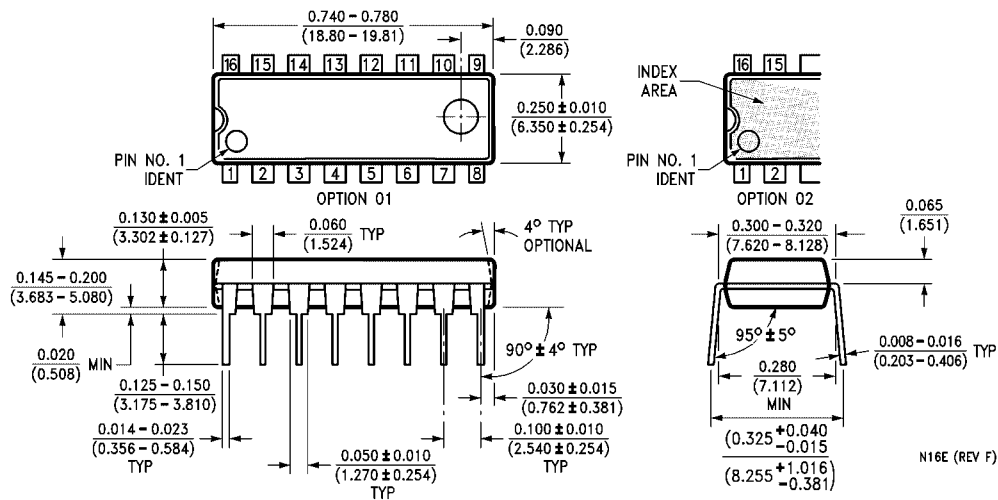


Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Intergrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M16B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E**

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