CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T

December 1996

High-Speed CMOS Dual 4-Input Multiplexers

Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pin Compatible with Bipolar FAST™ Series at a Higher Speed and Lower Power Consumption
- 25Ω Series Resistor On All Outputs (FCT2XXX Only)
- TTL Input and Output Levels
- Low Ground Bounce Outputs (25Ω Series Only)
- Extremely Low Static Power
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74FCT153TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT153TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT153TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT153ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT153CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT253TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT253TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT253CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2153TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2153TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2153CTQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253TM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253ATM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253CTM	-40 to 85	16 Ld SOIC	M16.3-P
CD74FCT2253TNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253ATNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253CTNM	-40 to 85	16 Ld SOIC	M16.15-P
CD74FCT2253TQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253ATQM	-40 to 85	16 Ld QSOP	M16.15A-P
CD74FCT2253CTQM	-40 to 85	16 Ld QSOP	M16.15A-P

NOTE: When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

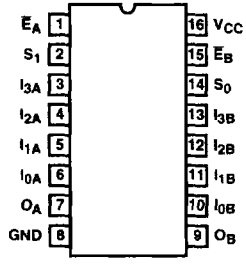
Description

The CD74FCT153T, CD74FCT253T, CD74FCT2153T and CD74FCT2253T are high-speed dual 4-input multiplexers. The CD74FCT153T and CD74FCT2153T have TTL outputs, while the CD74FCT253T and CD74FCT2253T have three-state outputs. The output buffers are designed with a poweroff disable allowing 'live insertion' of boards when used as backplane drivers.

The CD74FCT2153T and CD74FCT2253T devices have a built-in 25Ω series resistor on all outputs to reduce noise due to reflections, thus eliminating the need for an external terminating resistor.

Pinout

CD74FCT153T, CD74FCT253T, CD74FCT2153T, CD74FCT2253T (QSOP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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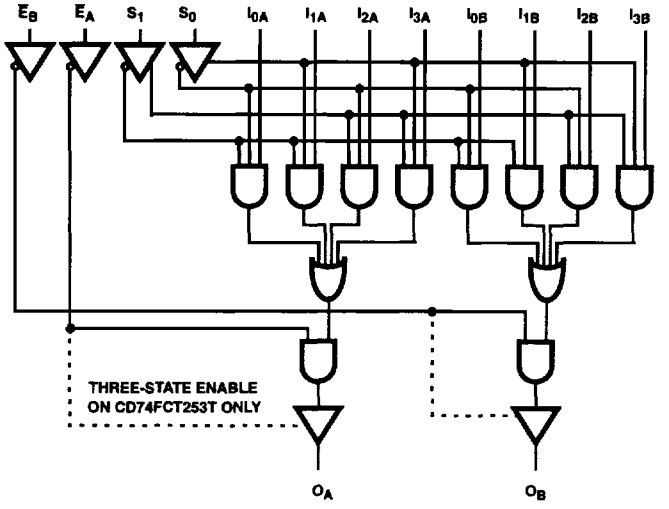
File Number **4161.2**

Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS				OUTPUTS			
				CD74FCT153, CD74FCT2153		CD74FCT253, CD74FCT2253	
$\overline{E}_A$	$\overline{E}_B$	S_1	S_0	O_A	O_B	O_A	O_B
H	X	X	X	L	X	Z	X
X	H	X	X	X	L	X	Z
L	L	L	L	I_{0A}	I_{0B}	I_{0A}	I_{0B}
L	L	L	H	I_{1A}	I_{1B}	I_{1A}	I_{1B}
L	L	H	L	I_{2A}	I_{2B}	I_{2A}	I_{2B}
L	L	H	H	I_{3A}	I_{3B}	I_{3A}	I_{3B}

NOTE:

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   Z = High Impedance

Pin Description

PIN NAME	DESCRIPTION
I_{0A}-I_{3A}, I_{0B}-I_{3B}	Data Inputs
S_0, S_1	Select Inputs
$\overline{E}_A$, $\overline{E}_B$	Enable Input
O_A, O_B	Data Outputs
GND	Ground
V_{CC}	Power

Absolute Maximum Ratings

DC Input Voltage . . . . . -0.5V to 7.0V
DC Output Current 120mA

Operating Conditions

Operating Temperature Range . . . . . -40°C to 85°C
Supply Voltage to Ground Potential
Inputs and V_{CC} Only . . . . . -0.5V to 7.0V
Supply Voltage to Ground Potential
Outputs and D/O Only . . . . . -0.5V to 7.0V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)
16 Lead SOIC (150 mil) Package	110
16 Lead SOIC (300 mil) Package	97
16 Lead QSOP Package	140

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied

NOTE:

2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS		MIN	(NOTE 4) TYP	MAX	UNITS
DC ELECTRICAL SPECIFICATIONS Over the Operating Range, T_A = -40°C to 85°C, V_{CC} = 5.0V ± 5%							
Output HIGH Voltage	V_{OH}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = -15.0mA	2.4	3.0	-	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA	-	0.3	0.50	V
Output LOW Voltage	V_{OL}	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA (25Ω series)	-	0.3	0.50	V
Input HIGH Voltage	V_{IH}	Guaranteed Logic HIGH Level		2.0	-	-	V
Input LOW Voltage	V_{IL}	Guaranteed Logic LOW Level		-	-	0.8	V
Input HIGH Current	I_{IH}	V_{CC} = Max	V_{IN} = V_{CC}	-	-	1	µA
Input LOW Current	I_{IL}	V_{CC} = Max	V_{IN} = GND	-	-	-1	µA
High Impedance Output Current	I_{OZH}, I_{OZL}	V_{CC} = Max	V_{OUT} = 2.7V			1	µA
			V_{OUT} = 0.5V			-1	µA
Clamp Diode Voltage	V_{IK}	V_{CC} = Min, I_{IN} = -18mA		-	-0.7	-1.2	V
Short Circuit Current	I_{OS}	V_{CC} = Max (Note 5), V_{OUT} = GND		-60	-120	-	mA
Power Down Disable	I_{OFF}	V_{CC} = GND, V_{OUT} = 4.5V		-	-	100	µA
Input Hysteresis	V_H			-	200	-	mV
CAPACITANCE T_A = 25°C, f = 1MHz							
Input Capacitance (Note 6)	C_{IN}	V_{IN} = 0V		-	6	10	pF
Output Capacitance (Note 6)	C_{OUT}	V_{OUT} = 0V		-	8	12	pF
POWER SUPPLY SPECIFICATIONS							
Quiescent Power Supply Current	I_{CC}	V_{CC} = Max	V_{IN} = GND or V_{CC}	-	0.1	500	µA
Supply Current per Input at TTL HIGH	ΔI_{CC}	V_{CC} = Max	V_{IN} = 3.4V (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	I_{CCD}	V_{CC} = Max, Outputs Open Other Inputs at GND One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	-	0.15	0.25	mA/ MHz
Total Power Supply Current (Note 10)	I_C	V_{CC} = Max, Outputs Open f_i = 10MHz, 50% Duty Cycle Other Inputs at GND One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND	-	3.2	6.5 (Note 9)	mA
			V_{IN} = 3.4V V_{IN} = GND	-	3.5	7.5 (Note 9)	mA

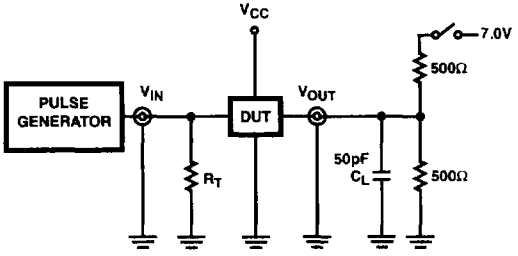
Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	T (NOTE 12) MIN	T MAX	AT (NOTE 12) MIN	AT MAX	CT (NOTE 12) MIN	CT MAX	UNIT
CD74FCT153T, CD74FCT2153T									
Propagation Delay Sn to O	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay In to O	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.5	ns
Propagation Delay $\overline{E}$ to O	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.8	ns
CD74FCT253T, CD74FCT2253T									
Propagation Delay Sn to O	t_{PLH}, t_{PHL}	C_L = 50pF R_L = 500Ω	1.5	9.0	1.5	6.6	1.5	5.6	ns
Propagation Delay In to O	t_{PLH}, t_{PHL}		1.5	7.0	1.5	5.2	1.5	4.5	ns
Output Enable Time $\overline{E}$ to O	t_{PZH}, t_{PZL}		1.5	9.0	1.5	6.0	1.5	5.0	ns
Output Enable Time $\overline{E}$ to O (Note 13)	t_{PHZ}, t_{PLZ}		1.5	7.0	1.5	6.0	1.5	5.0	ns

NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is determined by device characterization but is not production tested.
7. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
8. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
9. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
10. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
    $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
    I_{CC} = Quiescent Current
    ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
    D_H = Duty Cycle for TTL Inputs High
    N_T = Number of TTL Inputs at D_H
    I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
    f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
    f_i = Input Frequency
    N_i = Number of Inputs at f_i
    All currents are in milliamps and all frequencies are in megahertz.
11. See test circuit and wave forms.
12. Minimum limits are guaranteed but not tested on Propagation Delays.
13. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



SWITCH POSITION

TEST	SWITCH
t_{PLZ}, t_{PZL}	Closed
t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

NOTE:

14. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; Z_{OUT} ≤ 50Ω; t_f, t_r ≤ 2.5ns.

FIGURE 1. TEST CIRCUIT

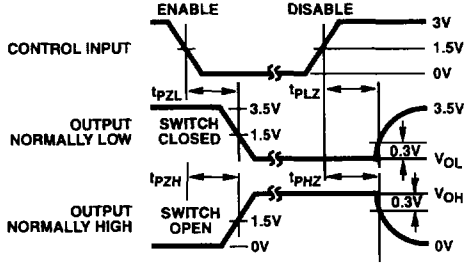


FIGURE 2. ENABLE AND DISABLE TIMING

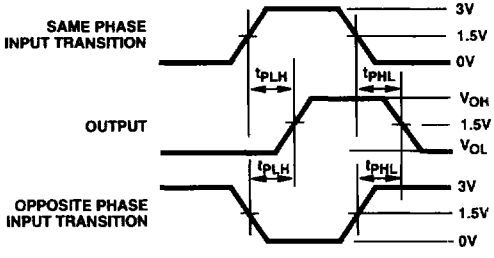


FIGURE 3. PROPAGATION DELAY