MC74HC125A, MC74HC126A

Quad 3-State Noninverting Buffers

High−Performance Silicon−Gate CMOS

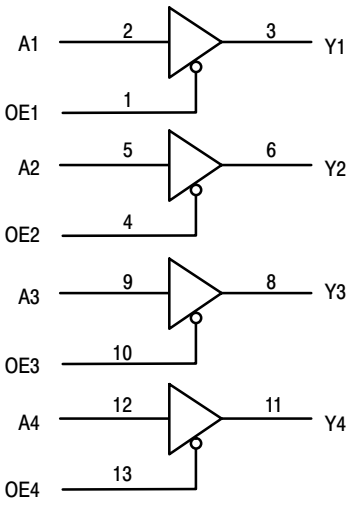
The MC74HC125A and MC74HC126A are identical in pinout to the LS125 and LS126. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC125A and HC126A noninverting buffers are designed to be used with 3−state memory address drivers, clock drivers, and other bus−oriented systems. The devices have four separate output enables that are active−low (HC125A) or active−high (HC126A).

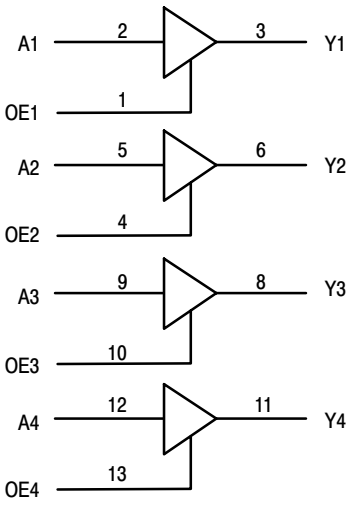
- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 72 FETs or 18 Equivalent Gates

LOGIC DIAGRAM

HC125A
Active−Low Output Enables



HC126A
Active−High Output Enables



PIN 14 = V_{CC}
PIN 7 = GND

FUNCTION TABLE

HC125A		
Inputs		Output
A	OE	Y
H	L	H
L	L	L
X	H	Z

HC126A		
Inputs		Output
A	OE	Y
H	H	H
L	H	L
X	L	Z

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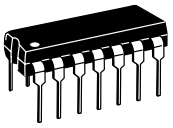
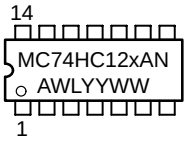
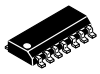
MARKING DIAGRAMS

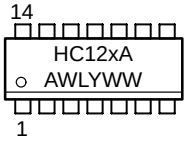


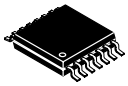
PDIP−14
N SUFFIX
CASE 646



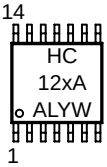


SOIC−14
D SUFFIX
CASE 751A



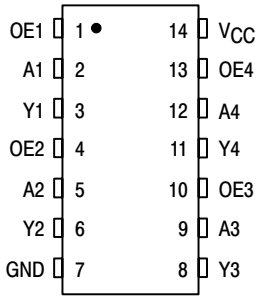


TSSOP−14
DT SUFFIX
CASE 948G



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping
MC74HC12xAN	PDIP−14	2000 / Box
MC74HC12xAD	SOIC−14	55 / Rail
MC74HC12xADR2	SOIC−14	2500 / Reel
MC74HC12xADT	TSSOP−14	96 / Rail
MC74HC12xADTR2	TSSOP−14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	– 0.5 to V_{CC} + 0.5	V
I_{in}	DC Input Current, per Pin	± 20	mA
I_{out}	DC Output Current, per Pin	± 35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air Plastic DIP†	750	mW
	SOIC Package†	500	
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC or TSSOP Package)	260	C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
†Derating — Plastic DIP: – 10 mW/ C from 65 to 125 C
SOIC Package: – 7 mW/ C from 65 to 125 C
TSSOP Package: – 6.1 mW/ C from 65 to 125 C
For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage (Referenced to GND)		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 55	+ 125	C
t_r, t_f	Input Rise and Fall Time (Figure 1)	V_{CC} = 2.0 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6.0 V	0	400	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				– 55 to 25 C	≤ 85 C	≤ 125 C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = V_{CC} – 0.1 V, $\|I_{out}\|$ ≤ 20 μA	2.0	1.5	1.5	1.5	V
			3.0	2.1	2.1	2.1	
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V, $\|I_{out}\|$ ≤ 20 μA	2.0	0.5	0.5	0.5	V
			3.0	0.9	0.9	0.9	
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH}, $\|I_{out}\|$ ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V_{in} = V_{IH}, $\|I_{out}\|$ ≤ 3.6 mA	3.0	2.48	2.34	2.2	
		$\|I_{out}\|$ ≤ 6.0 mA	4.5	3.98	3.84	3.7	
		$\|I_{out}\|$ ≤ 7.8 mA	6.0	5.48	5.34	5.2	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IL}, $\|I_{out}\|$ ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V_{in} = V_{IL}, $\|I_{out}\|$ ≤ 3.6 mA	3.0	0.26	0.33	0.4	
		$\|I_{out}\|$ ≤ 6.0 mA	4.5	0.26	0.33	0.4	
		$\|I_{out}\|$ ≤ 7.8 mA	6.0	0.26	0.33	0.4	

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				− 55 to 25 C	≤ 85 C	≤ 125 C	
I_{in}	Maximum Input Leakage Current	$V_{in} = V_{CC}$ or GND	6.0	± 0.1	± 1.0	± 1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State $V_{in} = V_{IL}$ or V_{IH} $V_{out} = V_{CC}$ or GND	6.0	± 0.5	± 5.0	± 10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input $t_r = t_f$ = 6.0 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			− 55 to 25 C	≤ 85 C	≤ 125 C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 3)	2.0 3.0 4.5 6.0	90 36 18 15	115 45 23 20	135 60 27 23	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	120 45 24 20	150 60 30 26	180 80 36 31	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Y (Figures 2 and 4)	2.0 3.0 4.5 6.0	90 36 18 15	115 45 23 20	135 60 27 23	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0 3.0 4.5 6.0	60 22 12 10	75 28 15 13	90 34 18 15	ns
C_{in}	Maximum Input Capacitance	—	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	—	15	15	15	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Buffer)*	30	pF

* Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High−Speed CMOS Data Book (DL129/D).

SWITCHING WAVEFORMS

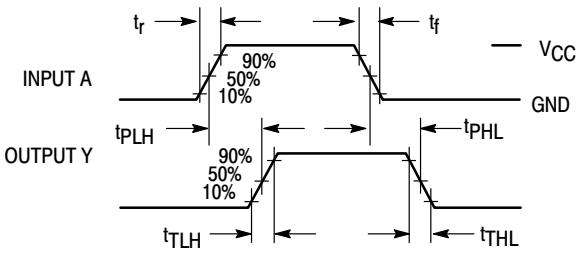


Figure 1.

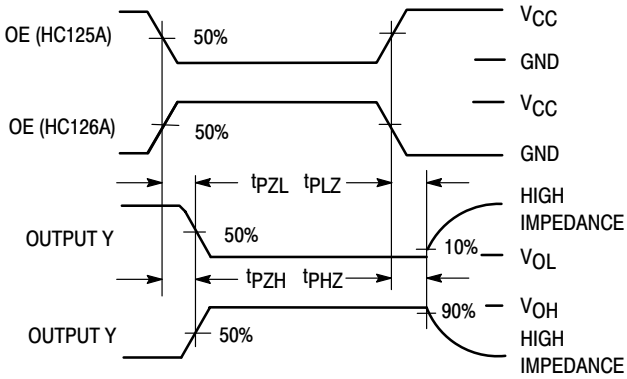
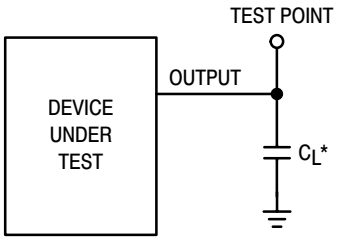
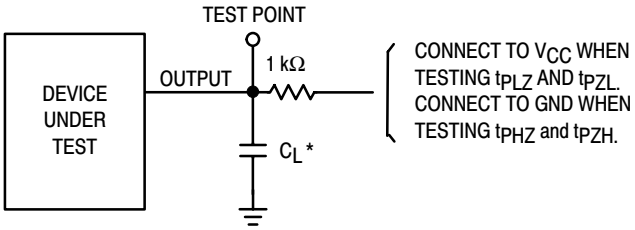


Figure 2.



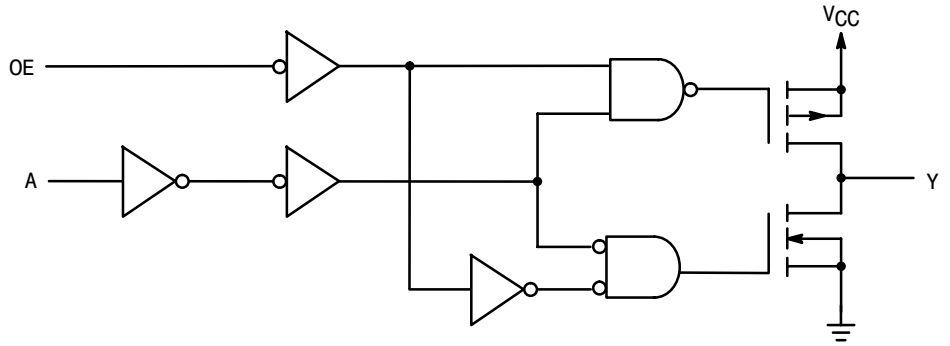
*Includes all probe and jig capacitance

Figure 3. Test Circuit

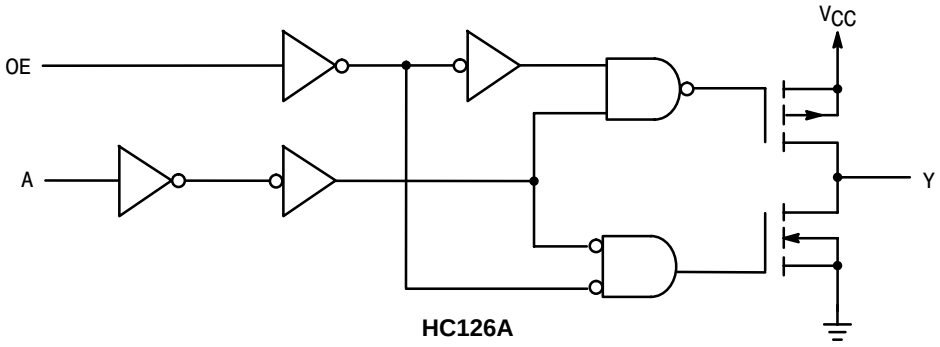


*Includes all probe and jig capacitance

Figure 4. Test Circuit



HC125A
(1/4 OF THE DEVICE)



HC126A
(1/4 OF THE DEVICE)