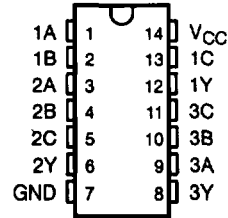


# SN74LVC10 TRIPLE 3-INPUT POSITIVE-NAND GATE

SCAS284B – JANUARY 1993 – REVISED JULY 1995

- **EPIC™** (Enhanced-Performance Implanted CMOS) Submicron Process
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JEDEC Standard JESD-17**
- **Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3 V, T_A = 25^\circ C$**
- **Inputs Accept Voltages to 5.5 V**
- **Package Options Include Plastic Small-Outline (D), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

D, DB, OR PW PACKAGE  
(TOP VIEW)



## description

This triple 3-input positive-NAND gate is designed for 2.7-V to 3.6-V  $V_{CC}$  operation. The SN74LVC10 performs the Boolean functions  $Y = \overline{A \cdot B \cdot C}$  or  $Y = \overline{A + B + C}$  in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of these devices as translators in a mixed 3.3-V/5-V system environment.

The SN74LVC10 is characterized for operation from  $-40^\circ C$  to  $85^\circ C$ .

**FUNCTION TABLE**  
(each gate)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	L
L	X	X	H
X	L	X	H
X	X	L	H

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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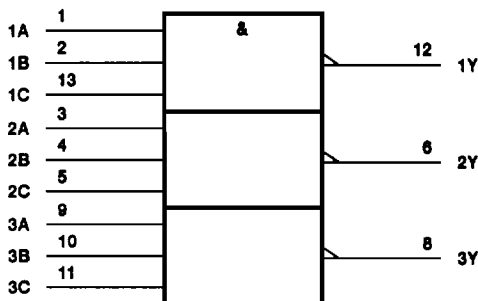
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# SN74LVC10

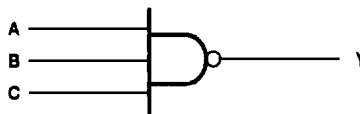
## TRIPLE 3-INPUT POSITIVE-NAND GATE

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### logic symbol†



### logic diagram, each gate (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, $V_{CC}$ .....	-0.5 V to 6.5 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to 6.5 V
Output voltage range, $V_O$ (see Notes 1 and 2) .....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	±50 mA
Continuous current through $V_{CC}$ or GND .....	±100 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 3): D package .....	1.25 W
DB or PW package .....	0.5 W
Storage temperature range, $T_{stg}$ .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This value is limited to 4.6 V maximum.  
 3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

### recommended operating conditions (see Note 4)

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	Operating	2	3.6	V
		Data retention only	1.5		
$V_{IH}$	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		V	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	
$V_I$	Input voltage	0	5.5	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$I_{OH}$	High-level output current	$V_{CC} = 2.7$ V	-12	mA	
		$V_{CC} = 3$ V	-24		
$I_{OL}$	Low-level output current	$V_{CC} = 2.7$ V	12	mA	
		$V_{CC} = 3$ V	24		
$T_A$	Operating free-air temperature	-40	85	°C	

NOTE 4: Unused inputs must be held high or low to prevent them from floating.



# SN74LVC10

## TRIPLE 3-INPUT POSITIVE-NAND GATE

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> †	MIN	TYP‡	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -100 µA	MIN to MAX	V <sub>CC</sub> -0.2			V
	I <sub>OH</sub> = -12 mA	2.7 V	2.2			
	I <sub>OH</sub> = -24 mA	3 V	2.4			
V <sub>OL</sub>	I <sub>OL</sub> = 100 µA	MIN to MAX			0.2	V
	I <sub>OL</sub> = 12 mA	2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10	µA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	µA
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5			pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

‡ All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

**switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	6		7	ns
t <sub>sk(o)</sub> §			1				ns

§ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

**operating characteristics, V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C**

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance per gate	C <sub>L</sub> = 50 pF, f = 10 MHz	11	pF

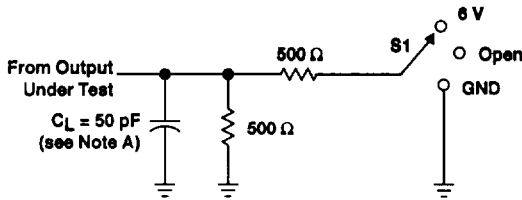


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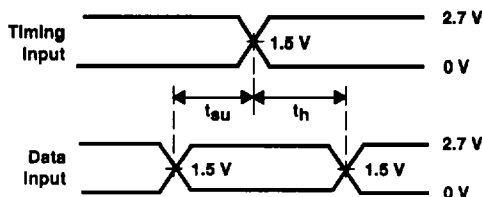
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## PARAMETER MEASUREMENT INFORMATION

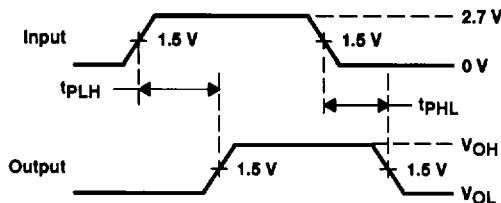
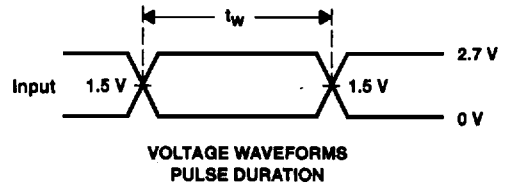


LOAD CIRCUIT

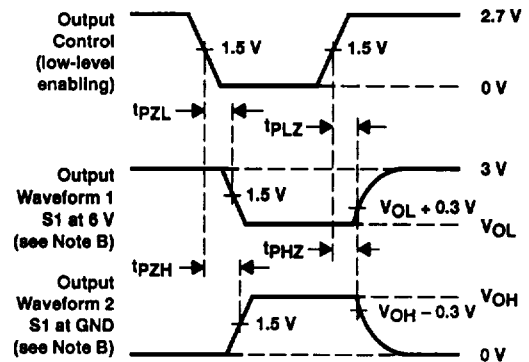
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

