

**High Performance 1:5 LVPECL Fanout Buffer**

**Features**

- 5 LVPECL Outputs
- Up to 1.5GHz Output Frequency
- Ultra Low Additive Phase Jitter: < 0.03ps (typ) (differential 156.25MHz, 12KHz to 20MHz integration range)
- Two Selectable Inputs. LVPECL, LVDS, HCSL, CML, etc.
- Low Delay from Input to Output (Tpd typ. 1.5ns)
- 3.3V Power Supply
- Industrial Temperature Support
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. “Green” Device (Note 3)
- For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact@diodes.com) or your local Diodes representative.  
<https://www.diodes.com/quality/product-definitions/>
- Packaging (Pb-free & Green):
  - 20-pin, TSSOP (L)

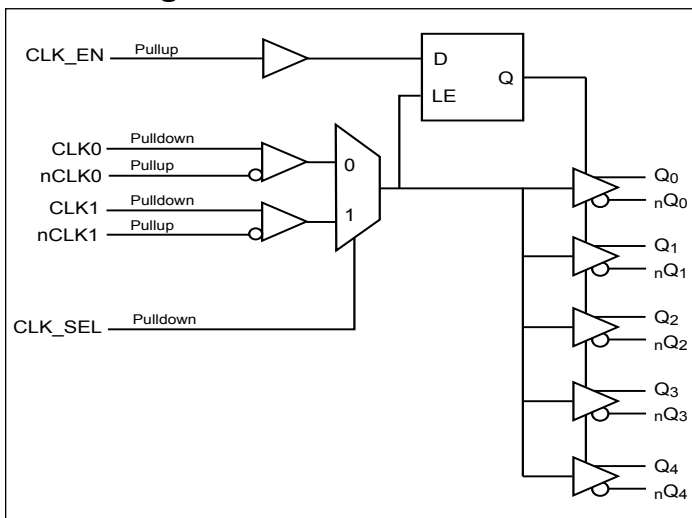
**Description**

The PI6C4911505 is a high performance fanout buffer device which supports up to 1.5GHz frequency. The device has 2 selectable clock inputs that can accept most differential clock sources. This device is ideal for systems that need to distribute low jitter clock signals to multiple destinations.

**Applications**

- Networking Systems including Switches and Routers
- High Frequency Backplane based Computing and Telecom Platforms

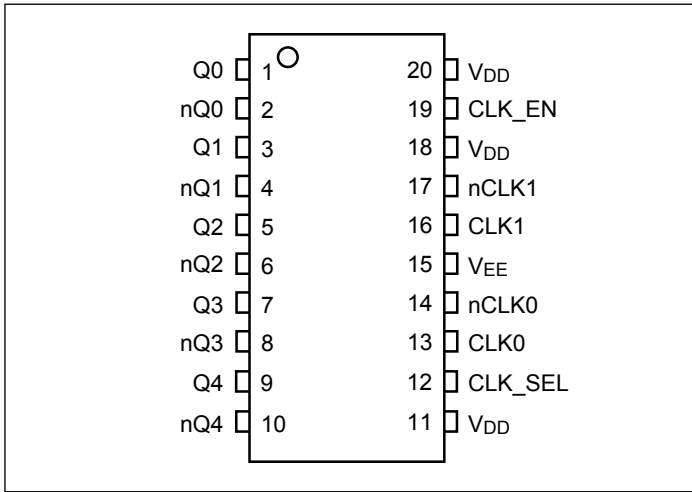
**Block Diagram**



**Notes:**

1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated’s definitions of Halogen- and Antimony-free, “Green” and Lead-free.
3. Halogen- and Antimony-free “Green” products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Pin Configuration



## Pin Description

Pin #	Pin Name	Type		Description
1, 2	Q0 nQ0	Output		LVPECL output clock
3, 4	Q1 nQ1	Output		LVPECL output clock
5, 6	Q2 nQ2	Output		LVPECL output clock
7, 8	Q3 nQ3	Output		LVPECL output clock
9, 10	Q4 nQ4	Output		LVPECL output clock
11, 18, 20	V <sub>DD</sub>	Power		Power supply
12	CLK_SEL	Input	Pulldown	Clock input source selection pin
13, 14	CLK0 nCLK0	Input	Pulldown Pullup	Differential clock input
15	V <sub>EE</sub>	Power		Negative power supply
16, 17	CLK1 nCLK1	Input	Pulldown Pullup	Differential clock input
19	CLK_EN	Input	Pullup	Clock output enable/ disable

## Function Table

Table 1: Input Select Function

CLK_SEL	Function
0	CLK0, nCLK0
1	CLK1, nCLK1

Table 2: Output Mode Select Function

CLK_EN	Outputs	
	Q0:Q4	nQ0:nQ4
0	Disabled; LOW	Disabled; HIGH
1	Enabled	Enabled

**PI6C4911505**

**Maximum Ratings** (Above which the useful life may be impaired. For user guidelines, not tested)

Storage Temperature.....	-55 to +150°C
Junction Temperature Max .....	125°C
Supply Voltage to Ground Potential (V <sub>DD</sub> ).....	-0.5 to +4.6V
Inputs (Referenced to GND) .....	-0.5 to V <sub>DD</sub> +0.5V
Clock Output (Referenced to GND).....	-0.5 to V <sub>DD</sub> +0.5V
Latch up .....	200mA
ESD Protection (Input).....	2000V min (HBM)

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Power Supply Characteristics and Operating Conditions**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V <sub>DD</sub>	Core Supply Voltage		3.135	3.3	3.465	V
I <sub>DD</sub>	Power Supply Current	All outputs unloaded			160	mA
T <sub>A</sub>	Ambient Operating Temperature		-40		85	°C

**DC Electrical Specifications - Differential Inputs**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
I <sub>IH</sub>	Input High current: CLK0, CLK1	Input = V <sub>DD</sub>			200	uA
	Input High current: nCLK0, nCLK1	Input = V <sub>DD</sub>			10	uA
I <sub>IL</sub>	Input Low current: CLK0, CLK1	Input = GND	-200			uA
	Input Low current: nCLK0, nCLK1	Input = GND	-200			uA
C <sub>IN</sub>	Input capacitance			4		pF
V <sub>IH</sub>	Input high voltage				V <sub>DD</sub> +0.3	V
V <sub>IL</sub>	Input low voltage		-0.3			V
V <sub>ID</sub>	Input Differential Amplitude PK-PK		0.15		V <sub>DD</sub> -0.85	V
V <sub>CM</sub>	Common mode input voltage		GND + 0.5		V <sub>DD</sub> -0.85	V

### DC Electrical Specifications - LVCMOS Inputs

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{IH}$	Input High current	Input = $V_{DD}$			200	$\mu A$
$I_{IL}$	Input Low current	Input = GND	-200			$\mu A$
$V_{IH}$	Input high voltage	$V_{DD}=3.3V$	2.0		$V_{DD}+0.3$	V
$V_{IL}$	Input low voltage	$V_{DD}=3.3V$	-0.3		0.8	V

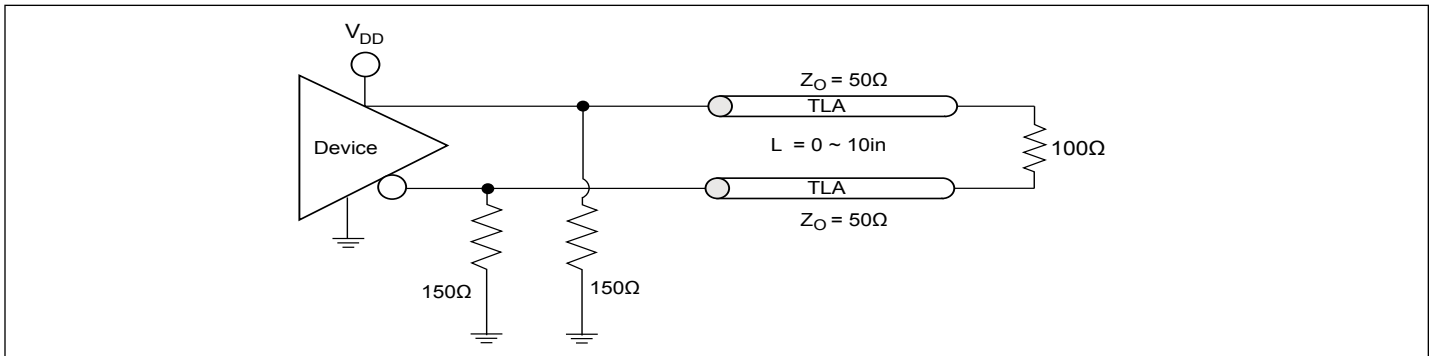
### DC Electrical Specifications- LVPECL Outputs

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
$V_{OH}$	Output High voltage	$V_{DD}=3.3V$	2.1		2.6	V
$V_{OL}$	Output Low voltage	$V_{DD}=3.3V$	1.3		1.8	V

### AC Electrical Specifications

Parameter	Description	Conditions	Min.	Typ.	Max.	Units
$F_{OUT}$	Clock output frequency	LVPECL			1500	MHz
$T_r$	Output rise time	From 20% to 80%		150		ps
$T_f$	Output fall time	From 80% to 20%		150		ps
$T_{ODC}$	Output duty cycle	Frequency<650MHz	48		52	%
$V_{PP}$	Output swing Single-ended	LVPECL outputs	400			mV
$T_j$	Buffer additive jitter RMS			0.03		ps
$T_{SK}$	Output Skew	5 outputs devices, outputs in same bank, with same load, at DUT.		40		ps
$T_{PD}$	Propagation Delay			1500		ps

### Configuration Test Load Board Termination for LVPECL



### Application Information

#### Wiring the differential input to accept single ended levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R1/R2 = 0.609$ .

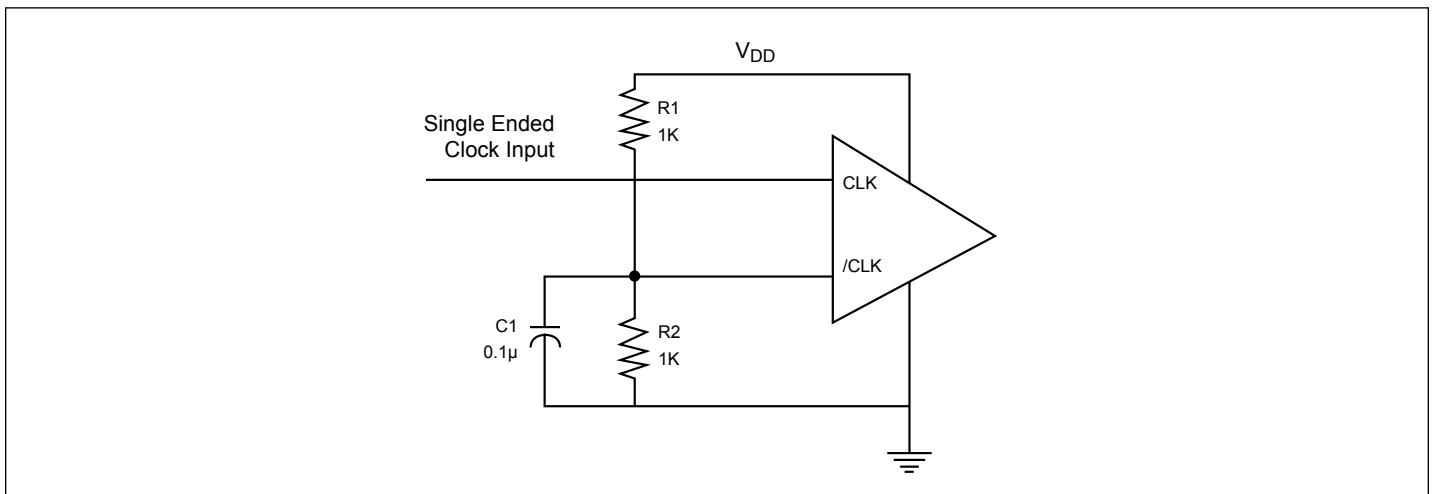
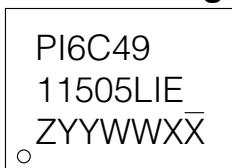


Figure 1. Single-ended Input to Differential Input Device

### Part Marking



Z: Die Rev  
YY: Year  
WW: Workweek  
1st X: Assembly Code  
2nd X: Fab Code

**Packaging Mechanical: 20-TSSOP (L)**

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
C	0.09	–	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
$\theta$	0°	–	8°

**NOTES:**  
 1. ALL DIMENSIONS IN MILLIMETERS. ANGLES IN DEGREES.  
 2. JEDEC MO-153F  
 3. DIMENSIONS DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

		DATE: 03/31/16
DESCRIPTION: 20-Pin, 173mil Wide TSSOP		
PACKAGE CODE: L (L20)		
DOCUMENT CONTROL #: PD-1311	REVISION: G	

16-0074

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

**Ordering Information**

Ordering Code	Package Code	Package Description
PI6C4911505LIEX	L	20-pin, 173mil Wide (TSSOP)

Notes:

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3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. I = Industrial
5. E = Pb-free and Green
6. X suffix = Tape/Reel

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