

MJ11021 (PNP) MJ11022 (NPN)

Complementary Darlington Silicon Power Transistors

Complementary Darlington Silicon Power Transistors are designed for use as general purpose amplifiers, low frequency switching and motor control applications.

Features

- High dc Current Gain @ 10 Adc – $h_{FE} = 400$ Min (All Types)
- Collector–Emitter Sustaining Voltage
 $V_{CEO(sus)} = 250$ Vdc (Min) – MJ11022, 21
- Low Collector–Emitter Saturation
 $V_{CE(sat)} = 1.0$ V (Typ) @ $I_C = 5.0$ A
 $= 1.8$ V (Typ) @ $I_C = 10$ A
- 100% SOA Tested @ $V_{CE} = 44$ V
 $I_C = 4.0$ A
 $t = 250$ ms
- Pb–Free Packages are Available*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|----------------|------------------------------------|--------------------------|
| Collector–Emitter Voltage | V_{CEO} | 250 | Vdc |
| Collector–Base Voltage | V_{CBO} | 250 | Vdc |
| Emitter–Base Voltage | V_{EBO} | 50 | Vdc |
| Collector Current – Continuous – Peak (Note 1) | I_C | 15 30 | Adc |
| Base Current | I_B | 0.5 | Adc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C | P_D | 175 1.16 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -65 to $+175$ -65 to $+200$ | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--------------------------------------|-----------------|------|---------------------------|
| Thermal Resistance, Junction–to–Case | $R_{\theta JC}$ | 0.86 | $^\circ\text{C}/\text{W}$ |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle $\leq 10\%$.

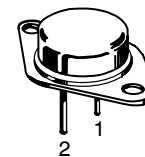
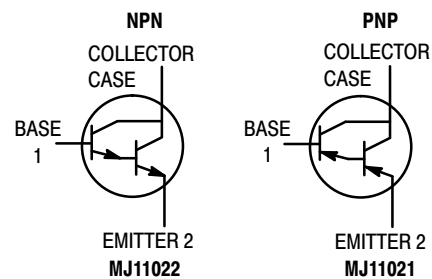
*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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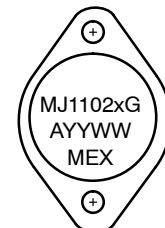
<http://onsemi.com>

15 AMPERE COMPLEMENTARY DARLINGTON POWER TRANSISTORS 250 VOLTS, 175 WATTS



TO–204 (TO–3)
CASE 1–07
STYLE 1

MARKING DIAGRAM



MJ1102x = Device Code
x = 1 or 2
G = Pb–Free Package
A = Location Code
YY = Year
WW = Work Week
MEX = Country of Origin

ORDERING INFORMATION

| Device | Package | Shipping |
|----------|-------------------|----------------|
| MJ11021 | TO–3 | 100 Units/Tray |
| MJ11021G | TO–3 (Pb–Free) | 100 Units/Tray |
| MJ11022 | TO–3 | 100 Units/Tray |
| MJ11022G | TO–3 (Pb–Free) | 100 Units/Tray |

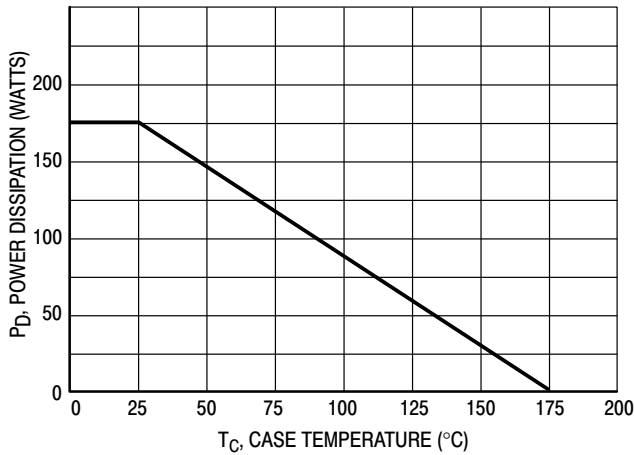
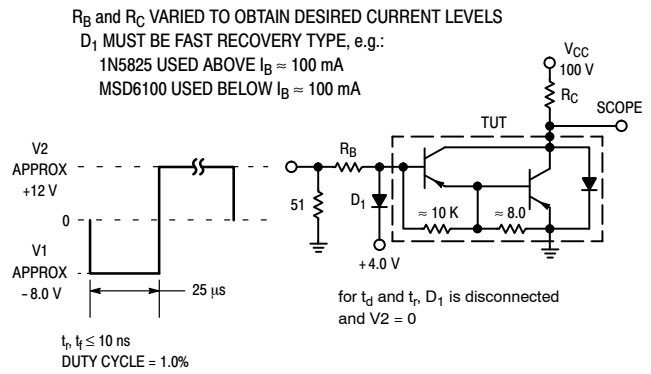


Figure 1. Power Derating



For NPN test circuit reverse diode and voltage polarities.

Figure 2. Switching Times Test Circuit

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|--|----------------|-----|------------|------|
| OFF CHARACTERISTICS | | | | |
| Collector–Emitter Sustaining Voltage (Note 1) ($I_C = 0.1 \text{ Adc}$, $I_B = 0$) | $V_{CEO(sus)}$ | 250 | – | Vdc |
| Collector Cutoff Current ($V_{CE} = 125$, $I_B = 0$) | I_{CEO} | – | 1.0 | mAdc |
| Collector Cutoff Current ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$) ($V_{CE} = \text{Rated } V_{CB}$, $V_{BE(off)} = 1.5 \text{ Vdc}$, $T_J = 150^\circ\text{C}$) | I_{CEV} | – | 0.5 5.0 | mAdc |
| Emitter Cutoff Current ($V_{BE} = 5.0 \text{ Vdc}$, $I_C = 0$) | I_{EBO} | – | 2.0 | mAdc |

ON CHARACTERISTICS (Note 1)

| | | | | |
|--|---------------|------------|-------------|-----|
| DC Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) ($I_C = 15 \text{ Adc}$, $V_{CE} = 5.0 \text{ Vdc}$) | h_{FE} | 400 100 | 15,000 – | – |
| Collector–Emitter Saturation Voltage ($I_C = 10 \text{ Adc}$, $I_B = 100 \text{ mA}$) ($I_C = 15 \text{ Adc}$, $I_B = 150 \text{ mA}$) | $V_{CE(sat)}$ | – | 2.0 3.4 | Vdc |
| Base–Emitter On Voltage $I_C = 10 \text{ A}$, $V_{CE} = 5.0 \text{ Vdc}$ | $V_{BE(on)}$ | – | 2.8 | Vdc |
| Base–Emitter Saturation Voltage ($I_C = 15 \text{ Adc}$, $I_B = 150 \text{ mA}$) | $V_{BE(sat)}$ | – | 3.8 | Vdc |

DYNAMIC CHARACTERISTICS

| | | | | |
|---|------------|-----|------------|-----|
| Current–Gain Bandwidth Product ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ MHz}$) | $[h_{fe}]$ | 3.0 | – | Mhz |
| Output Capacitance ($V_{CB} = 10 \text{ Vdc}$, $I_E = 0$, $f = 0.1 \text{ MHz}$) | C_{ob} | – | 400 600 | pF |
| Small–Signal Current Gain ($I_C = 10 \text{ Adc}$, $V_{CE} = 3.0 \text{ Vdc}$, $f = 1.0 \text{ kHz}$) | h_{fe} | 75 | – | – |

SWITCHING CHARACTERISTICS

| Characteristic | Symbol | Typical | | Unit |
|----------------|--------|---------|-----|---------------|
| | | NPN | PNP | |
| Delay Time | t_d | 150 | 75 | ns |
| Rise Time | t_r | 1.2 | 0.5 | μs |
| Storage Time | t_s | 4.4 | 2.7 | μs |
| Fall Time | t_f | 10.0 | 2.5 | μs |

$(V_{CC} = 100 \text{ V}$, $I_C = 10 \text{ A}$, $I_B = 100 \text{ mA}$
 $V_{BE(off)} = 50 \text{ V}$) (See Figure 2)

1. Pulsed Test: Pulse Width = 300 μs , Duty Cycle $\leq 2\%$.

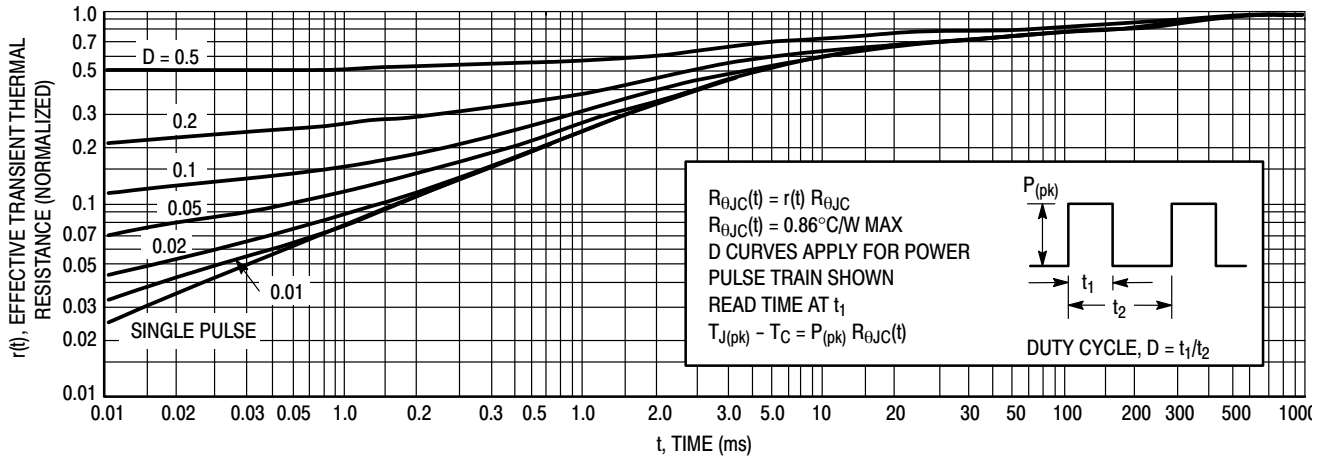


Figure 3. Thermal Response

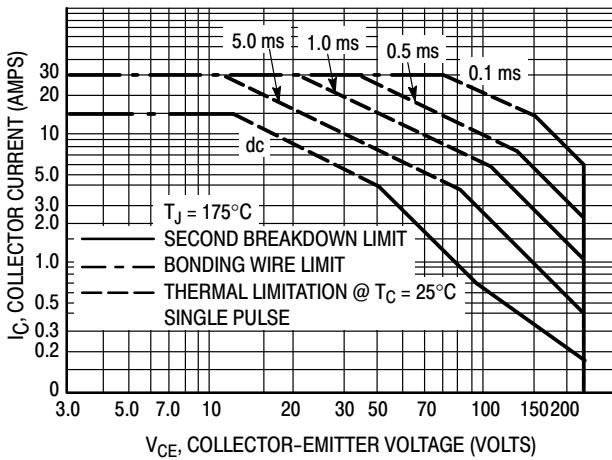


Figure 4. Maximum Rated Forward Bias Safe Operating Area (FBSOA)

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 4 is based on $T_{J(pk)} = 175^\circ\text{C}$, T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 175^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 3. At high case temperatures thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

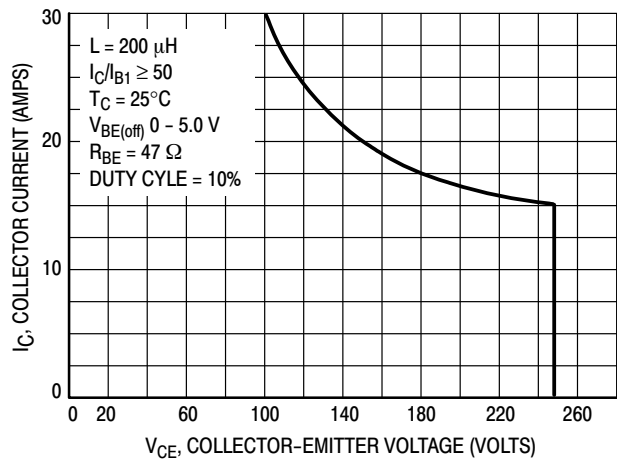


Figure 5. Maximum RBSOA, Reverse Bias Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 5 gives ROSOA characteristics.

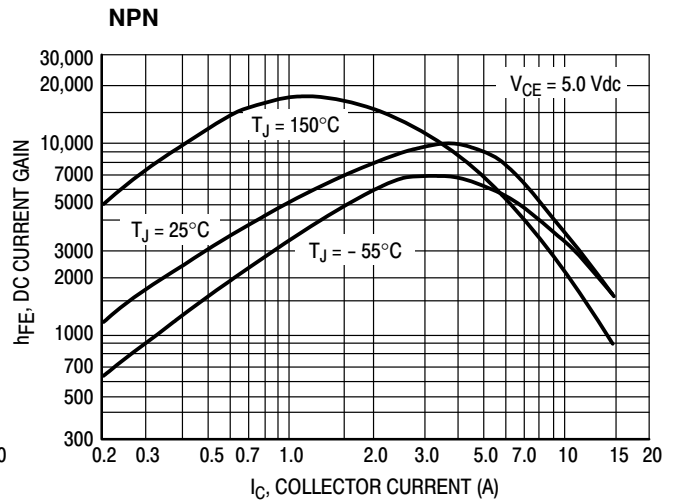
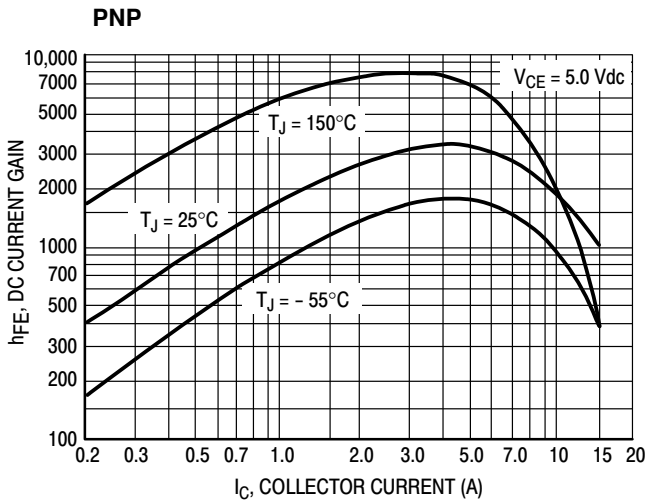


Figure 6. DC Current Gain

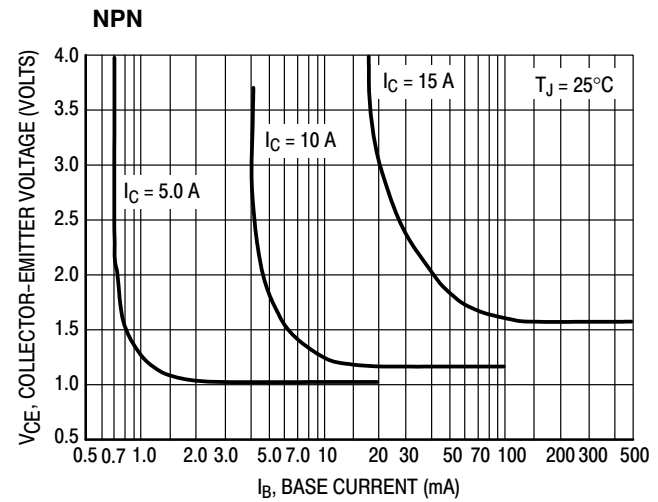
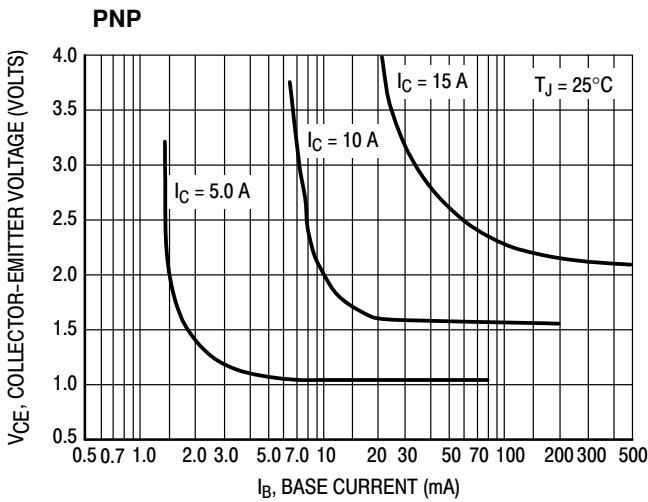


Figure 7. Collector Saturation Region

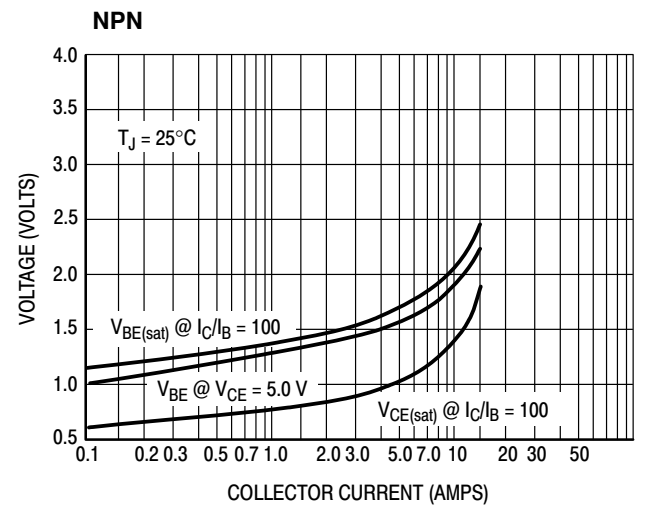
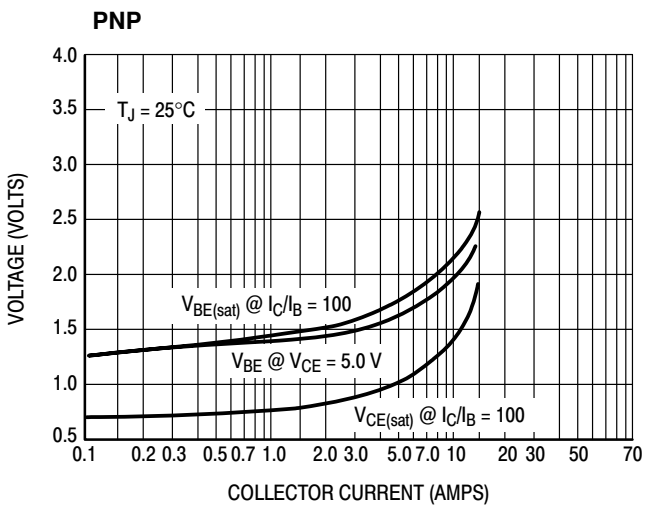


Figure 8. "On" Voltages

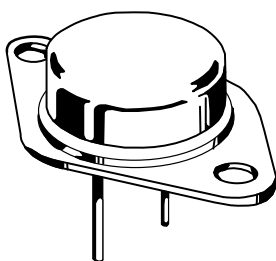
MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

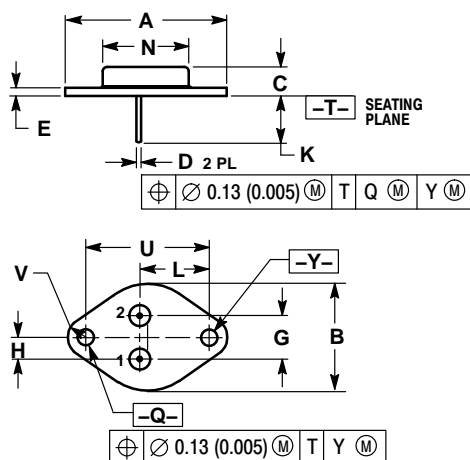


TO-204 (TO-3) CASE 1-07 ISSUE Z

DATE 05/18/1988



SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-----------|-------------|-----------|
| | MIN | MAX | MIN | MAX |
| A | 1.550 REF | --- | 39.37 REF | --- |
| B | --- | 1.050 | --- | 26.67 |
| C | 0.250 | 0.335 | 6.35 | 8.51 |
| D | 0.038 | 0.043 | 0.97 | 1.09 |
| E | 0.055 | 0.070 | 1.40 | 1.77 |
| G | 0.430 BSC | --- | 10.92 BSC | --- |
| H | 0.215 BSC | --- | 5.46 BSC | --- |
| K | 0.440 | 0.480 | 11.18 | 12.19 |
| L | --- | 0.665 BSC | --- | 16.89 BSC |
| N | --- | 0.830 | --- | 21.08 |
| Q | 0.151 | 0.165 | 3.84 | 4.19 |
| U | 1.187 BSC | --- | 30.15 BSC | --- |
| V | 0.131 | 0.188 | 3.33 | 4.77 |

- | | | | | |
|--|--|---|---|---|
| <p>STYLE 1: PIN 1. BASE 2. EMITTER CASE: COLLECTOR</p> | <p>STYLE 2: PIN 1. BASE 2. COLLECTOR CASE: EMITTER</p> | <p>STYLE 3: PIN 1. GATE 2. SOURCE CASE: DRAIN</p> | <p>STYLE 4: PIN 1. GROUND 2. INPUT CASE: OUTPUT</p> | <p>STYLE 5: PIN 1. CATHODE 2. EXTERNAL TRIP/DELAY CASE: ANODE</p> |
| <p>STYLE 6: PIN 1. GATE 2. EMITTER CASE: COLLECTOR</p> | <p>STYLE 7: PIN 1. ANODE 2. OPEN CASE: CATHODE</p> | <p>STYLE 8: PIN 1. CATHODE #1 2. CATHODE #2 CASE: ANODE</p> | <p>STYLE 9: PIN 1. ANODE #1 2. ANODE #2 CASE: CATHODE</p> | |

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