MOTOROLA

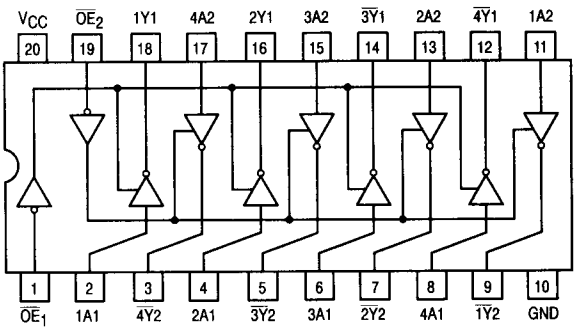
Octal Buffer With Active Low Enable 3-State Inverted Outputs

ELECTRICALLY TESTED PER:
MIL-M-38510/33201

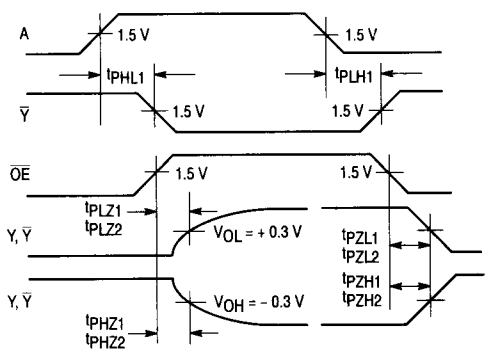
The F240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter/receiver which provides improved PC board density.

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Register
- Outputs Sink 64 mA
- 15 mA Source Current
- Input Clamp Diodes Limit High Speed Termination Effects

LOGIC DIAGRAM



WAVEFORMS



Military 54F240

AVAILABLE AS:

1) JAN: JM38510/33201BXA
2) SMD: N/A
3) 883: 54F240/BXAJC

X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: R
CERFLAT: S
LCC: 2

THE LETTER "M" APPEARS BEFORE THE / ON LCC.

PIN ASSIGNMENTS

FUNCT.	DIL 732-03	FLATS 737-02	LCC 756A-02	BURN-IN (COND. A)
$\overline{OE}_1$	1	1	1	V_{CC}
1A1	2	2	2	V_{CC}
$\overline{4Y}2$	3	3	3	OPEN
2A1	4	4	4	V_{CC}
$\overline{3Y}2$	5	5	5	OPEN
3A1	6	6	6	V_{CC}
$\overline{2Y}2$	7	7	7	OPEN
4A1	8	8	8	V_{CC}
$\overline{1Y}2$	9	9	9	OPEN
GND	10	10	10	GND
1A2	11	11	11	V_{CC}
$\overline{4Y}1$	12	12	12	OPEN
2A2	13	13	13	V_{CC}
$\overline{3Y}1$	14	14	14	OPEN
3A2	15	15	15	V_{CC}
2Y1	16	16	16	OPEN
4A2	17	17	17	V_{CC}
1Y1	18	18	18	OPEN
$\overline{OE}_2$	19	19	19	V_{CC}
V_{CC}	20	20	20	V_{CC}

BURN-IN CONDITIONS:
V_{CC} = 5.0 V MIN/6.0 V MAX

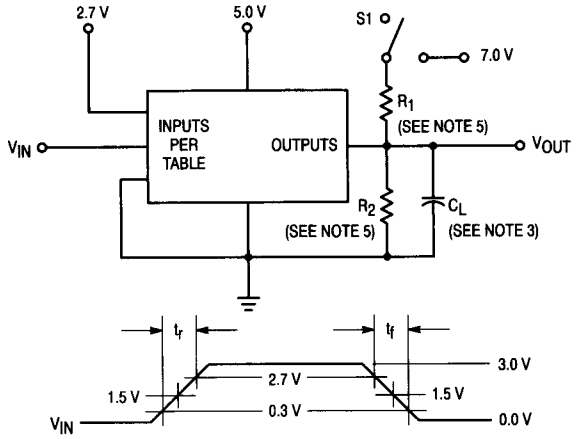
TRUTH TABLE

Inputs		Output
$\overline{OE}_1$, $\overline{OE}_2$	D	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level X = Immaterial
L = LOW Voltage Level Z = HIGH Impedance

4

AC TEST CIRCUIT



Test Type	S1
t_{PLH}	open
t_{PHL}	open
t_{PHZ}	open
t_{PZH}	open
t_{PLZ}	closed
t_{PZL}	closed

REFERENCE NOTES ON PAGE 4-105

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Static Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V_{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V_{CC} = 4.5 V, I_{OH} = −3.0 mA, V_{IL} = 0.8 V (all inputs).
V_{OL}	Logical "0" Output Voltage		0.55		0.55		0.55	V	V_{CC} = 4.5 V, I_{OL} = 48 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V.
V_{IC}	Input Clamping Voltage		−1.2					V	V_{CC} = 4.5 V, I_{IN} = −18 mA, other inputs are open.
I_{IH}	Logical "1" Input Current		20		20		20	µA	V_{CC} = 5.5 V, V_{IH} = 2.7 V, other inputs are open.
I_{IHH}	Logical "1" Input Current		100		100		100	µA	V_{CC} = 5.5 V, V_{IHH} = 7.0 V, other inputs are open.
I_{OD}	Dioue Current	65		65		65		mA	V_{CC} = 4.5 V, V_{IN} = GND, other input = 5.5 V, V_{OUT} = 2.5 V.
I_{IL}	Logical "0" Input Current	−0.03	−1.0	−0.03	−1.0	−0.03	−1.0	mA	V_{CC} = 5.5 V, V_{IN} = 0.5 V, other inputs are open.
I_{OS}	Output Short Circuit Current	−100	−325	−100	−325	−100	−325	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{IOZH}	Output Off Current High		50		50		50	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other input = 4.5 V, V_{OUT} = 2.4 V.
I_{IOZL}	Output Off Current Low		−50		−50		−50	µA	V_{CC} = 5.5 V, V_{IN} = 2.0 V, other input = 0 V, V_{OUT} = 0.5 V.
I_{CCH}	Power Supply Current		35		35		35	mA	V_{CC} = 5.5 V, V_{IN} = 0 V (all inputs).
I_{CCL}	Power Supply Current		75		75		75	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, other input = 0 V.
I_{CCZ}	Power Supply Current Off		75		75		75	mA	V_{CC} = 5.5 V, V_{IN} = 4.5 V, OE_2 = 4.5 V, other input is open.
V_{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V_{CC} = 4.5 V.
V_{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V_{CC} = 4.5 V.

Symbol	Parameter	Limits			Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C	+ 125°C	− 55°C		
	Functional Tests	Subgroup 7	Subgroup 8A	Subgroup 8B		
						per Truth Table with V_{CC} = (See Note 6), V_{INL} = 0.55 V, V_{INH} = 2.4 V.

Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
	Switching Parameters:	+ 25°C		+ 125°C		− 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t_{PHL1}	Propagation Delay /Data-Output Output High-Low	1.0	4.7	1.0	6.0	1.0	6.0	ns	V_{CC} = (See Note 6), C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLH1}	Propagation Delay /Data-Output Output Low-High	1.0	7.0	1.0	9.0	1.0	9.0	ns	V_{CC} = (See Note 6), C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PLZ1}	Propagation Delay /Data-Output Output Low-High	2.0	10	2.0	12.5	2.0	12.5	ns	V_{CC} = (See Note 6), C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PHZ1}	Propagation Delay /Data-Output Output High-Low	2.0	6.0	2.0	6.5	2.0	6.5	ns	V_{CC} = (See Note 6), C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZL1}	Propagation Delay /Data-Output Output Low-High	2.0	9.0	2.0	10.5	2.0	10.5	ns	V_{CC} = (See Note 6), C_L = 50 pF, $R_1 = R_2$ = 500 Ω.
t_{PZH1}	Propagation Delay /Data-Output Output High-Low	2.0	6.0	2.0	6.5	2.0	6.5	ns	V_{CC} = (See Note 6), C_L = 50 pF, $R_1 = R_2$ = 500 Ω.

NOTES:
1. Pulse generator has the following characteristics: $t_r = t_f \leq 2.5$ ns, PRR ≤ 1.0 MHz and $Z_{OUT} \approx 50$ Ω.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. C_L = 50 pF ± 10% including scope probe, wiring and stray capacitance, without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_1 = R_2$ = 500 Ω ± 5.0%.
6. Perform functional tests at V_{CC} = 4.5 V **(repeat at)** V_{CC} = 5.0 V, and V_{CC} = 5.5 V (Motorola imposed).