National Semiconductor

MICROCIRCUIT DATA SHEET

MNDM54LS109-X REV 1A0

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DUAL J$\overline{K}$ POSITIVE EDGE-TRIGGERED FLIP-FLOP

General Description

The 'LS109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to 'LS74 data sheet) by connecting the J and K inputs.

Industry Part Number

54LS109

NS Part Numbers

DM54LS109J/883
DM54LS109W/883

Prime Die

L109

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{o}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- Low input to $\overline{S}D$ sets Q to High level
- Low input to $\overline{C}D$ sets Q to Low Level
- Clear and set are independent of clock
- Simultaneous Low on $\overline{C}D$ and $\overline{S}D$ makes both Q and $\overline{Q}$ HIGH

(Absolute Maximum Ratings)

(Note 1)

Storage Temperature	-65 C to +150 C
Ambient Temperature under Bias	-55 C to +125 C
Input Voltage	-0.5V to +5.5V
VCC Pin Potential to Ground Pin	-0.5V to +7.0V
Junction Temperature under Bias	-55 C to +175 C
Current Applied to Output in LOW state (Max)	twice the rated Iol (ma)

Note 1: Absolute Maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55 C to +125 C
Supply Voltage	
Military	+4.5V to +5.5V

Electrical Characteristics

DC PARAMETER

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: VCC 4.5V to 5.5V, Temp range: -55C to 125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH (1)	Input High Current	VCC=5.5V, VM=2.7V, VINL=0.0V, VINH=4.5V	1, 3	Jn/$\overline{K}$n		20.0	uA	1, 2, 3
IIH (2)	Input High Current	VCC=5.5V, VM=2.7V, VINL=0.0V, VINH=4.5V	1, 3	CPn/$\overline{S}$Dn		40.0	uA	1, 2, 3
IIH (4)	Input High Current	VCC=5.5V, VM=2.7V, VINL=0.0V, VINH=4.5V	1, 3	$\overline{C}$Dn		80.0	uA	1, 2, 3
IBVI (1)	Input High Current	VCC=5.5V, VM=5.5V, VINH=4.5V, VINL=0.0V	1, 3	Jn/$\overline{K}$n		100	uA	1, 2, 3
IBVI (2)	Input High Current	VCC=5.5V, VM=5.5V, VINH=4.5V, VINL=0.0V	1, 3	CPn/$\overline{S}$Dn		200	uA	1, 2, 3
IBVI (4)	Input High Current	VCC=5.5V, VM=5.5V, VINH=4.5V, VINL=0.0V	1, 3	$\overline{C}$Dn		400	uA	1, 2, 3
IIL (1)	Input LOW Current	VCC=5.5V, VM=0.4V, VINL=0.0V, VINH=4.5V	1, 3	Jn/$\overline{K}$n	-0.03	-0.4	mA	1, 2, 3
IIL (2)	Input LOW Current	VCC=5.5V, VM=0.4V, VINH=4.5V, VINL=0.0V	1, 3	CPn/$\overline{S}$Dn	-0.06	-0.8	mA	1, 2, 3
IIL (4)	Input LOW Current	VCC=5.5V, VM=0.4V, VINL=0.0V, VINH=4.5V	1, 3	$\overline{C}$Dn	-.12	-1.6	mA	1, 2, 3
VOL	Output LOW Voltage	VCC=4.5V, VIH=2.0V, IOL=4.0mA, VINH=4.5V, VIL=0.7V	1, 3	OUTPUTS		0.4	V	1, 2, 3
VOH	High Level Output Voltage	VCC=4.5V, VIH=2.0V, IOH=-0.4mA, VINH=4.5V	1, 3	OUTPUTS	2.5		V	1, 2, 3
IOS	Short Circuit Output Current	VCC=5.5V, VINH=4.5V, VOUT=0.0V, VINL=0.0V	1, 3	OUTPUT	-20.0	-100	mA	1, 2, 3
VCD	Input Clamp Diode Voltage	VCC=4.5V, IM=-18mA, VINH=4.5V	1, 3	INPUTS		-1.5	V	1, 2, 3
ICC	Supply Current	VCC=5.5V, VINL=0.0V, VINH=4.5V	1, 3	VCC		8.0	mA	1, 2, 3

Electrical Characteristics

AC PARAMETER - 15pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=15pF, RL=2k ohms Temp range: +25C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH (1)	Propagation Delay	VCC=5.0V	5	CPn to Qn/$\overline{Qn}$		25.0	ns	9
tpHL (1)	Propagation Delay	VCC=5.0V	5	CPn to Qn/$\overline{Qn}$		35.0	ns	9
tpLH (2)	Propagation Delay	VCC=5.0V Clock High	5	$\overline{CDn}$/$\overline{SDn}$ to Q/		15.0	ns	9
tpHL (2)	Propagation Delay	VCC=5.0V Clock High	5	$\overline{CDn}$/$\overline{SDn}$ to Q/		35.0	ns	9
tpLH (3)	Propagation Delay	VCC=5.0V Clock Low	5	$\overline{CDn}$/$\overline{SDn}$ to Q/		15.0	ns	9
tpHL (3)	Propagation Delay	VCC=5.0V Clock Low	5	$\overline{CDn}$/$\overline{SDn}$ to Q/		24.0	ns	9
tS (H)	Setup Time	VCC=5.0V	5	Jn/$\overline{Kn}$ to CPn	20.0		ns	9
tS (L)	Setup Time	VCC=5.0V	5	Jn/$\overline{Kn}$ to CPn	18.0		ns	9
tH (H/L)	Hold Time	VCC=5.0V	5	Jn/$\overline{Kn}$ to CPn	0.0		ns	9
tW (H/L)	Pulse Width	VCC=5.0V	5	CPn	16.5		ns	9
tW (L)	Pulse Width	VCC=5.0V	5	$\overline{CDn}$ or $\overline{SDn}$	20.0		ns	9
fMAX	Maximum Clock Frequency	VCC=5.0V	5		30.0		MHZ	9

Electrical Characteristics

AC PARAMETER - 50pF

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: CL=50pF, RL=2K ohms Temp range: -55C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tpLH (1)	Propagation Delay	VCC=5.0V	2, 4	CPn to Qn/$\overline{Qn}$	2.0	25.0	ns	9
			2, 4	CPn to Qn/$\overline{Qn}$	2.0	39.0	ns	10, 11
tpHL (1)	Propagation Delay	VCC=5.0V	2, 4	CPn to Qn/$\overline{Qn}$	2.0	35.0	ns	9
			2, 4	CPn to Qn/$\overline{Qn}$	2.0	59.0	ns	10, 11
tpLH (2)	Propagation Delay	VCC=5.0V Clock High	2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	20.0	ns	9
			2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	39.0	ns	10, 11
tpHL (2)	Propagation Delay	VCC=5.0V Clock High	2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	35.0	ns	9
			2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	59.0	ns	10, 11
tpLH (3)	Propagation Delay	VCC=5.0V Clock Low	2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	20.0	ns	9
			2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	39.0	ns	10, 11
tpHL (3)	Propagation Delay	VCC=5.0V Clock Low	2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	32.0	ns	9
			2, 4	$\overline{CDn}$/$\overline{SDn}$ to Q/	2.0	59.0	ns	10, 11
ts (H/L)	Setup Time	VCC=5.0V	2, 4	Jn or $\overline{Kn}$ to CPn	25.0		ns	9, 10, 11
th (H/L)	Hold Time	VCC=5.0V	2, 4	Jn or $\overline{Kn}$ to CPn	5.0		ns	9, 10, 11
tw (H/L)	Pulse Width	VCC=5.0V	2, 4	CPn	25.0		ns	9, 10, 11
tw (L)	Pulse Width	VCC=5.0V	2, 4	$\overline{CDn}$ or $\overline{SDn}$	30.0		ns	9, 10, 11
fMAX	Clock Frequency	VCC=5.5V	2, 4		20.0		MHZ	9, 10, 11

Note 1: Screen tested 100% on each device at -55C, +25C & +125C temperature, subgroups A1, 2, 3, 7 & 8.
Note 2: Screen tested 100% on each device at +25C temperature only, subgroup A9.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, +125C & -55C temperature, subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25C, subgroup A9. Subgroups 10 & 11 are guaranteed, not tested.
Note 5: Guaranteed, not tested.

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1A0	M0002951	09/14/98	Donald B. Miller	Archive: Table 1, 54LS109 rev C1.2. Initial MDS release: MNDM54LS109-X rev 1A0. Changed note 5 (guaranteed, not tested) in the AC 50pF notes reference column to note 2 (screen tested 100% at +25C, subgroup 9) & to note 4 (Subgroups 10 & 11 are guaranteed, not tested). Changed note 2 in the AC 15pF notes reference column to note 5. Re-worded the phrase in note 4 from "and periodically at +125C and -55C, subgroups 10 & 11" to "Subgroups 10 & 11 are guaranteed, not tested.