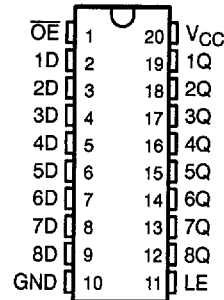


SN74LVC573 OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

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- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Typical V_{OLP} (Output Ground Bounce) $< 0.8\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot) $> 2\text{ V}$ at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**DB, DW, OR PW PACKAGE
(TOP VIEW)**



description

This octal transparent D-type latch is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LVC573 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When the latch enable is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LVC573 is characterized for operation from -40°C to 85°C .

**FUNCTION TABLE
(each latch)**

| INPUTS | | | OUTPUT |
|-----------------|----|---|--------|
| \overline{OE} | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | Q_0 |
| H | X | X | Z |

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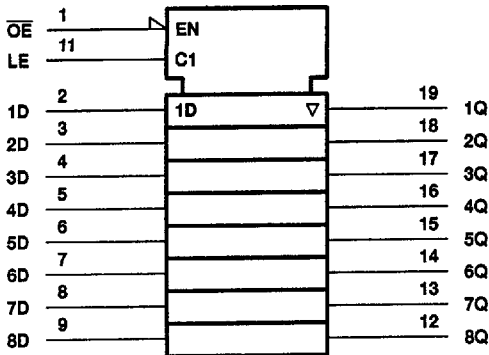
PRODUCT PREVIEW

SN74LVC573

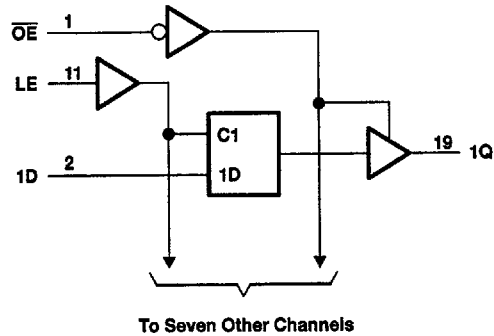
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logic symbol



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | | |
|-----------------------------------------------------------------------|-------|----------------------------|
| Supply voltage range, V_{CC} | | -0.5 V to 4.6 V |
| Input voltage range, V_I | | -0.5 V to 4.6 V |
| Output voltage range, V_O (see Note 1) | | -0.5 V to $V_{CC} + 0.5$ V |
| Input clamp current, I_{IK} ($V_I < 0$) | | -50 mA |
| Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) | | ±50 mA |
| Continuous output current, I_O ($V_O = 0$ to V_{CC}) | | ±50 mA |
| Continuous current through V_{CC} or GND | | ±100 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air): | | |
| DB package | | 0.6 W |
| DW package | | 1.6 W |
| PW package | | 0.7 W |
| Storage temperature range | | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 2)

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|---------------------------|----------|------|
| V_{CC} | Supply voltage | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | $V_{CC} = 2.7$ V to 3.6 V | | V |
| V_{IL} | Low-level input voltage | $V_{CC} = 2.7$ V to 3.6 V | | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| V_O | Output voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | $V_{CC} = 2.7$ V | -12 | mA |
| | | $V_{CC} = 3$ V | -24 | |
| I_{OL} | Low-level output current | $V_{CC} = 2.7$ V | 12 | mA |
| | | $V_{CC} = 3$ V | 24 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | 10 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 2: Unused or floating inputs must be held high or low.

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SN74LVC573
OCTAL TRANSPARENT D-TYPE LATCH
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} † | T _A = -40°C to 85°C | | UNIT |
|------------------|--------------------------------------------------------------------------------------------------------------|-------------------|--------------------------------|-----|------|
| | | | MIN | MAX | |
| V _{OH} | I _{OH} = -100 μA | MIN to MAX | V _{CC} -0.2 | | V |
| | I _{OH} = -12 mA | 2.7 V | 2.2 | | |
| | I _{OH} = -24 mA | 3 V | 2.4 | | |
| V _{OL} | I _{OL} = 100 μA | MIN to MAX | 0.2 | | V |
| | I _{OL} = 12 mA | 2.7 V | 0.4 | | |
| | I _{OL} = 24 mA | 3 V | 0.55 | | |
| I _I | V _I = V _{CC} or GND | 3.6 V | ±5 | | μA |
| I _{OZ} | V _O = V _{CC} or GND | 3.6 V | ±10 | | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6 V | 20 | | μA |
| ΔI _{CC} | V _{CC} = 3 V to 3.6 V, One input at V _{CC} - 0.6 V, Other inputs at V _{CC} or GND | | 500 | | μA |
| C _i | V _I = V _{CC} or GND | 3.3 V | | | pF |
| C _o | V _O = V _{CC} or GND | 3.3 V | | | pF |

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

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