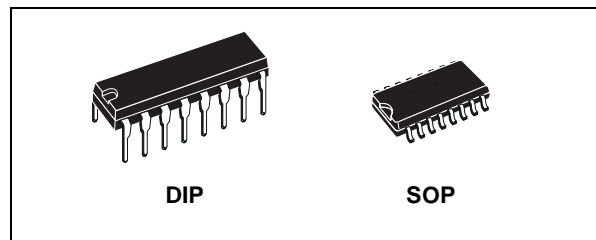




# HCF4052B

## DIFFERENT 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

- LOW "ON" RESISTANCE : 125Ω (Typ.) OVER 15V p.p SIGNAL-INPUT RANGE FOR  $V_{DD} - V_{EE} = 15V$
- HIGH "OFF" RESISTANCE : CHANNEL LEAKAGE  $\pm 100pA$  (Typ.) at  $V_{DD} - V_{EE} = 18V$
- BINARY ADDRESS DECODING ON CHIP
- HIGH DEGREE OF LINEARITY :  $< 0.5\%$  DISTORTION TYP. at  $f_{IS} = 1KHz$ ,  $V_{IS} = 5 V_{pp}$ ,  $V_{DD} - V_{SS} \geq 10V$ ,  $R_L = 10K\Omega$
- VERY LOW QUIESCENT POWER DISSIPATION UNDER ALL DIGITAL CONTROL INPUT AND SUPPLY CONDITIONS :  $0.2 \mu W$  (Typ.) at  $V_{DD} - V_{SS} = V_{DD} - V_{EE} = 10V$
- MATCHED SWITCH CHARACTERISTICS :  $R_{ON} = 5\Omega$  (Typ.) FOR  $V_{DD} - V_{EE} = 15V$
- WIDE RANGE OF DIGITAL AND ANALOG SIGNAL LEVELS : DIGITAL 3 to 20, ANALOG TO 20V p.p.
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  $I_l = 100nA$  (MAX) AT  $V_{DD} = 18V$   $T_A = 25^\circ C$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B " STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



### ORDER CODES

PACKAGE	TUBE	T & R
DIP	HCF4052BEY	
SOP	HCF4052BM1	HCF4052M013TR

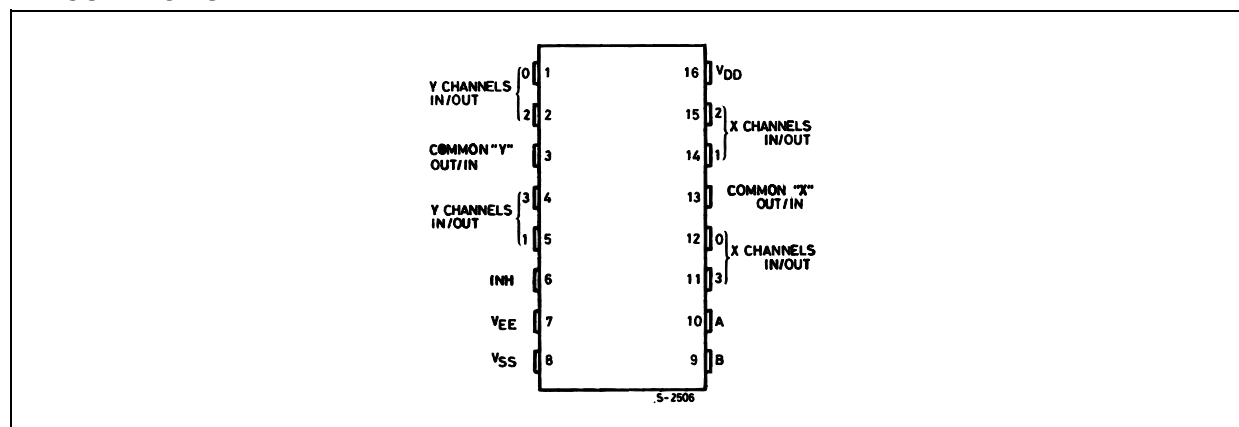
technology available in DIP and SOP packages. The HCF4052B analog multiplexer/demultiplexer is a digitally controlled analog switch having low ON impedance and very low OFF leakage current. This multiplexer circuit dissipate extremely low quiescent power over the full  $V_{DD} - V_{SS}$  and  $V_{DD} - V_{EE}$  supply voltage range, independent of the logic state of the control signals.

When a logic "1" is present at the inhibit input terminal all channel are off. This device is a differential 4-channel multiplexer having two binary control inputs, A and B and an inhibit input. The two binary input signals selects 1 of 4 pairs of channels to be turned on and connect the analog inputs to the outputs.

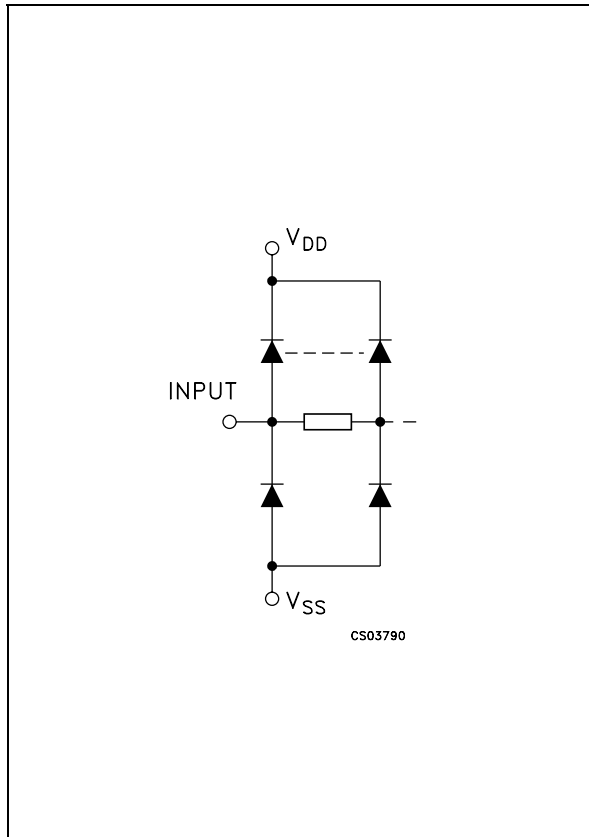
### DESCRIPTION

The HCF4052B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor

### PIN CONNECTION



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

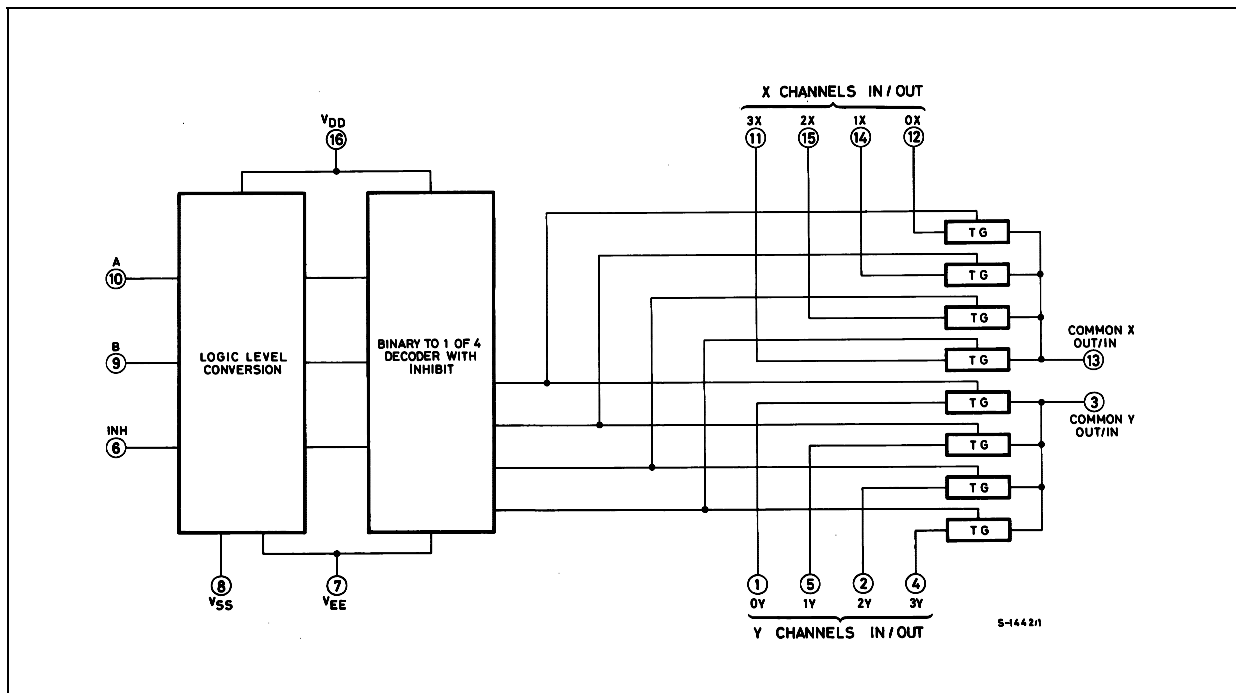
PIN No	SYMBOL	NAME AND FUNCTION
10, 9	A, B	Binary Control Inputs
6	INH	Inhibit Inputs
12, 14, 15, 11	0X to 3X CHANNEL IN/OUT	X channels Input/Output
1, 5, 2, 4	0Y to 3Y CHANNEL IN/OUT	Y channels Input/Output
3	COM Y OUT/IN	Y Common Output/Input
13	COM X OUT/IN	X Common Output/Input
7	$V_{EE}$	Supply Voltage
8	$V_{SS}$	Negative Supply Voltage
16	$V_{DD}$	Positive Supply Voltage

TRUTH TABLE

INHIBIT	B	A	
0	0	0	0x, 0y
0	0	1	1x, 1y
0	1	0	2x, 2y
0	1	1	3x, 3y
1	X	X	NONE

X : Don't Care

FUNCTIONAL DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to $V_{DD} + 0.5$	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	500 (*)	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	°C
$T_{stg}$	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to  $V_{SS}$  pin voltage.

(\*) 500mW at 65 °C; derate to 300mW by 10mW/°C from 65°C to 85°C

**RECOMMENDED OPERATING CONDITIONS**


Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	0 to $V_{DD}$	V
$T_{op}$	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>SS</sub> (V)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Device Current (all switches ON or all switches OFF)				5		0.04	5		150		150	μA
					10		0.04	10		300		300	
					15		0.04	20		600		600	
					20		0.08	100		3000		3000	
<b>SWITCH</b>													
R <sub>ON</sub>	Resistance	0 ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	0	0	5		470	1050		1200		1200	Ω
					10		180	400		520		520	
					15		125	280		360		360	
Δ <sub>ON</sub>	Resistance Δ <sub>RON</sub> (between any 2 of 4 switches)	0 ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	0	0	5		10						Ω
					10		10						
					15		5						
OFF*	Channel Leakage Current (All Channel OFF) (COMMON O/I)		0	0	18		±0.1	100		1000		1000	nA
OFF*	Channel Leakage Current (Any Channel OFF)		0	0	18		±0.1	100		1000		1000	nA
C <sub>I</sub>	Input Capacitance		-5	-5	5		5						pF
C <sub>O</sub>	Output Capacitance					18							
C <sub>IO</sub>	Feed through					0.2							
<b>CONTROL (Address or Inhibit)</b>													
V <sub>IL</sub>	Input Low Voltage	= V <sub>DD</sub> thru 1KΩ	V <sub>EE</sub> = V <sub>SS</sub> R <sub>L</sub> = 1KΩ to V <sub>SS</sub> I <sub>IS</sub> < 2μA (on all OFF channels)	5			1.5		1.5		1.5	V	
				10			3		3		3		
				15			4		4		4		
V <sub>IH</sub>	Input High Voltage	= V <sub>DD</sub> thru 1KΩ	V <sub>EE</sub> = V <sub>SS</sub> R <sub>L</sub> = 1KΩ to V <sub>SS</sub> I <sub>IS</sub> < 2μA (on all OFF channels)	5	3.5		3.5		3.5		3.5	V	
				10	7		7		7		7		
				15	11		11		11		11		
I <sub>IH</sub> , I <sub>IL</sub>	Input Leakage Current		V <sub>I</sub> = 0/18V		18		±10 <sup>-3</sup>	±0.1		±1		±1	μA
C <sub>I</sub>	Input Capacitance						5	7.5					pF

\* Determined by minimum feasible leakage measurement for automating testing.

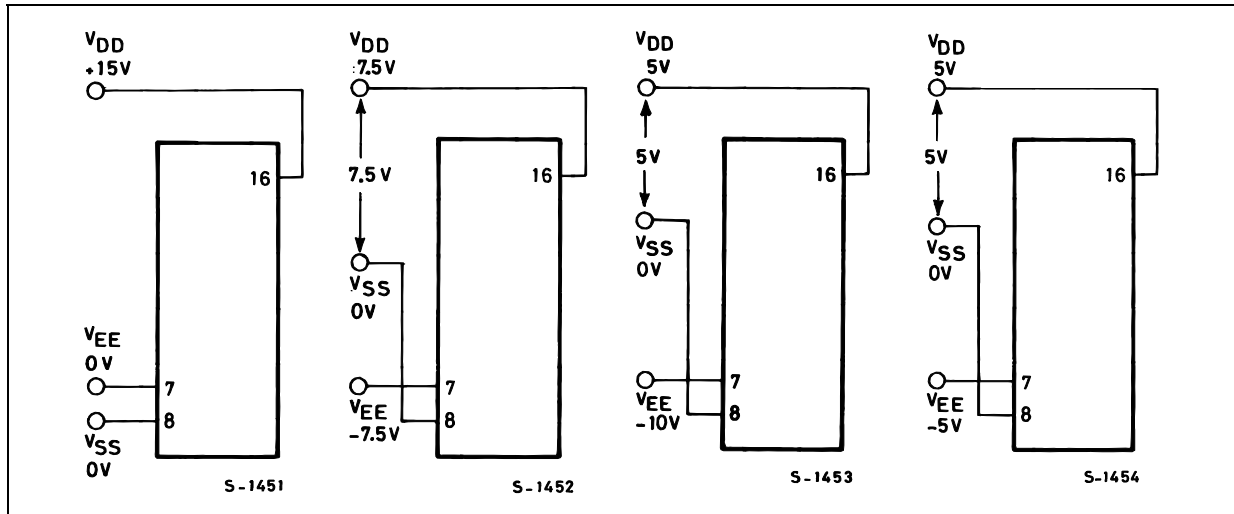
**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ , all input square wave rise and fall time = 20 ns )

Parameter	Test Condition							Value			Unit	
	$V_{EE}$ (V)	$R_L$ (K $\Omega$ )	$f_I$ (KHz)	$V_I$ (V)	$V_{SS}$ (V)	$V_{DD}$ (V)		Min.	Typ.	Max.		
Propagation Delay Time (signal input to output)		200		$V_{DD}$ 		5			30	60	ns	
						10			15	30		
						15			11	20		
Frequency Response Channel "ON" (sine wave input) at $20 \log V_O/V_I = -3\text{dB}$	$= V_{SS}$	1		5(*)		10	$V_O$ at Common OUT/IN		25		MHz	
							$V_O$ at any channel		60			
Feed through (all channels OFF) at $20 \log V_O/V_I = -40\text{dB}$	$= V_{SS}$	1		5(*)		10	$V_O$ at Common OUT/IN		10		MHz	
							$V_O$ at any channel		8			
Frequency Signal Crosstalk at $20 \log V_O/V_I = -40\text{dB}$	$= V_{SS}$	1		5(*)		10	Between Sections (measured on common)		6		MHz	
							Between Sections (measured on any channel)		10			
Sine Wave Distortion $f_{IS} = 1\text{KHz}$ Sine Wave	$= V_{SS}$	10	1	2(*)		5			0.3		%	
				3(*)		10			0.2			
				5(*)		15			0.12			
<b>CONTROL (Address or Inhibit)</b>												
Propagation Delay: Address to Signal OUT (Channels ON or OFF)	0					0	5			360	720	ns
	0					0	10			160	320	
	0					0	15			120	240	
	-5					0	5			225	450	
Propagation Delay: Inhibit to Signal OUT (Channel turning ON)	0	1				0	5			360	720	ns
	0					0	10			160	320	
	0					0	15			120	240	
	-10					0	5			200	400	
Propagation Delay: Inhibit to Signal OUT (Channel turning OFF)	0	10					5			200	450	ns
	0						10			90	210	
	0						15			70	160	
	-10						5			130	300	
Address or Inhibit to Signal Crosstalk	0	10 <sup>(1)</sup>			0	10	$V_C = V_{DD} - V_{SS}$ (square wave)		65		mV peak	

(1) Both ends of channel.

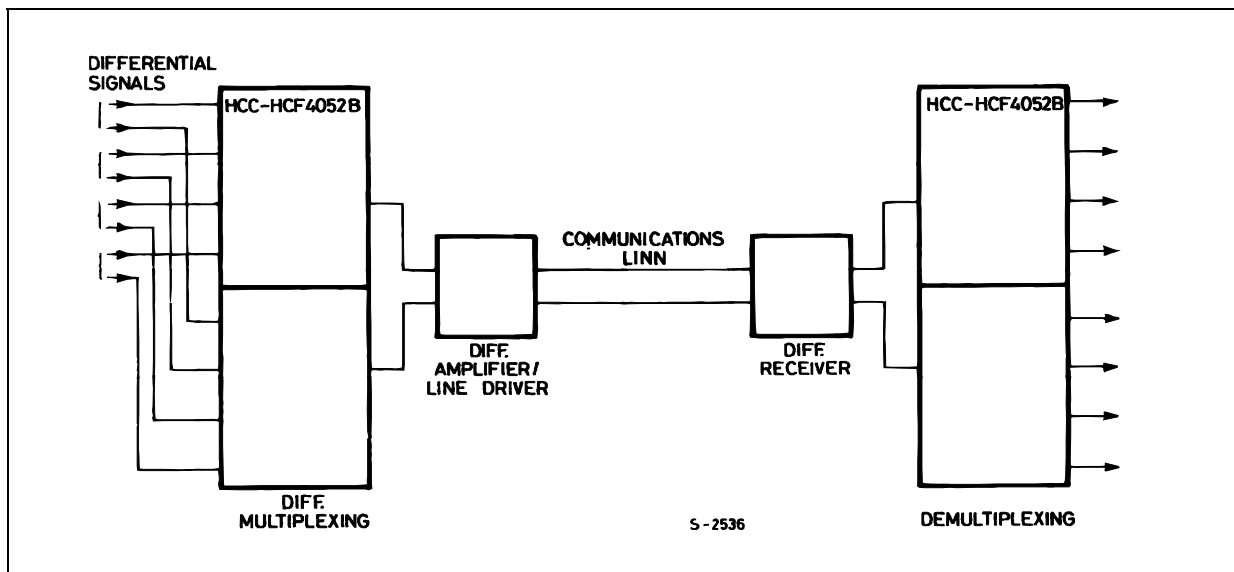
\* Peak to Peak voltage symmetrical about  $(V_{DD} - V_{EE}) / 2$

TYPICAL BIAS VOLTAGES



The ADDRESS (digital-control inputs) and INHIBIT logic levels are : "0"= $V_{SS}$  and "1"= $V_{DD}$ . The analog signal (through the TG) may swing from  $V_{EE}$  to  $V_{DD}$

TYPICAL APPLICATIONS (TYPICAL TIME-DIVISION APPLICATION)

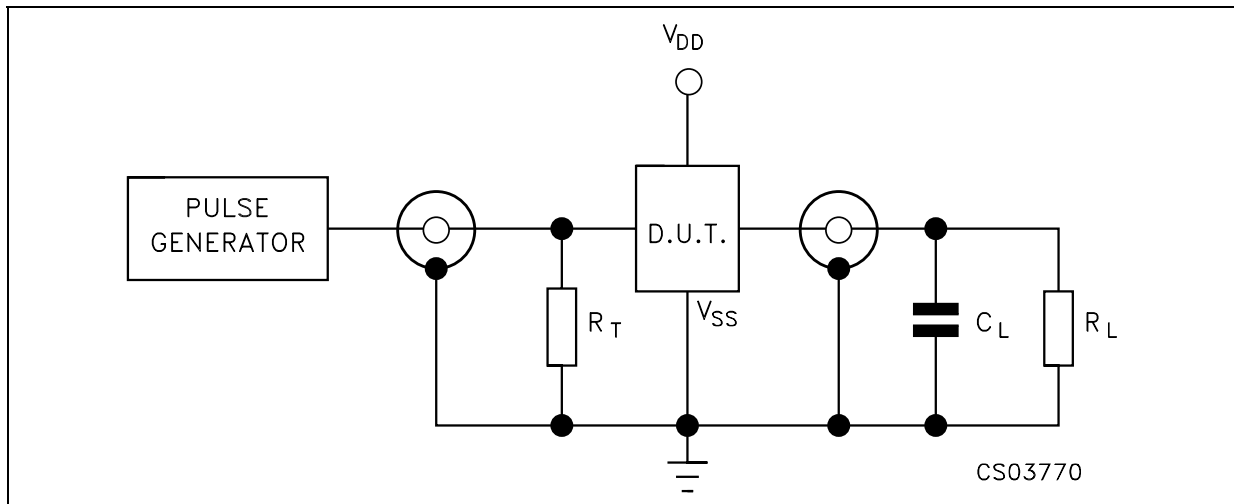


SPECIAL CONSIDERATIONS

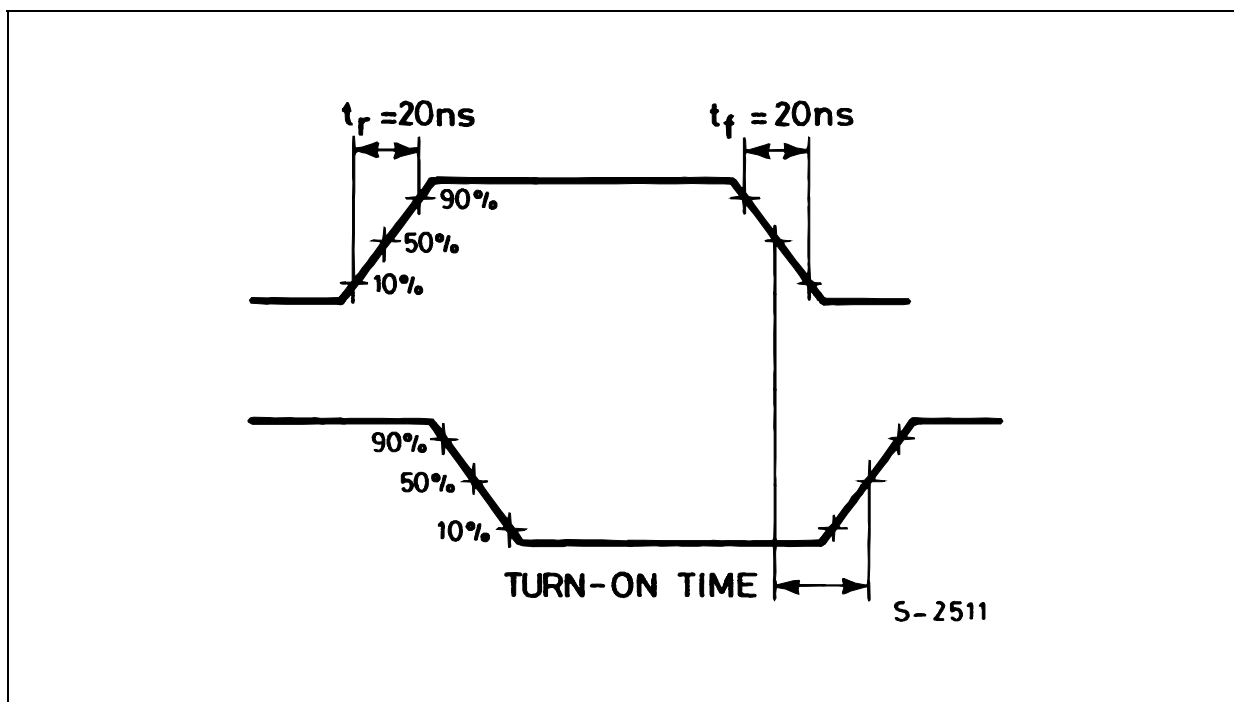
Control of analog signals up to 20V peak to peak can be achieved by digital signal amplitudes of 4.5 to 20V (if  $V_{DD} - V_{SS} = 3V$ , a  $V_{DD} - V_{EE}$  of up to 13V can be controlled; for  $V_{DD} - V_{EE}$  level differences above 13V, a  $V_{DD} - V_{SS}$  of at least 4.5V is required. For example, if  $V_{DD} = +5$ ,  $V_{SS} = 0$ , and  $V_{EE} = -13.5$ , analog signals from -13.5V to 4.5V can be controlled by digital inputs of 0 to 4.5V. In certain applications, the external load resistor

current may include both  $V_{DD}$  and signal-line components. To avoid drawing  $V_{DD}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.8V (calculated from  $R_{ON}$  values shown in DC SPECIFICATIONS). No  $V_{DD}$  current will flow through  $R_L$  if the switch current flows into leads 3 and 13.

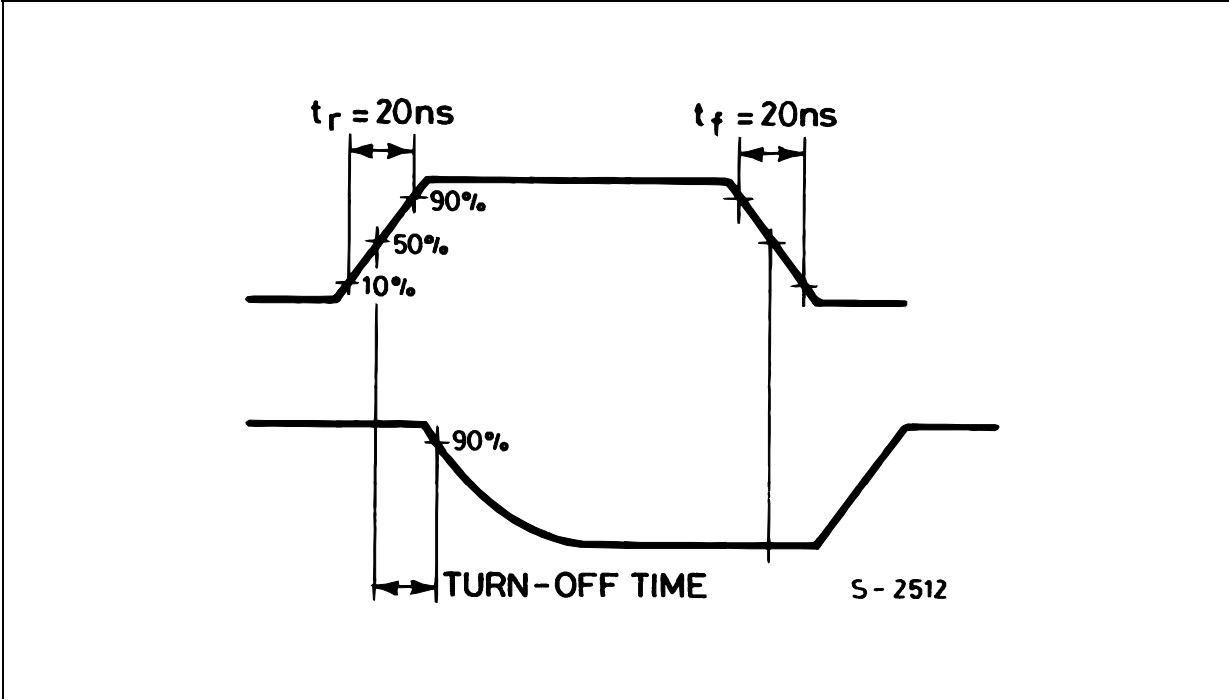
## TEST CIRCUIT



$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{K}\Omega$   
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**WAVEFORM 1 : CHANNEL BEING TURNED ON** ( $R_L = 1\text{K}\Omega$ ,  $f = 1\text{MHz}$ ; 50% duty cycle)


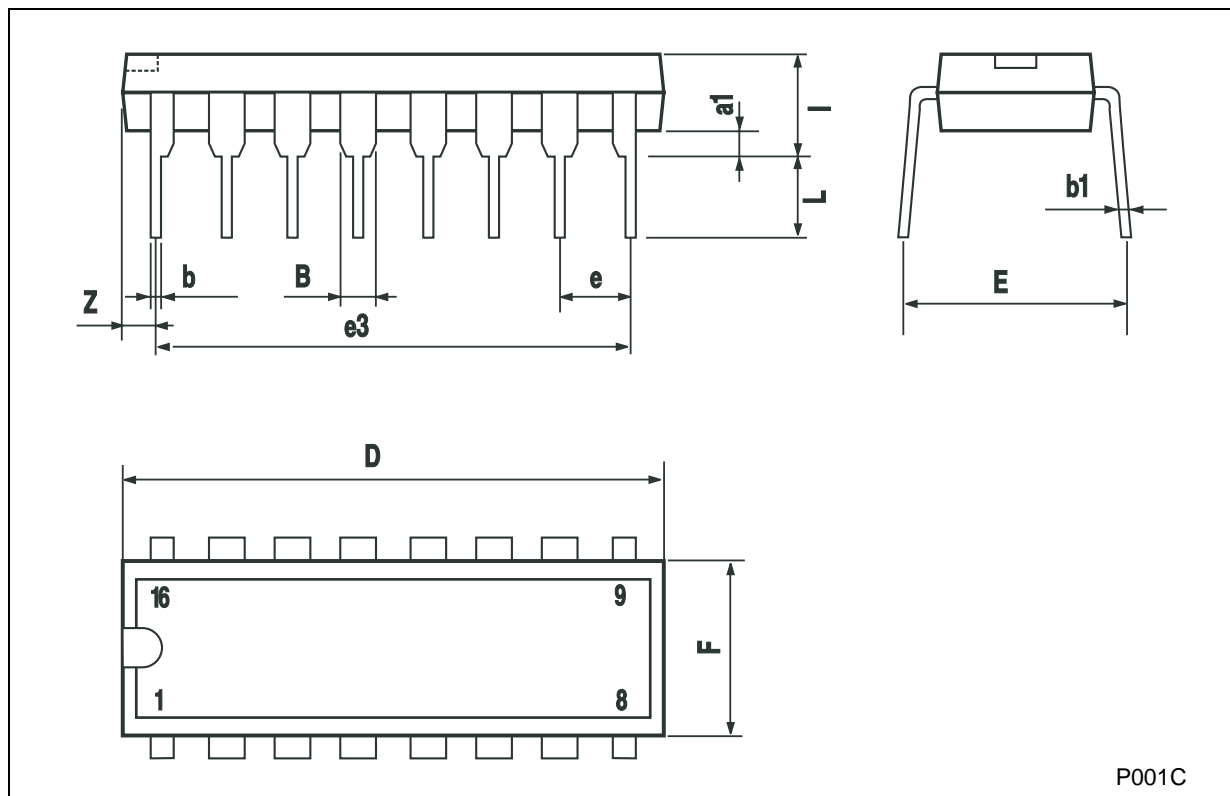
WAVEFORM 2 : CHANNEL BEING TURNED OFF ( $R_L = 1K\Omega$ ,  $f=1MHz$ ; 50% duty cycle)





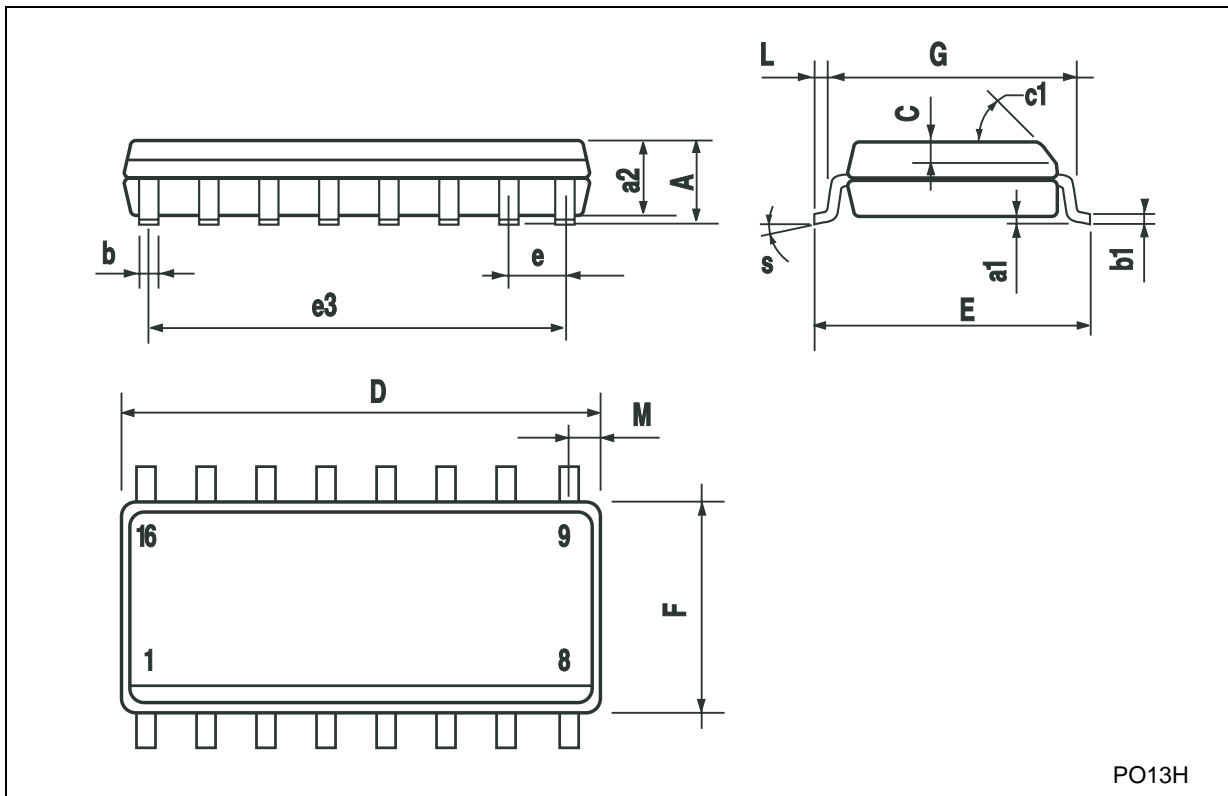
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8° (max.)					



PO13H

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>

