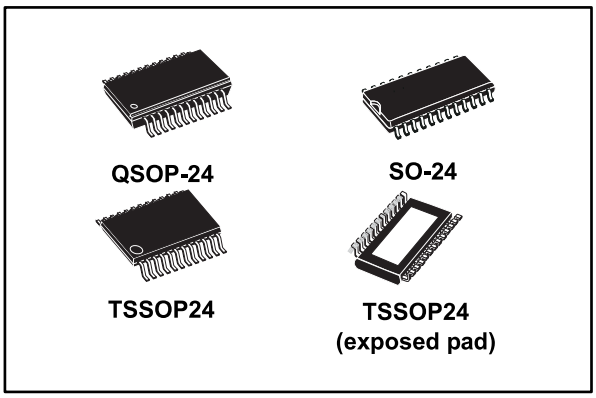
STP16CPP05

Low voltage 16-bit constant current LED sink driver

Datasheet - production data



Features

- 16 constant current output channels
- Adjustable output current through external resistor
- Output current: 3-40 mA
- Serial data in/parallel data ouT
- 3.3 V or 5 V supply voltage
- Max clock frequency 30 MHz
- Schmitt-trigger input
- ESD protection 2 kV HBM
- Thermal shutdown

Description

The STP16CPP05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The STP16CPP05 contains a 16-bit serial-in, parallel-out shift register that feeds a 16-bit, D-type storage register. In the output stage, sixteen regulated current sources provide from 3 mA to 40 mA constant current to drive the LEDs. The output current setup time is 40 ns (typ), thus improving the system performance. The LEDs' brightness can be controlled by using an external resistor to adjust the STP16CPP05 output current. The STP16CPP05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high clock frequency, 30 MHz, makes the device suitable for high data rate transmission. The 3.3 V voltage supply is useful in applications that interface with a 3.3 V micro controller.

Table 1: Device summary

Order code	Package	Packing
STP16CPP05MTR	SO-24	1000 parts per reel
STP16CPP05TTR	TSSOP24	2500 parts per reel
STP16CPP05XTTR	TSSOP24 exposed pad	2500 parts per reel
STP16CPP05PTR	QSOP-24	2500 parts per reel

Contents

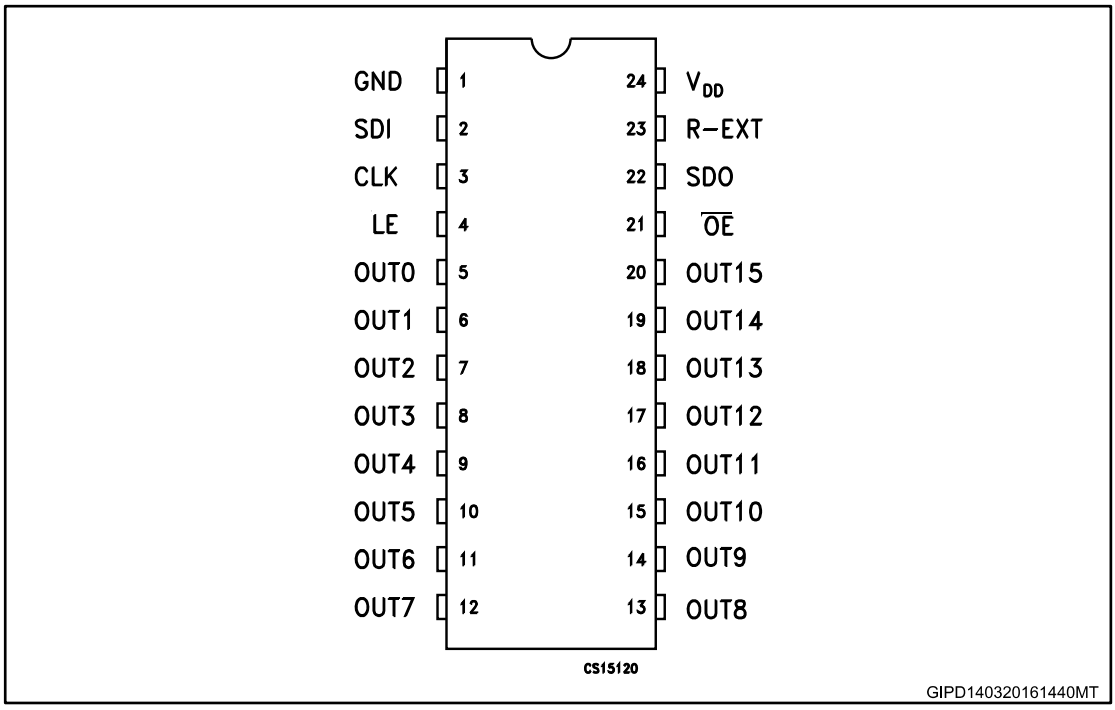
1 Summary description

Table 2: Typical current accuracy

Output voltage	Current accuracy		Output current	V_{DD}	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1.5%	± 5%	≥ 5 to 40 mA	3.3 V to 5 V	25 °C

1.1 Pin connection and description

Figure 1: Pin connection



The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3: Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE	Latch input terminal
5-20	OUT 0-15	Output terminal
21	$\overline{OE}$	Input terminal of output enable (active low)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V_{DD}	Supply voltage terminal

2 Electrical ratings

2.1 Absolute maximum ratings

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DD}	Supply voltage	0 to 7	V
V_O	Output voltage	-0.5 to 20	V
I_O	Output current	50	mA
V_I	Input voltage	-0.4 to V_{DD} + 0.4	V
I_{GND}	GND terminal current	800	mA
f_{CLK}	Clock frequency	50	MHz

2.2 Thermal data

Table 5: Thermal data

Symbol	Parameter		Value	Unit
T_{OPR}	Operating temperature range		-40 to +125	°C
T_{STG}	Storage temperature range		-55 to +150	°C
R_{thJA}	Thermal resistance junction-ambient	SO-24	60	°C/W
		TSSOP24	85	°C/W
		TSSOP24 (1) exposed pad	37.5	°C/W
		QSOP-24	72	°C/W

Notes:

(1) The exposed pad should be soldered directly to the PCB to realize the thermal benefits.

2.3 Recommended operating conditions

Table 6: Recommended operating conditions at 25 °C

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage		3.0		5.5	V
V_O	Output voltage				20	V
I_O	Output current	OUTn	3		40	mA
I_{OH}	Output current	SERIAL-OUT			+1	mA
I_{OL}	Output current	SERIAL-OUT			-1	mA
V_{IH}	Input voltage		0.7 V_{DD}		V_{DD} + 0.3	V
V_{IL}	Input voltage		-0.3		0.3 V_{DD}	V
t_{wLAT}	LE/DM1 pulse width	V_{DD} = 3.3 V to 5.0 V	20			ns
t_{wCLK}	CLK pulse width		16			ns
t_{wEN}	$\overline{OE}$ pulse width		70			ns
$t_{SETUP(D)}$	Setup time for DATA		5			ns
$t_{HOLD(D)}$	Hold time for DATA		5			ns
$t_{SETUP(L)}$	Setup time for LATCH		15			ns
f_{CLK}	Clock frequency	Cascade operation (1)			30	MHz

Notes:

(1) If the device is connected in cascade, it may not be possible achieve the maximum data transfer. Please consider the timings carefully.

3 Electrical characteristics

V_{DD} = 3.3 V to 5 V, T_A = 25 °C, unless otherwise specified.

Table 7: Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input voltage high level		0.7 V_{DD}		V_{DD}	V
V_{IL}	Input voltage low level		GND		0.3 V_{DD}	V
I_{OH}	Output leakage current	V_{OH} = 20 V		0.15	1	µA
V_{OL}	Output voltage (serial-OUT)	I_{OL} = 1 mA			0.4	V
V_{OH}	Output voltage (serial-OUT)	I_{OH} = -1 mA	V_{DD}-0.4V			V
I_{OL1}	Output current	V_O = 0.3 V, R_{ext} = 4 kΩ	4.75	5	5.25	mA
I_{OL2}		V_O = 0.3 V, R_{ext} = 980 Ω	19	20	21	
I_{OL3}		V_O = 1.3 V, R_{ext} = 490 Ω	38	40	42	
ΔI_{OL1}	Output current error between bit (all output ON)	V_O = 0.3 V, I_O = 5 mA, R_{ext} = 4 kΩ		± 1.2	± 5	%
ΔI_{OL2}		V_O = 0.3 V, I_O = 20 mA, R_{ext} = 980 Ω		± 0.5	± 3	
ΔI_{OL3}		V_O = 1.3 V, I_O = 40 mA, R_{ext} = 490 Ω		± 1.0	± 3	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	kΩ
$R_{SIN(down)}$	Pull-down resistor		100	200	400	kΩ
$I_{DD(OFF1)}$	Supply current (OFF)	R_{ext} = 980 OUT 0 to 15 = OFF		5.4	7.5	mA
$I_{DD(OFF2)}$		R_{ext} = 490 OUT 0 to 15 = OFF		8.0	9.5	
$I_{DD(ON1)}$	Supply current (ON)	R_{ext} = 980, OUT 0 to 15 = ON		5.5	7.5	
$I_{DD(ON2)}$		R_{ext} = 490, OUT 0 to 15 = ON		8.1	9.5	
Thermal	Thermal protection			170		°C

V_{DD} = 5 V, T_A = 25 °C, unless otherwise specified.

Table 8: Switching characteristics

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
t_{PLH1}	Propagation delay time, CLK- $\overline{OUTn}$, LE = H, $\overline{OE}$ = L	$V_{IH} = V_{DD}$ V_{IL} = GND C_L = 10 pF I_O = 20 mA V_L = 3.0 V R_{ext} = 1 KΩ R_L = 60 Ω	V_{DD} = 3.3 V	-	44	58	ns
			V_{DD} = 5 V	-	24	32	
t_{PLH2}	Propagation delay time, LE- $\overline{OUTn}$, $\overline{OE}$ = L		V_{DD} = 3.3 V	-	43	56	ns
			V_{DD} = 5 V	-	24	32	
t_{PLH3}	Propagation delay time, $\overline{OE}$ - $\overline{OUTn}$, LE = H		V_{DD} = 3.3 V	-	63	82	ns
			V_{DD} = 5 V	-	37	48	
t_{PLH}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	17	22	ns
			V_{DD} = 5 V	-	11	14	
t_{PHL1}	Propagation delay time, CLK- $\overline{OUTn}$, LE = H, $\overline{OE}$ = L		V_{DD} = 3.3 V	-	22	28	ns
			V_{DD} = 5 V	-	16	21	
t_{PHL2}	Propagation delay time, LE- $\overline{OUTn}$, $\overline{OE}$ = L		V_{DD} = 3.3 V	-	19	25	ns
			V_{DD} = 5 V	-	15	20	
t_{PHL3}	Propagation delay time, $\overline{OE}$ - $\overline{OUTn}$, LE = H		V_{DD} = 3.3 V	-	16	21	ns
			V_{DD} = 5 V	-	13	17	
t_{PHL}	Propagation delay time, CLK-SDO		V_{DD} = 3.3 V	-	21	27	ns
			V_{DD} = 5 V	-	13	17	
t_{ON}	Output rise time 10~90% of voltage waveform		V_{DD} = 3.3 V	-	26	35	ns
			V_{DD} = 5 V	-	12	16	
t_{OFF}	Output fall time 90~10% of voltage waveform		V_{DD} = 3.3 V	-	4	6	ns
			V_{DD} = 5 V	-	3	5	
t_r	CLK rise time (1)			-		5000	ns
t_f	CLK fall time (1)			-		5000	ns

Notes:

(1) In order to achieve high cascade data transfer, please consider tr/tf timings carefully.

4 Equivalent circuit and outputs

Figure 2: OE terminal

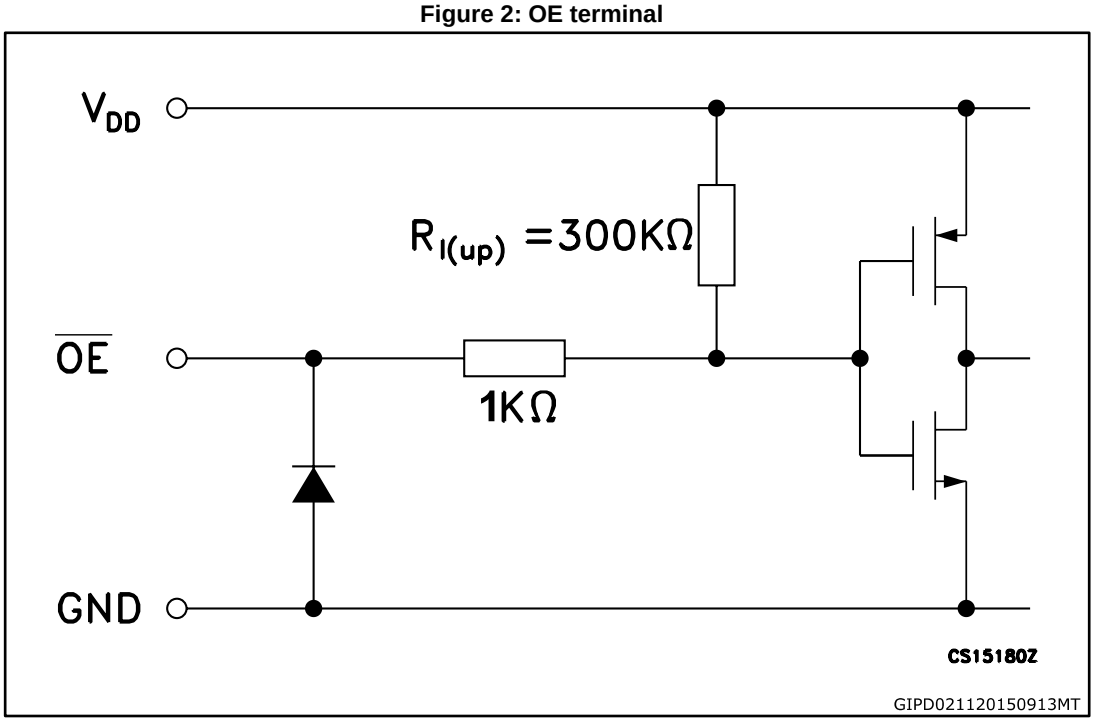


Figure 3: LE terminal

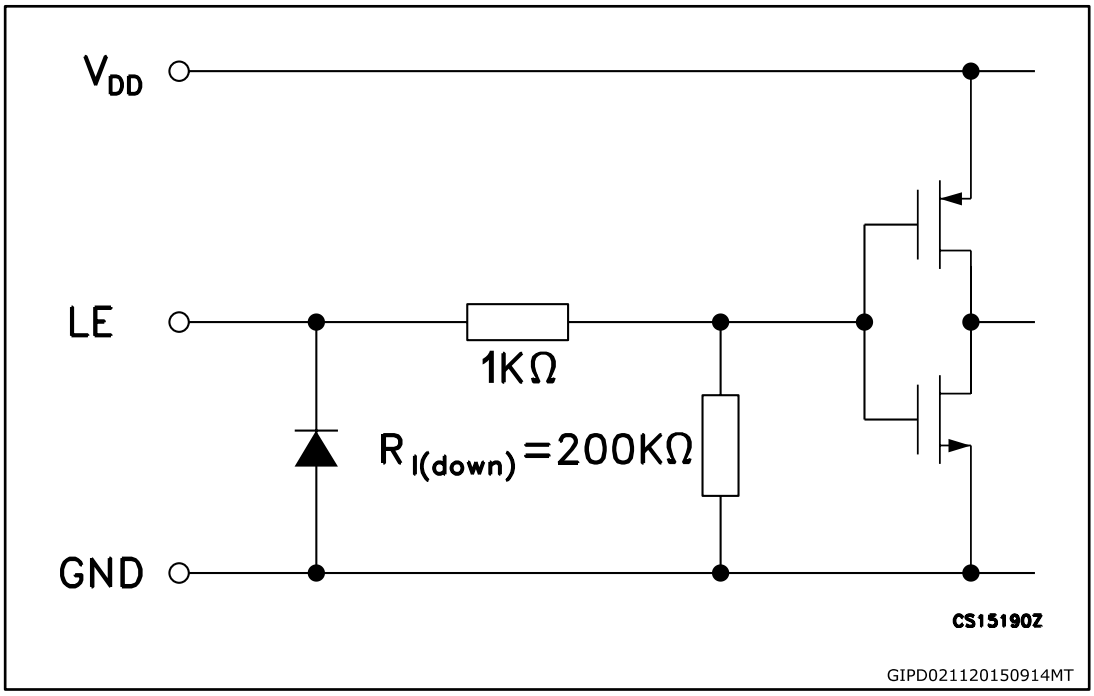


Figure 4: CLK, SDI terminal

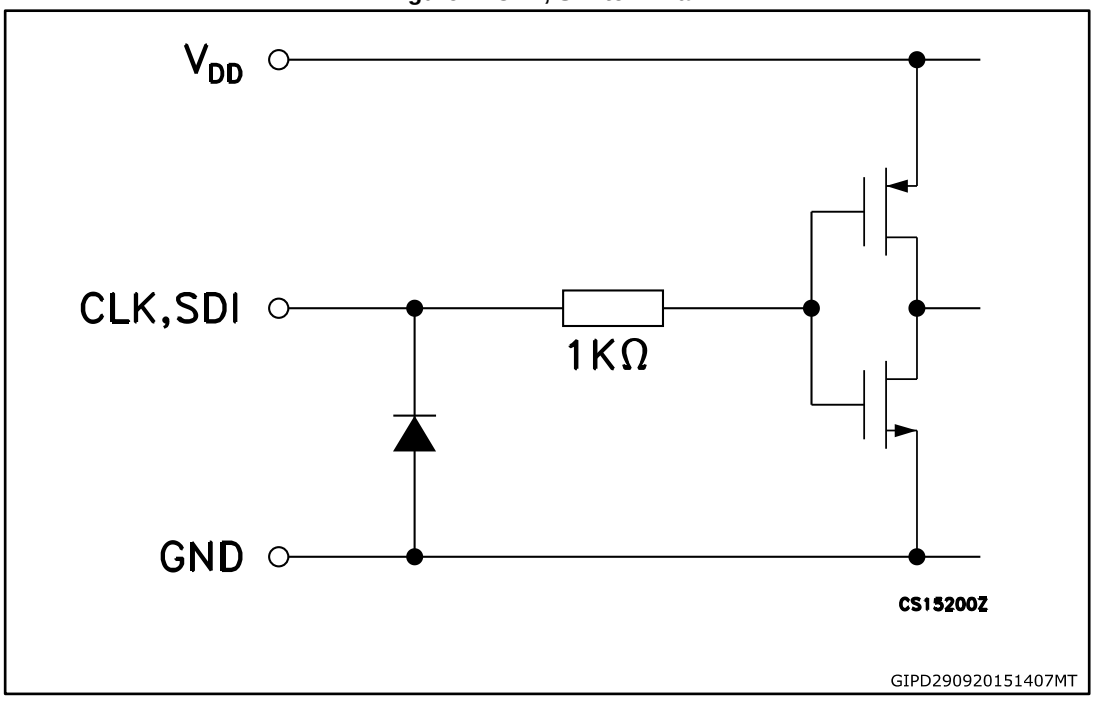


Figure 5: SDO terminal

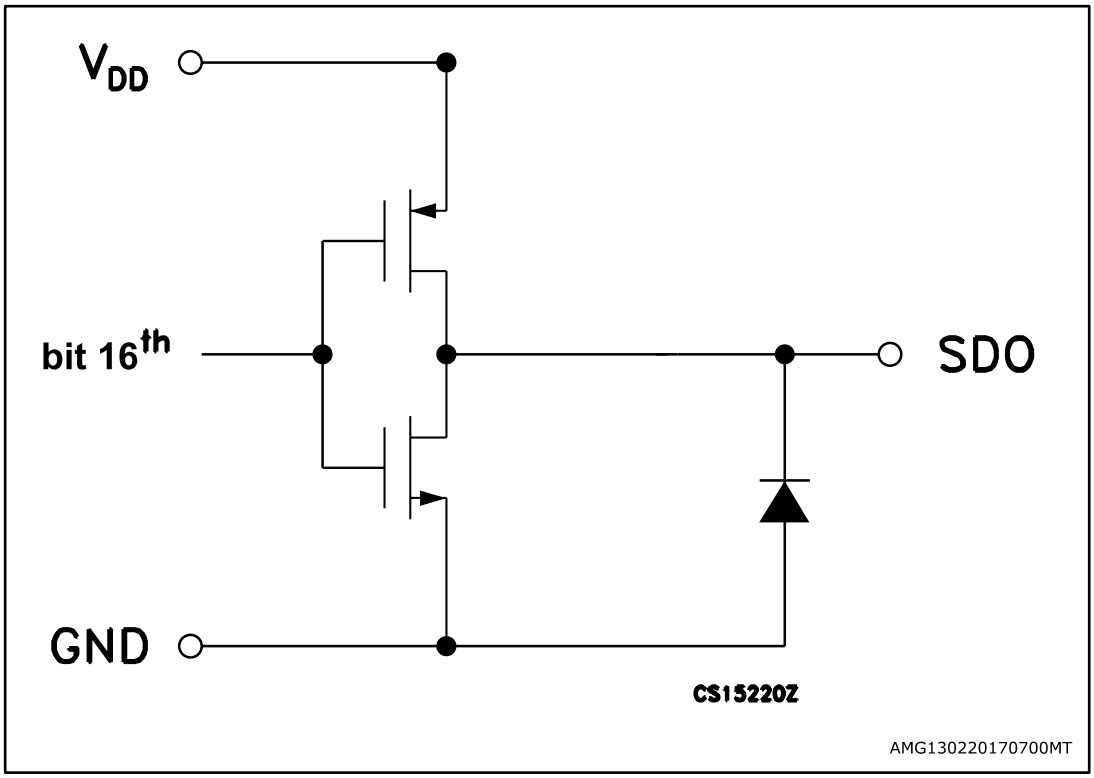
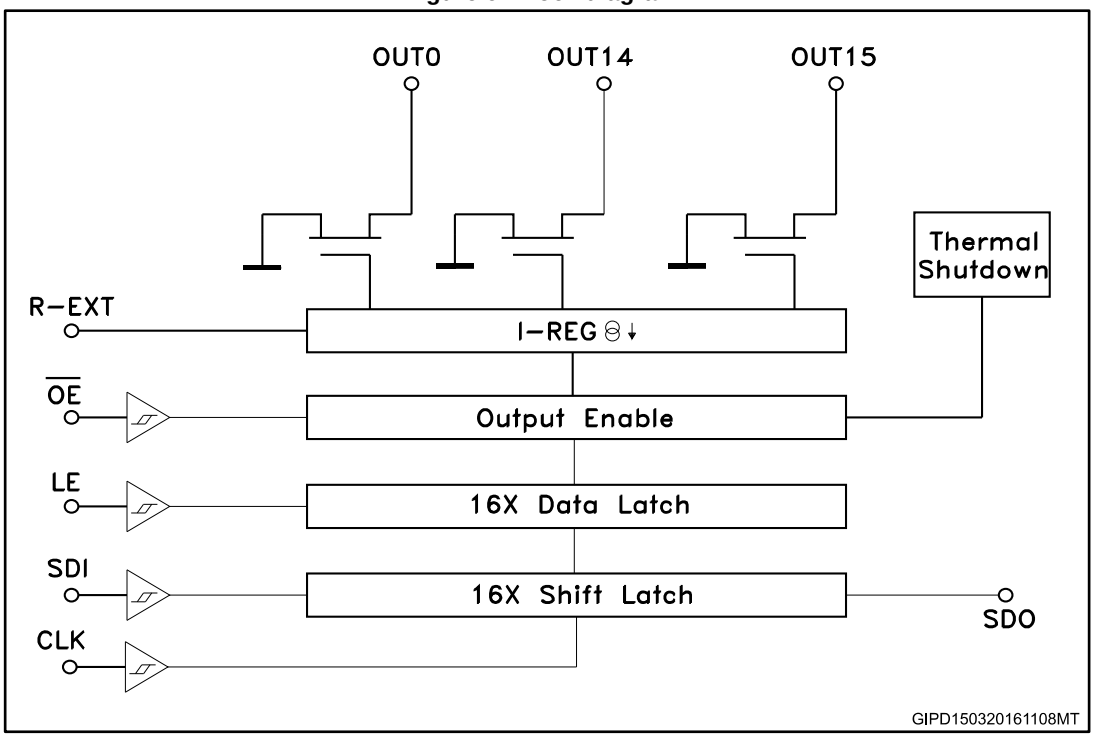


Figure 6: Block diagram



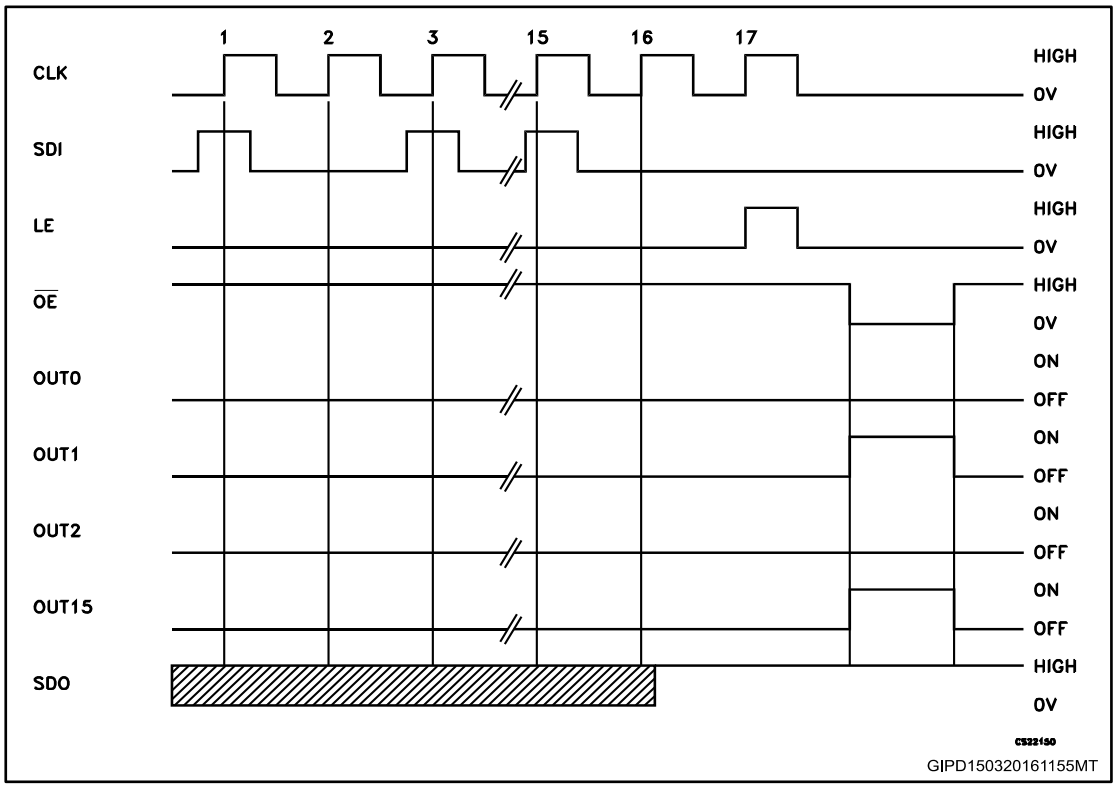
5 Timing diagrams

Table 9: Truth table

CLOCK	LE	$\overline{OE}$	SERIAL-IN	$\overline{OUT0}$ ..... $\overline{OUT7}$ ..... $\overline{OUT15}$	SDO
_|‾	H	L	Dn	Dn ..... Dn - 7 ..... Dn -15	Dn - 15
_|‾	L	L	Dn + 1	No change	Dn - 14
_|‾	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
‾|_	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn -13	Dn - 13
‾|_	X	H	Dn + 3	OFF	Dn - 13

OUTn = ON when Dn = H OUTn = OFF when Dn = L.

Figure 7: Timing diagram



The latches circuit holds data when the LE terminal is Low.

1 When LE terminal is at high level, latch circuit does not hold the data it passes from the input to the output.

2 When $\overline{OE}$ terminal is at low level, output terminals OUT0 to OUT15 respond to the data, either ON or OFF.

3 When $\overline{OE}$ terminal is at high level, it switches off all the data on the output terminal.

Figure 8: Clock, serial-in, serial-out

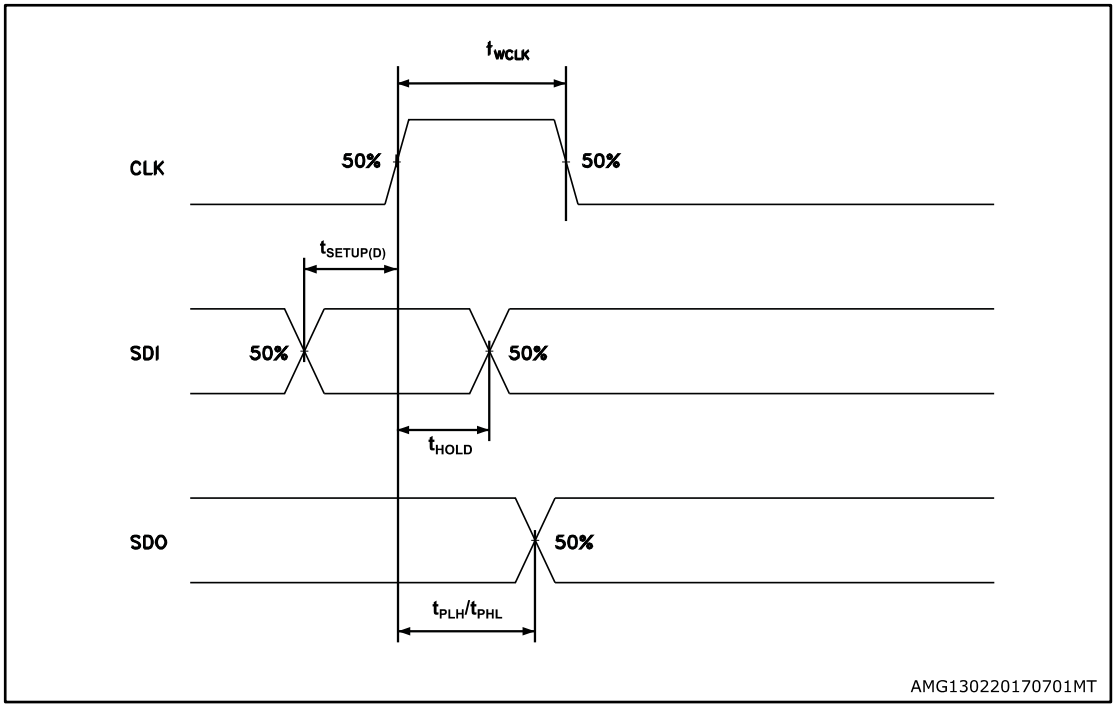


Figure 9: Clock, serial-in, latch, enable, outputs

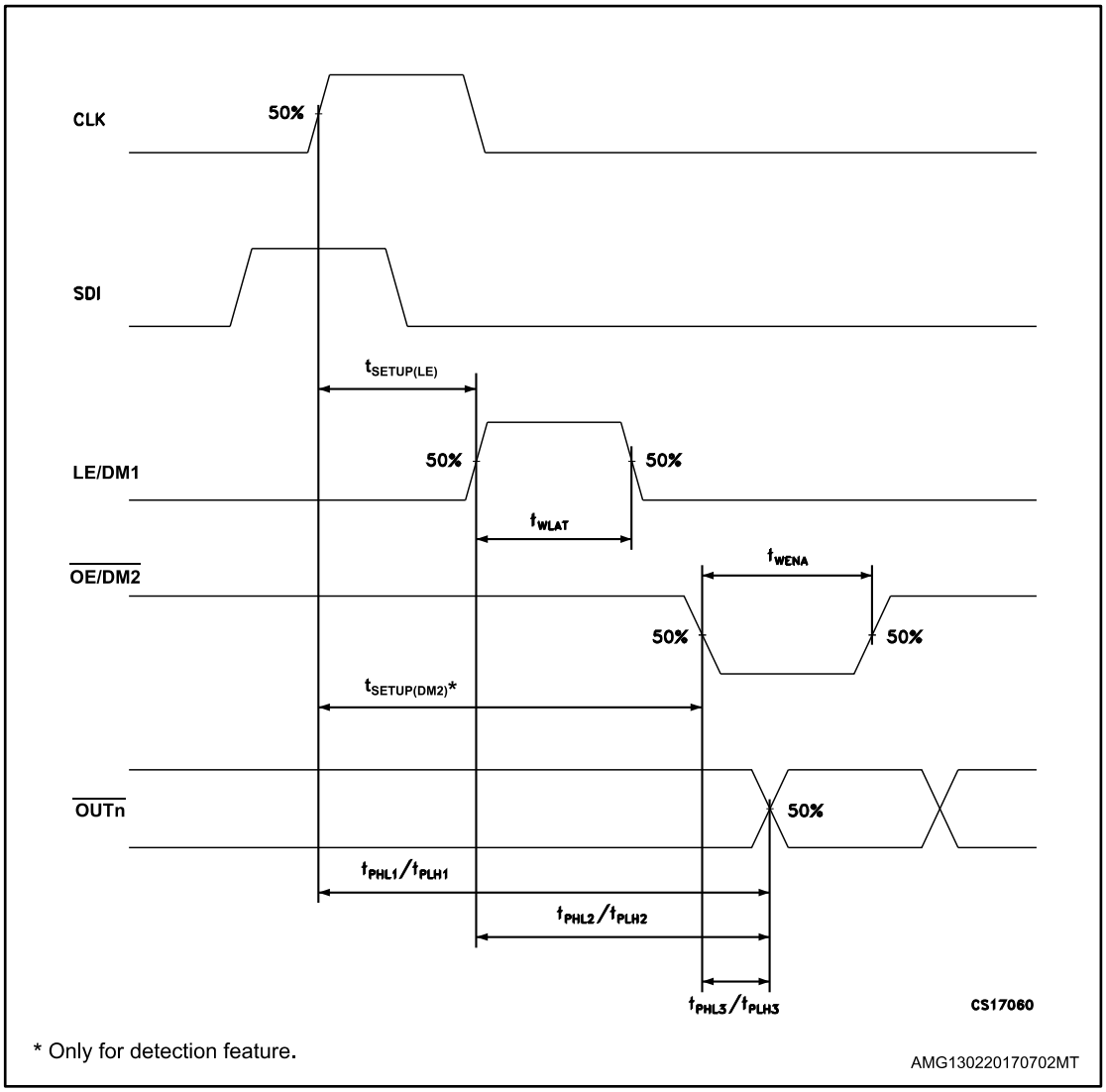
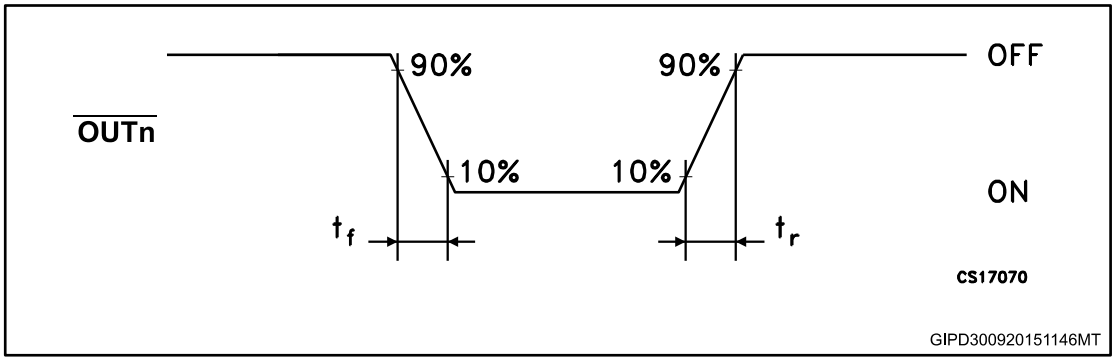


Figure 10: Outputs



6 Typical characteristics

Figure 11: Output current vs Rext resistor

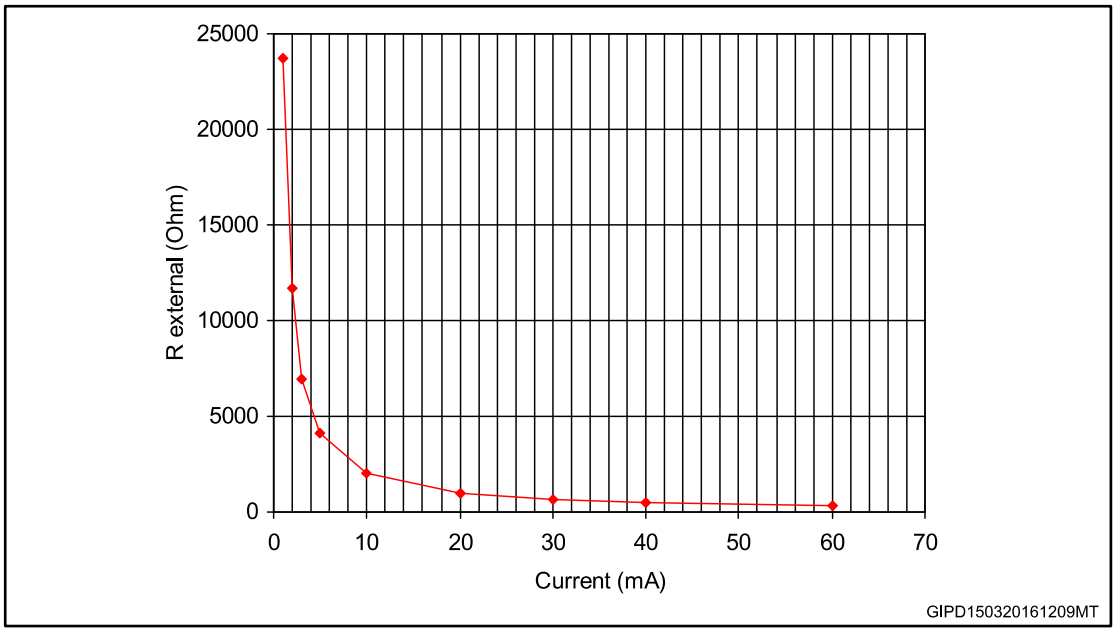


Table 10: Output current vs Rext resistor

Rext (Ω)	Output current (mA)
23700	1
11730	2
6930	3
4090	5
2025	10
1000	20
667	30
497	40
331	60

Figure 12: Output current vs ± ΔI_{OL}(%) (temp. = 25 °C, V_{dd} = 5 V, pin = all outputs)

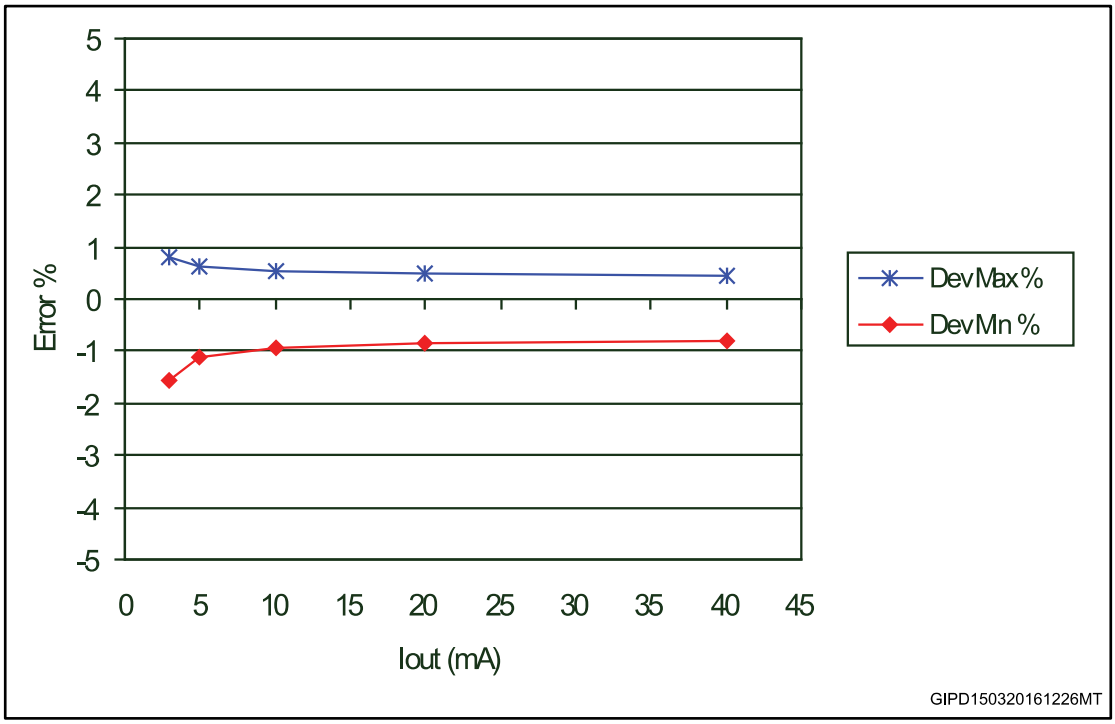


Figure 13: I_{SET} vs drop out voltage (V_{drop})

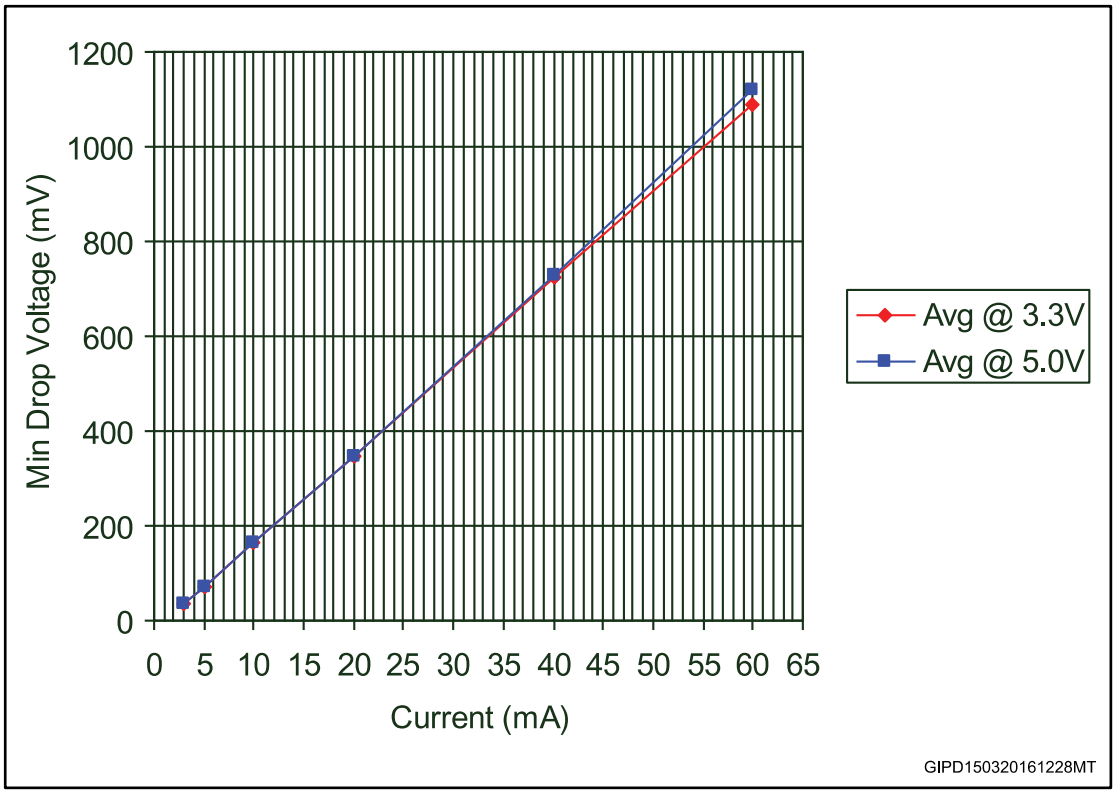


Table 11: I_{SET} vs drop out voltage (V_{drop})

Vdd (V)	Iset (mA)	Min (mV)	Max (mV)	Avg (mV)	Vdd (V)	Iset (mA)	Min (mV)	Max (mV)	Avg (mV)
3.3	3	35	37	36	5.0	3	37	37	37
	5	71	72	71		5	72	73	72
	10	162	165	163		10	162	164	163
	20	347	348	347		20	345	347	346
	40	724	724	724		40	725	728	726
	60	1080	1090	1080		60	1090	1140	1110

7 Tast circuits

Figure 14: DC characteristic

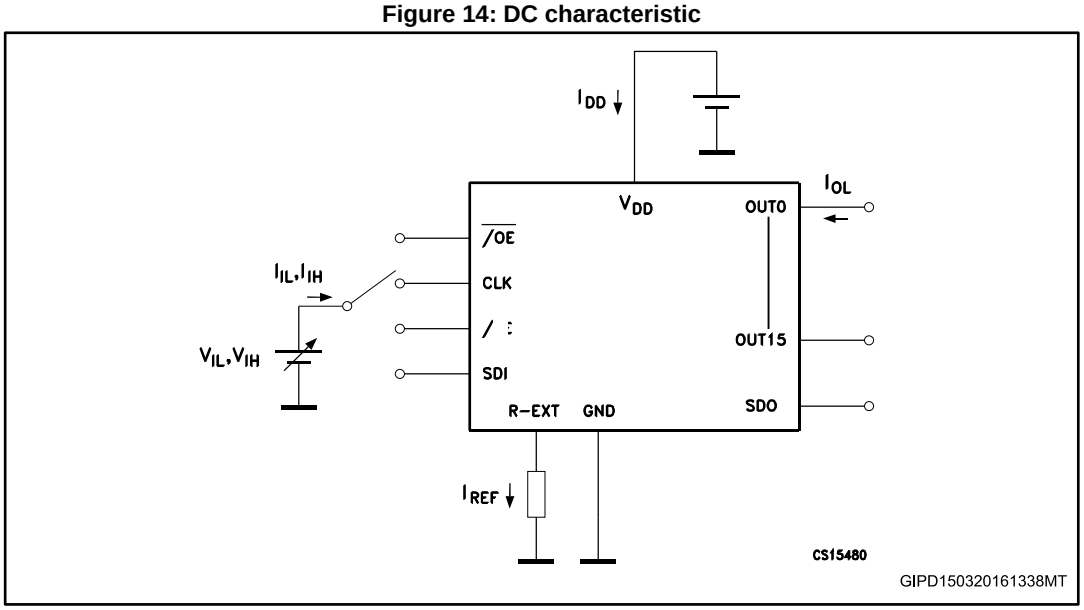


Figure 15: AC characteristic

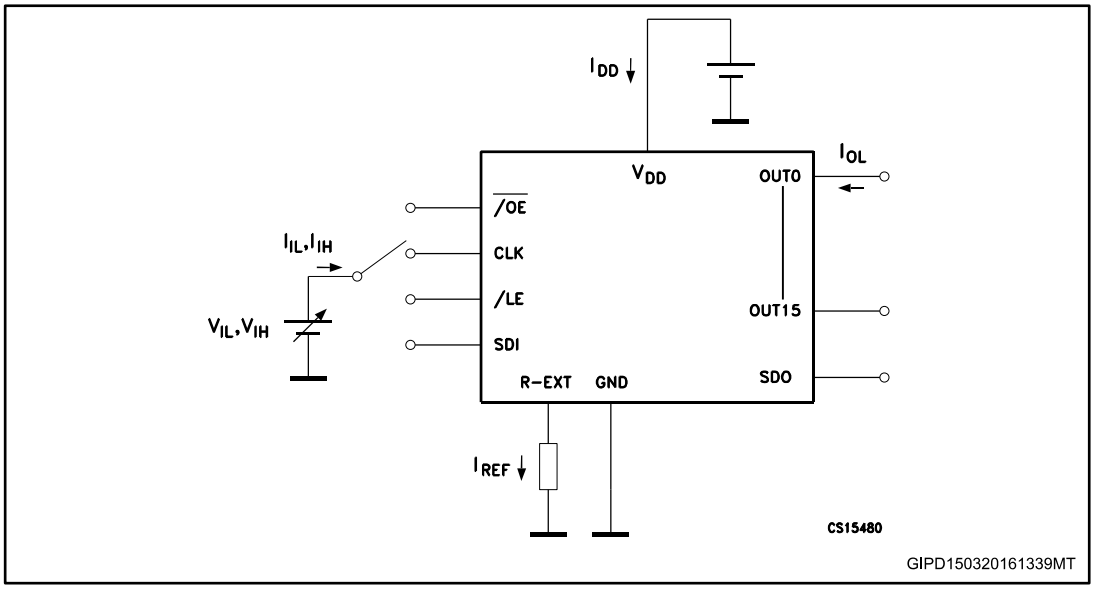
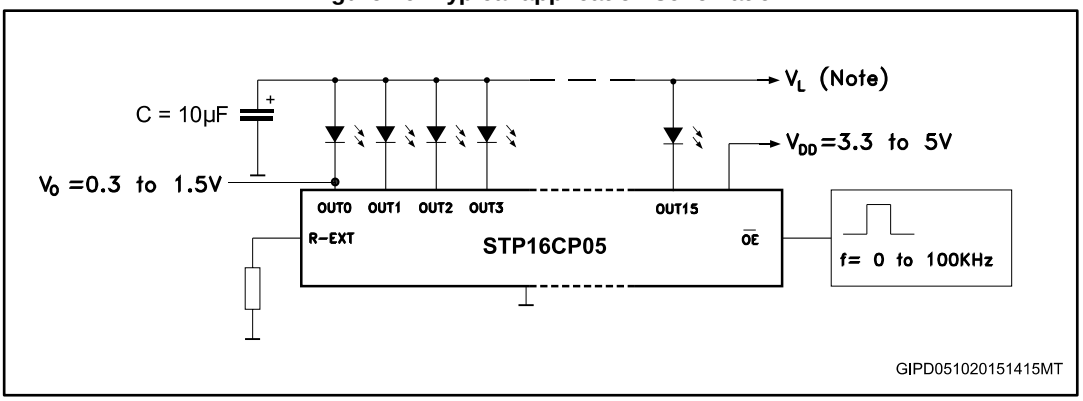


Figure 16: Typical application schematic



V_L will be determined by the V_F of the LEDs.

Test condition:

Temp. = 25 °C, V_{DD} = 3.3 V, V_{IN} = V_{DD}, C_L = 10 pF, Freq. = 1 MHz, Ch1 = CLK, Ch2 = SDI, Ch3 = OUTn, Ch4 = V_{OUT}

Figure 17: Turn ON output current setup

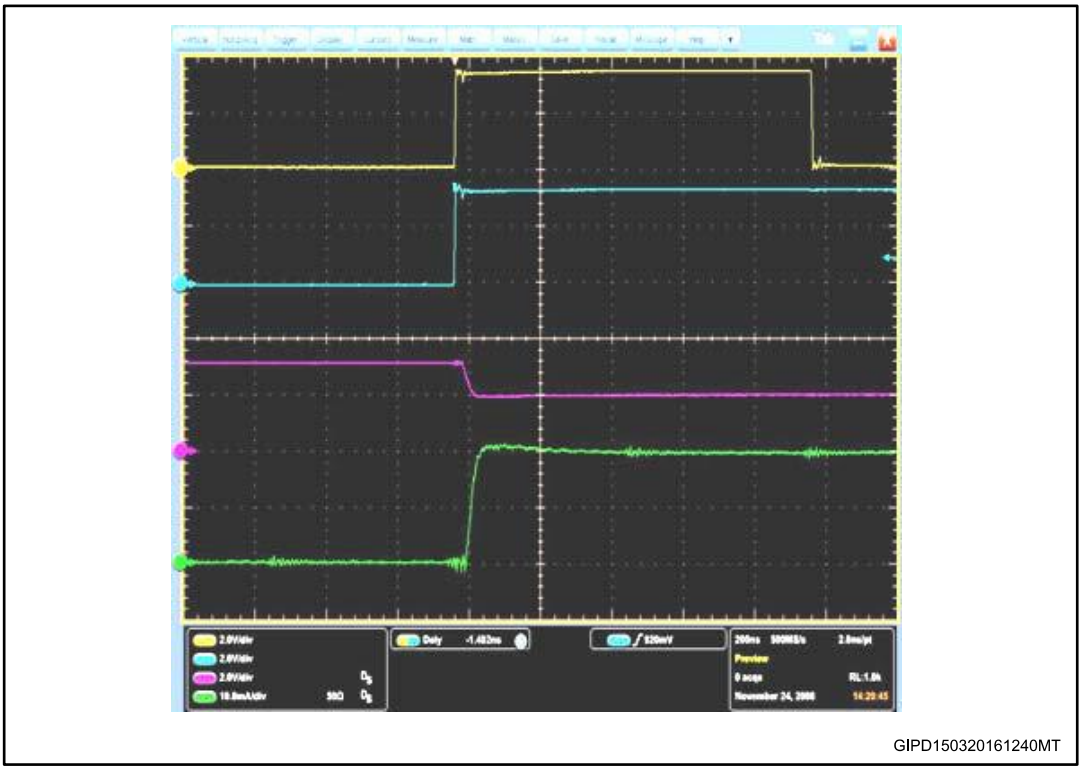
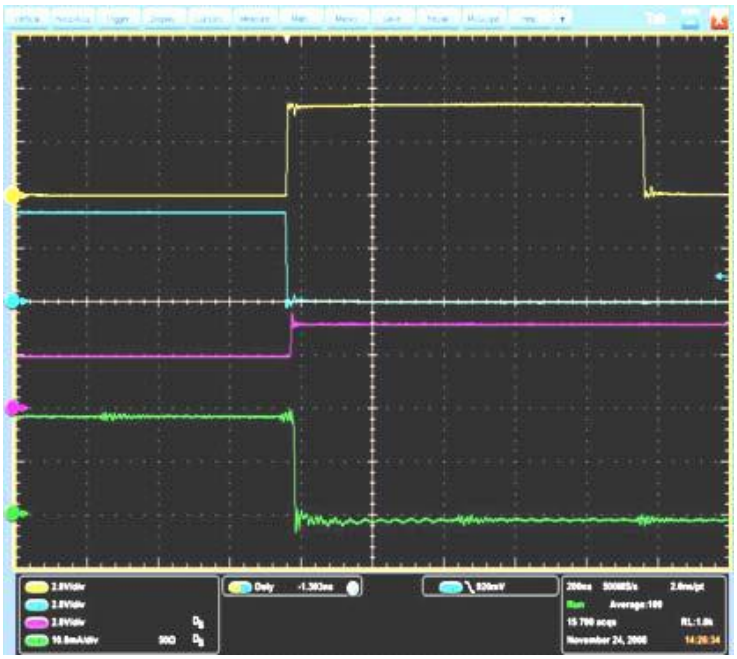


Figure 18: Turn OFF output current setup



GIPD150320161241MT

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

8.1 QSOP-24 package information

Figure 19: QSOP-24 package outline

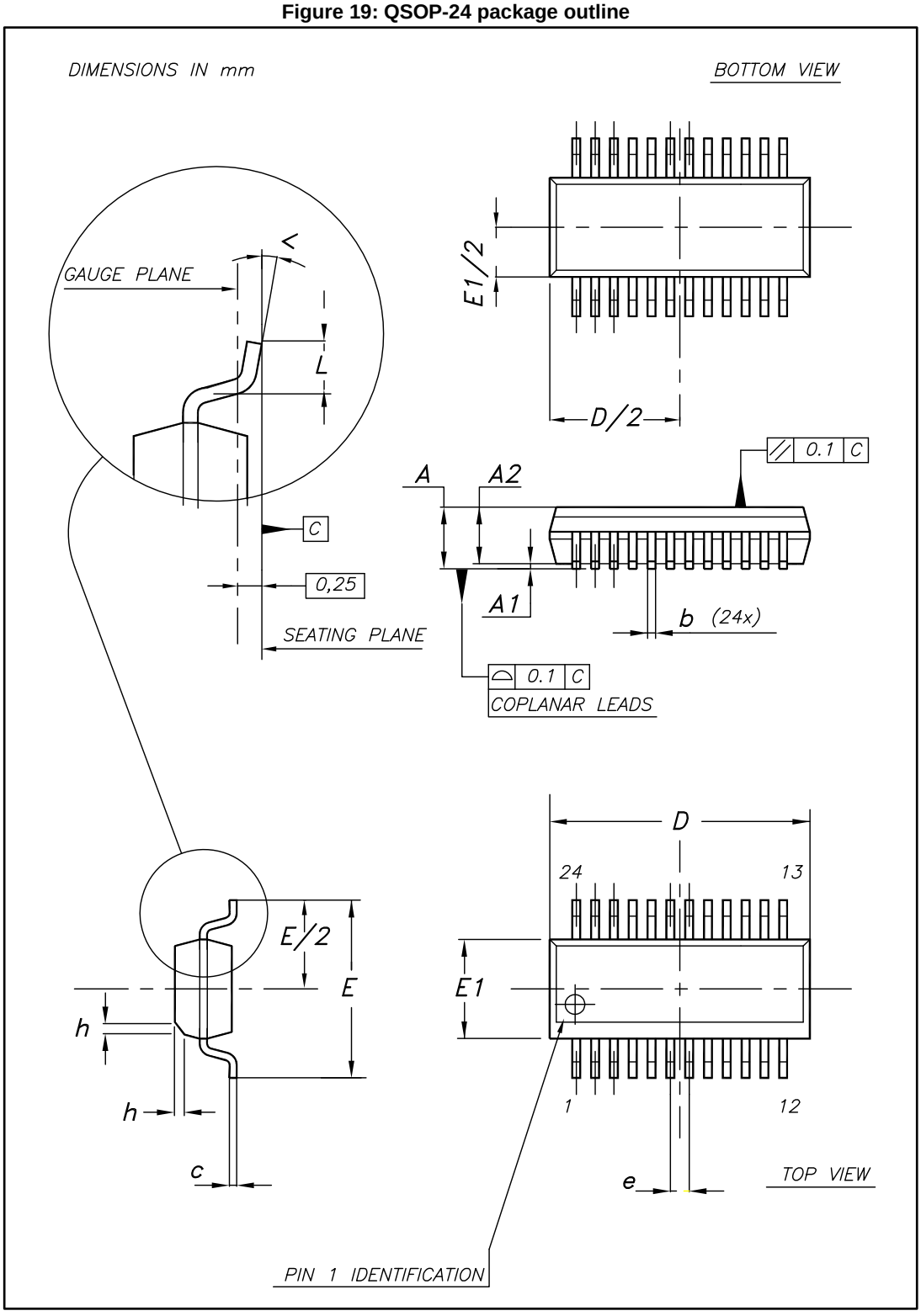


Table 12: QSOP-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.54	1.62	1.73
A1	0.10	0.15	0.25
A2		1.47	
b	0.20		0.31
c	0.17		0.254
D	8.56	8.66	8.76
E	5.80	6.00	6.20
E1	3.80	3.91	4.01
e		0.635	
L	0.40	0.635	0.89
h	0.25	0.33	0.41
<	0°		8°

8.2 SO-24 package information

Figure 20: SO-24 package outline

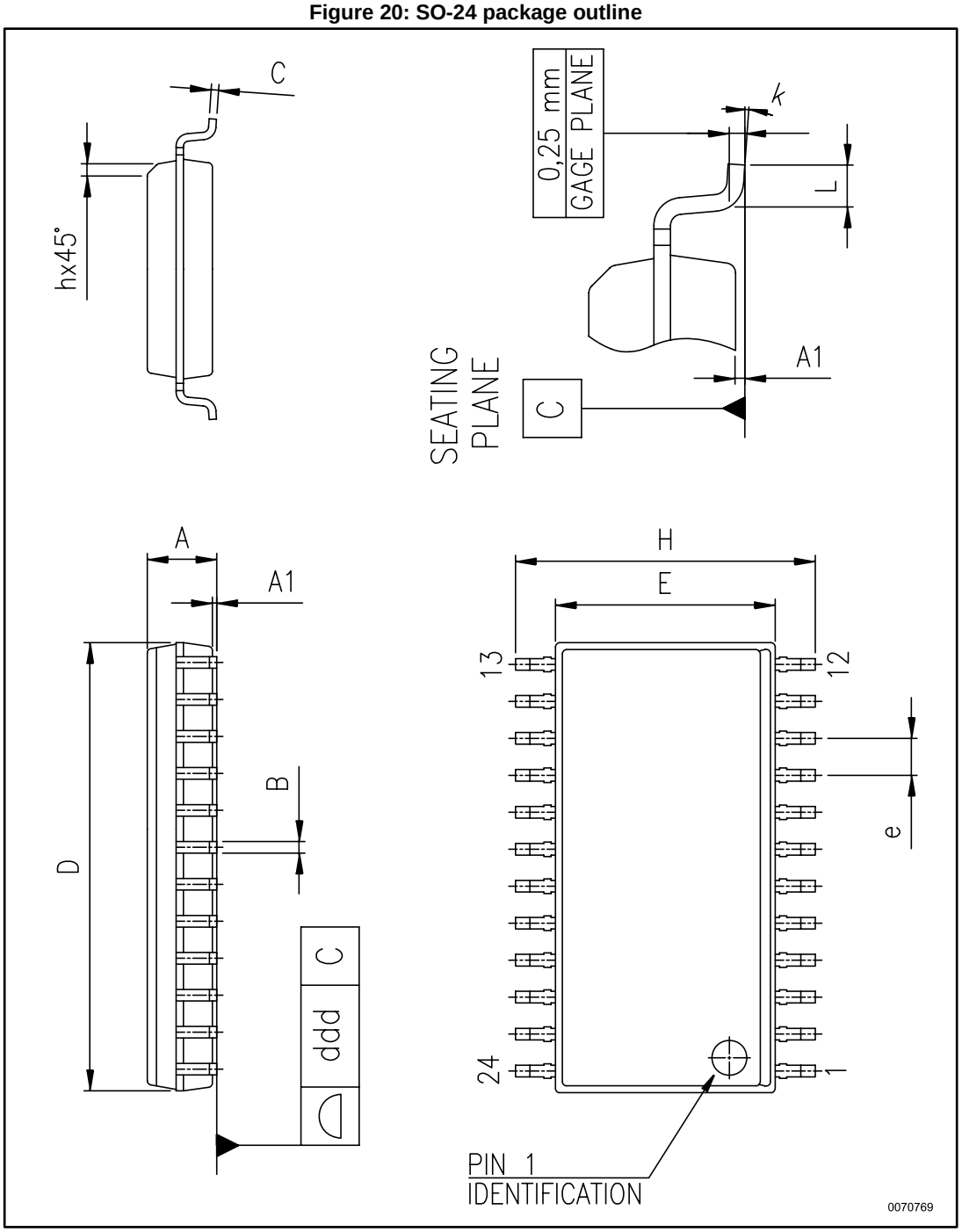


Table 13: SO-24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.35		2.65
A1	0.10		0.30
B	0.33		0.51
C	0.23		0.32
D	15.20		15.60
E	7.40		7.60
e		1.27	
H	10.00		10.65
h	0.25		0.75
L	0.40		1.27
k	0		8
ddd			0.10

8.3 TSSOP24 package information

Figure 21: TSSOP24 package outline

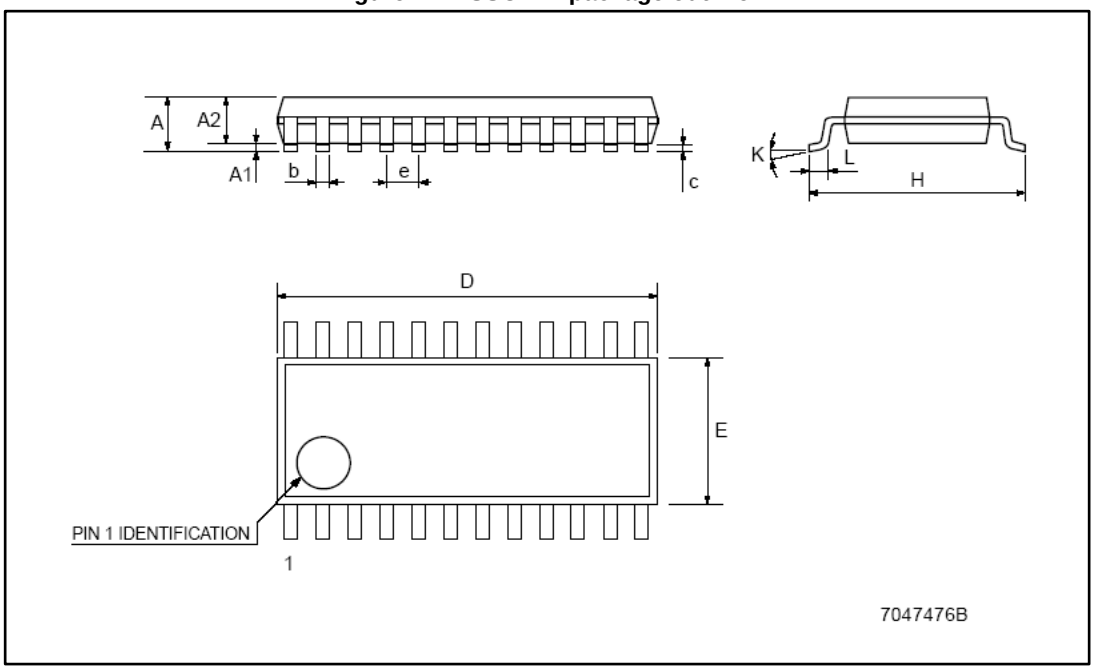


Table 14: TSSOP24 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.1
A1	0.05		0.15
A2		0.9	
b	0.19		0.30
c	0.09		0.20
D	7.7		7.9
E	4.3		4.5
e		0.65 BSC	
H	6.25		6.5
K	0°		8°
L	0.50		0.70

8.4 TSSOP24 exposed pad package information

Figure 22: TSSOP24 exposed pad package outline

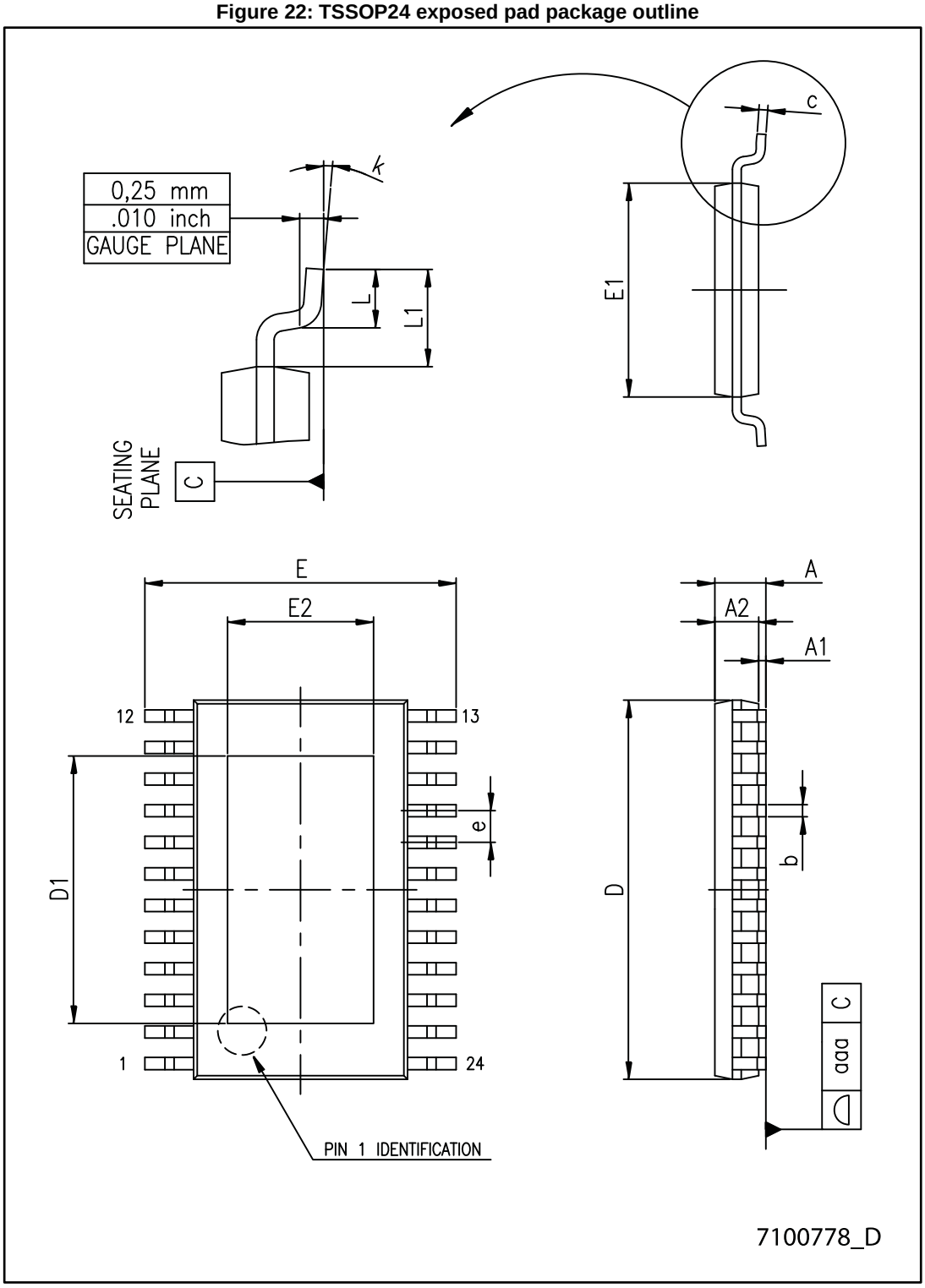


Table 15: TSSOP24 exposed pad mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	7.70	7.80	7.90
D1	4.80	5.00	5.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	3.00	3.20	3.40
e		0.65	
L	0.45	060	075
L1		1.00	
k	0°		8°
aaa			0.10

8.5 TSSOP24, TSSOP24 exposed pad and SO-24 packing information

Figure 23: TSSOP24, TSSOP24 exposed pad and SO-24 reel outline

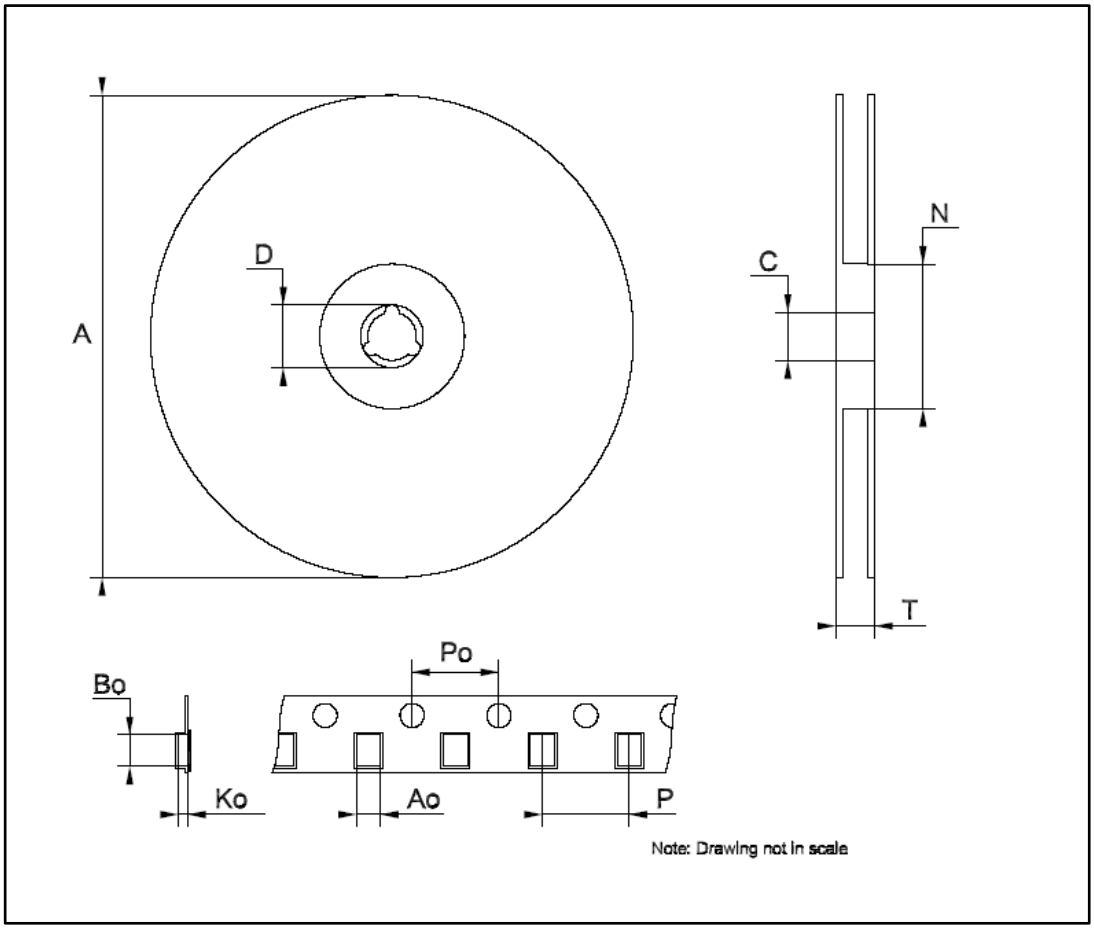


Table 16: TSSOP24 and TSSOP24 exposed pad tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	22.4
Ao	6.8	-	7
Bo	8.2	-	8.4
Ko	1.7	-	1.9
Po	3.9	-	4.1
P	11.9	-	12.1

Table 17: SO-24 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A		-	330
C	12.8	-	13.2
D	20.2	-	
N	60	-	
T		-	30.4
Ao	10.8	-	11.0
Bo	15.7	-	15.9
Ko	2.9	-	3.1
Po	3.9	-	4.1
P	11.9	-	12.1

9 Revision history

Table 18: Document revision history

Date	Revision	Changes
11-Feb-2009	1	First release
22-Oct-2009	2	Updated Figure 11 on page 14 and Figure 10 on page 14.
10-Jun-2014	3	Updated *Section 8: Package mechanical data*. Added *Section 9: Packaging mechanical data*. Minor text changes.
08-Apr-2016	4	Updated *Section 8.1: "QSOP-24 package information"*. Minor text changes.
09-Mar-2017	5	Updated *Figure 5: "SDO terminal"*, *Figure 8: "Clock, serial-in, serial-out"* and *Figure 9: "Clock, serial-in, latch, enable, outputs"*. Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.