

# 74ABT377

## Octal D-Type Flip-Flop with Clock Enable

### General Description

The ABT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously when the Clock Enable ( $\overline{CE}$ ) is LOW.

The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The  $\overline{CE}$  input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

### Features

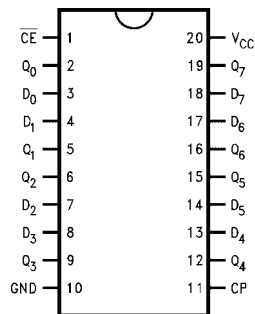
- Clock enable for address and data synchronization applications
- Eight edge-triggered D-type flip-flops
- Buffered common clock
- See ABT273 for master reset version
- See ABT373 for transparent latch version
- See ABT374 for 3-STATE version
- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability
- Disable time less than enable time to avoid bus contention

### Ordering Code:

Order Number	Package Number	Package Description
74ABT377CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body
74ABT377CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT377CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ABT377CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Connection Diagram



### Pin Descriptions

Pin Names	Descriptions
$D_0$ – $D_7$	Data Inputs
$\overline{CE}$	Clock Enable (Active LOW)
CP	Clock Pulse Input
$Q_0$ – $Q_7$	Data Outputs

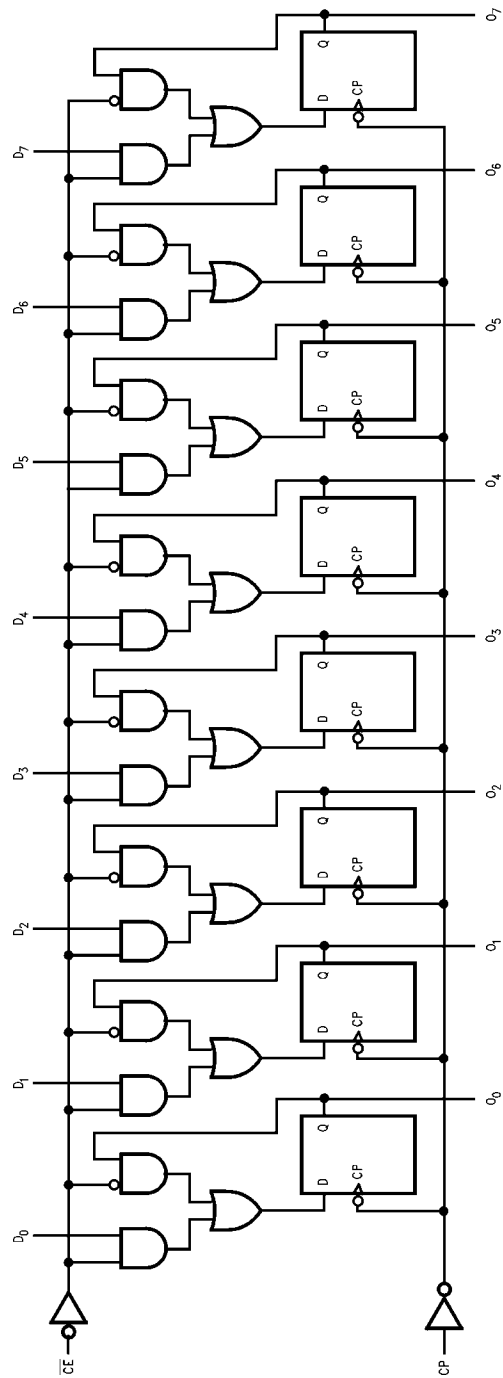
### Truth Table

Operating Mode	Inputs			Output
	CP	$\overline{CE}$	$D_n$	$Q_n$
Load "1"	↗	I	h	H
Load "0"	↗	I	I	L
Hold (Do Nothing)	↗	h	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level      L = LOW Voltage Level  
X = Immaterial      ↗ = LOW-to-HIGH Clock Transition  
h = HIGH Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition  
I = LOW Voltage Level one setup time prior to the LOW-to-HIGH Clock Transition

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Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-OFF State	-0.5V to +4.75V
in the HIGH State	-0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	Twice the rated I <sub>OL</sub> (mA)
DC Latchup Source Current (Across Comm Operating Range)	-500 mA
Over Voltage Latchup	V <sub>CC</sub> + 4.5V

**Recommended Operating Conditions**

Free Air Ambient Temperature	-40°C to +85°C
Supply Voltage	+4.5V to +5.5V
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
Data Input	50 mV/ns
Enable Input	20 mV/ns

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs

**DC Electrical Characteristics**

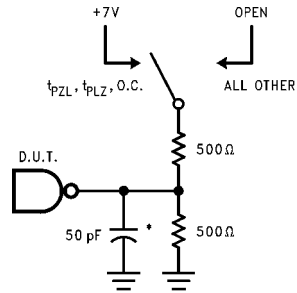
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	2.5			V	Min	I <sub>OH</sub> = -3 mA I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage			0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			1	μA	Max	V <sub>IN</sub> = 2.7V (Note 3) V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-1	μA	Max	V <sub>IN</sub> = 0.5V (Note 3) V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCT</sub>	Maximum I <sub>CC</sub> /Input Outputs Enabled			1.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or GND
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> No Load			0.3	mA/ MHz	Max	Outputs Open (Note 4) One bit Toggling, 50% Duty Cycle

**Note 3:** Guaranteed but not tested.

**Note 4:** For 8 bits toggling, I<sub>CCD</sub> < 0.5 mA/MHz.

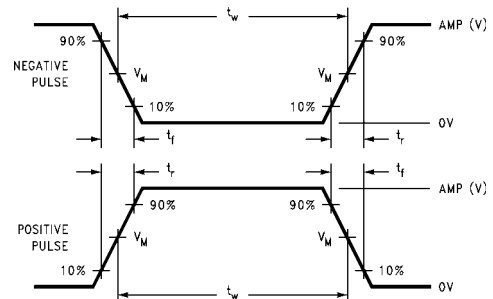
AC Electrical Characteristics							
(SOIC Package)							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	150	200		150		MHz
t <sub>PLH</sub>	Propagation Delay	2.2		6.0	2.2	6.0	ns
t <sub>PHL</sub>	CP to O <sub>n</sub>	2.8		6.8	2.8	6.8	
AC Operating Requirements							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C V <sub>CC</sub> = 4.5V to 5.5V C <sub>L</sub> = 50 pF		Units	
		Min	Max	Min	Max		
t <sub>S</sub> (H)	Setup Time, HIGH	2.0		2.0		ns	
t <sub>S</sub> (L)	or LOW D <sub>n</sub> to CP	2.0		2.0			
t <sub>H</sub> (H)	Hold Time, HIGH	1.8		1.8		ns	
t <sub>H</sub> (L)	or LOW D <sub>n</sub> to CP	1.8		1.8			
t <sub>S</sub> (H)	Setup Time, HIGH	3.0		3.0		ns	
t <sub>S</sub> (L)	or LOW $\overline{CE}$ to CP	3.0		3.0			
t <sub>H</sub> (H)	Hold Time, HIGH	1.0		1.0		ns	
t <sub>H</sub> (L)	or LOW $\overline{CE}$ to CP	1.0		1.0			
t <sub>W</sub> (H)	Pulse Width, CP,	3.3		3.3		ns	
t <sub>W</sub> (L)	HIGH or LOW	3.3		3.3			
Capacitance							
(SOIC Package) (Note 5)							
Symbol	Parameter	Typ	Units	Conditions			
C <sub>IN</sub>	Input Capacitance	5	pF	V <sub>CC</sub> = 0V, T <sub>A</sub> = 25°C			
C <sub>OUT</sub> (Note 5)	Output Capacitance	9	pF	V <sub>CC</sub> = 5.0V			
<b>Note 5:</b> C <sub>OUT</sub> is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.							

**AC Loading**



\*Includes jig and probe capacitance

**FIGURE 1. Standard AC Test Load**



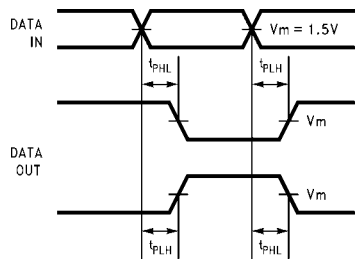
**FIGURE 2. V<sub>M</sub> = 1.5V**

**Input Pulse Requirements**

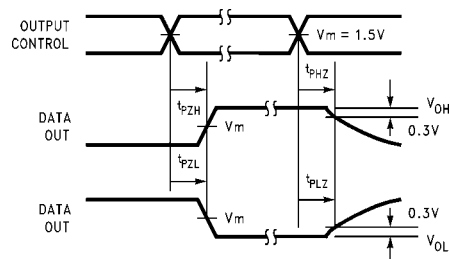
Amplitude	Rep. Rate	t <sub>w</sub>	t <sub>r</sub>	t <sub>f</sub>
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

**FIGURE 3. Test Input Signal Requirements**

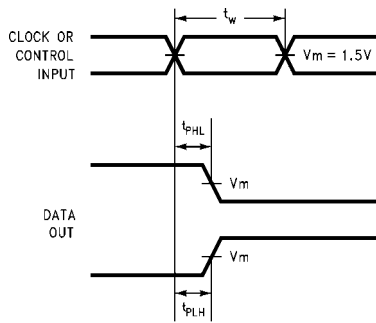
**AC Waveforms**



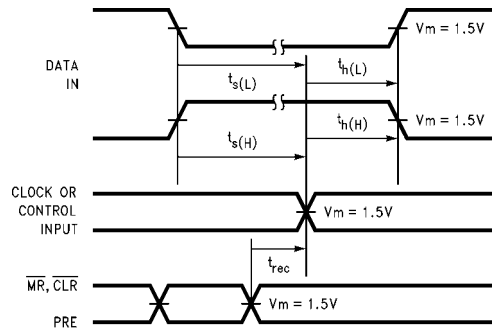
**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**



**FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times**

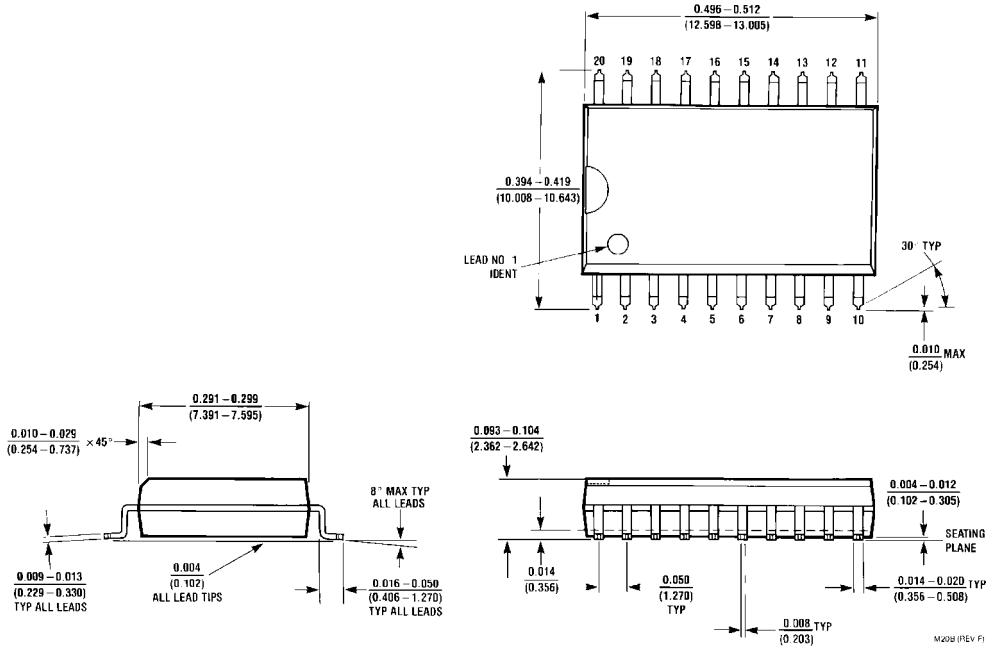


**FIGURE 5. Propagation Delay, Pulse Width Waveforms**



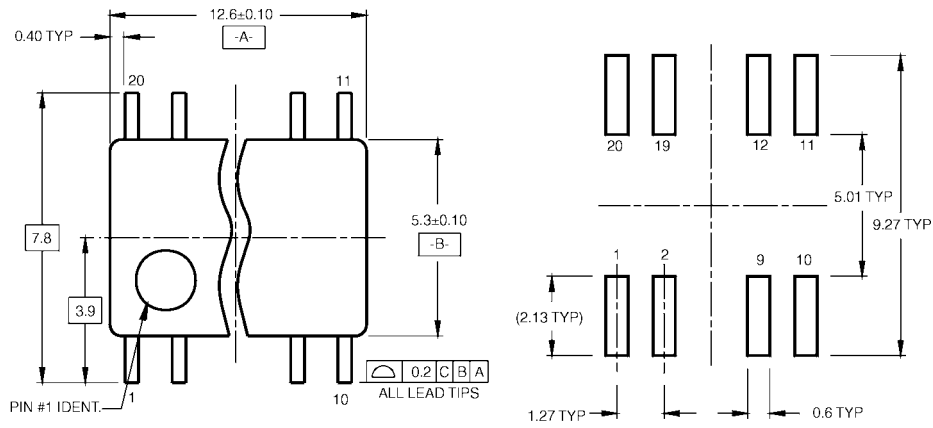
**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

**Physical Dimensions** inches (millimeters) unless otherwise noted

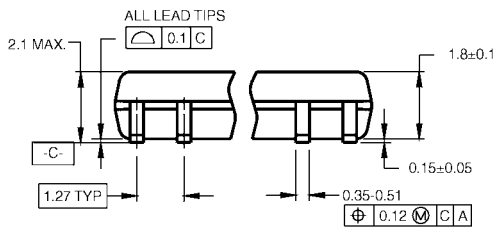


**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Body  
Package Number M20B**

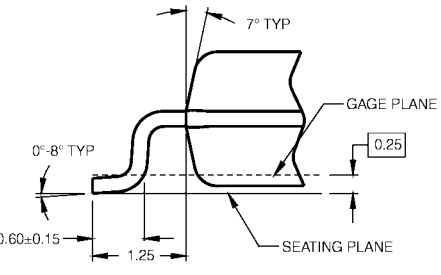
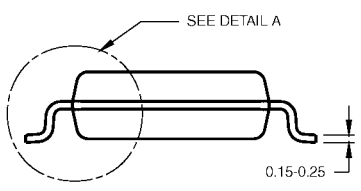
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS



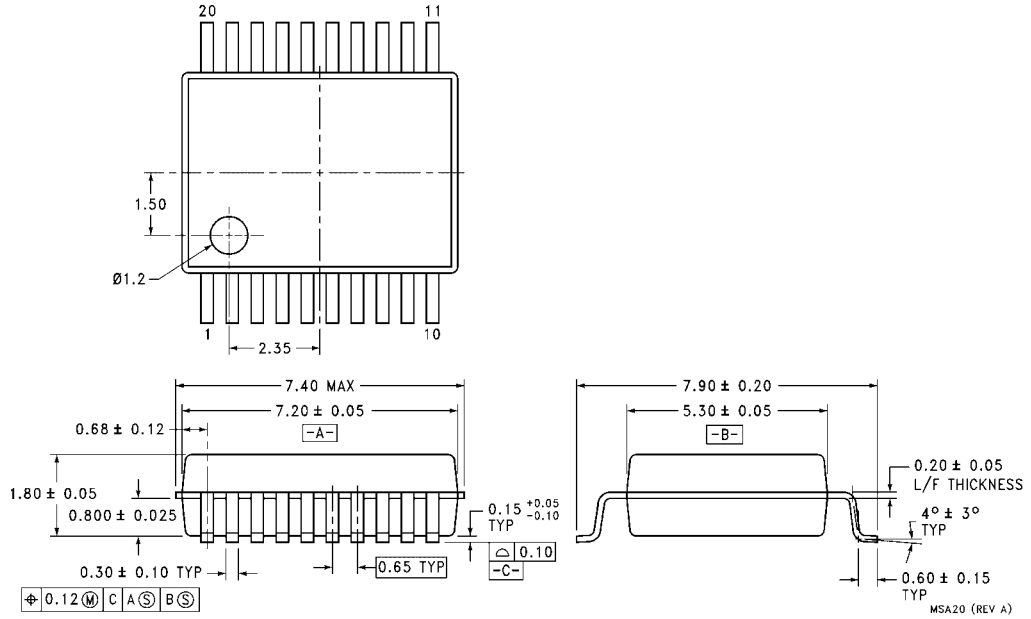
DETAIL A

- NOTES:
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
  - B. DIMENSIONS ARE IN MILLIMETERS.
  - C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

**20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

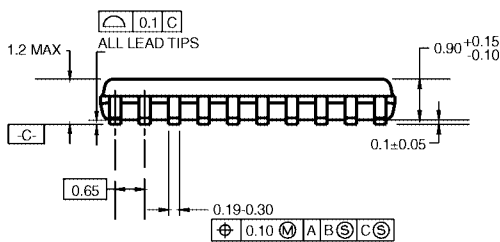
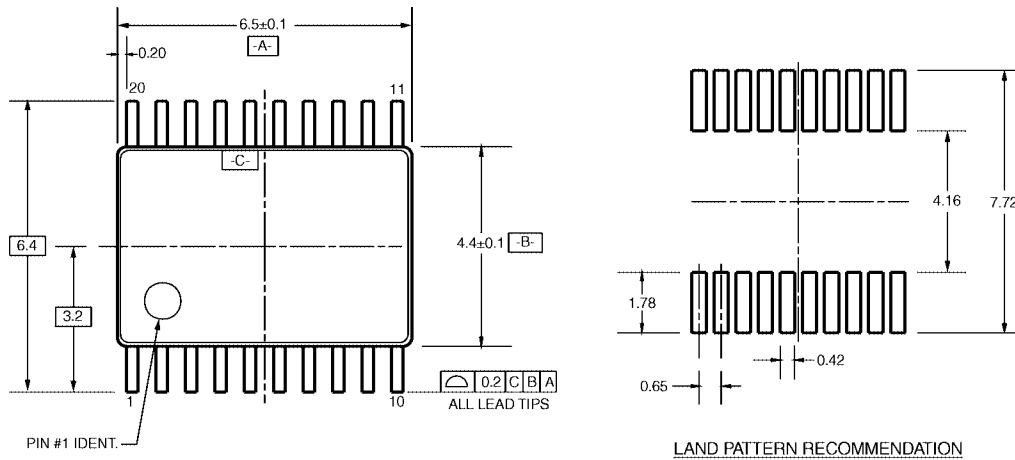
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide  
Package Number MSA20**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)

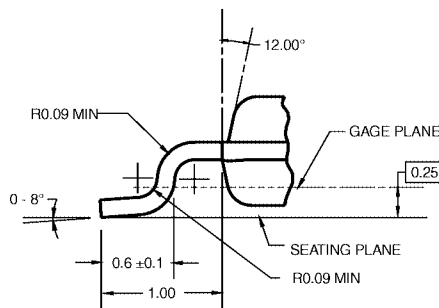


DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1



**DETAIL A**

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**

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