

June 1994

Monolithic CMOS Analog Switches

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- ON-Resistance <math><35\Omega</math>
- Low Power Consumption ($P_D <35\mu W</math>)$
- Fast Switching Action
 - $t_{ON} <150ns</math>$
 - $t_{OFF} <100ns</math>$
- Low Charge Injection
- DG401/883 Dual SPST; Replaces HI-5041/883
- DG403/883 Dual SPDT; Replaces DG190/883B, IH5043/883B, IH5151/883B, HI-5051/883, HI-5043/883B
- DG405/883 Dual DPST; Replaces DG184/883B, HI-5045/883, IH5145/883B
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems

Description

The DG401/883, DG403/883 and DG405/883 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance (<math><35\Omega</math>) and fast switch time ($t_{ON} <150ns</math>). Low charge injection simplifies sample and hold applications.$

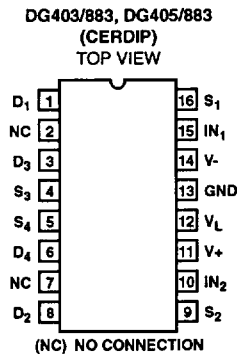
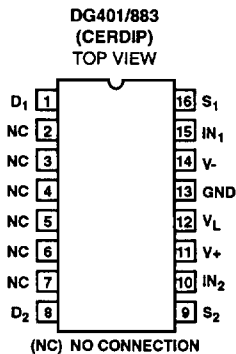
The improvements in the DG401/403/405/883 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from $\pm 5V$ to $\pm 17V$.

The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a $\pm 15V$ analog input range. The three different devices provide the equivalent of two SPST (DG401/883), two SPDT (DG403/883) or two DPST (DG405/883) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

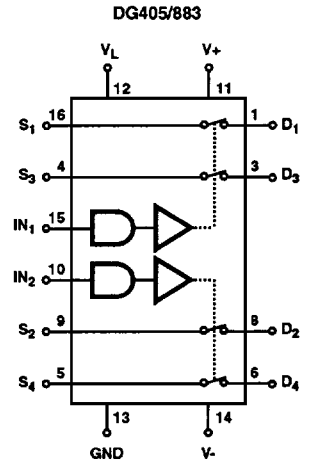
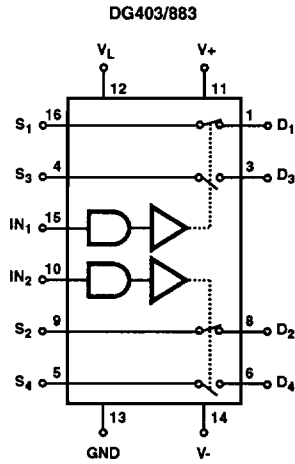
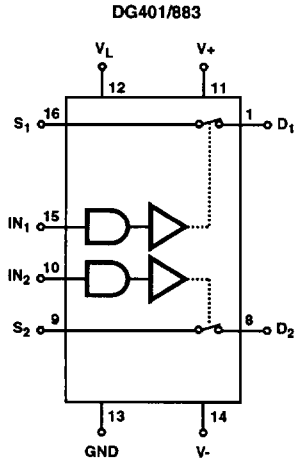
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG401AK/883	-55°C to +125°C	16 Lead CerDIP
DG403AK/883	-55°C to +125°C	16 Lead CerDIP
DG405AK/883	-55°C to +125°C	16 Lead CerDIP

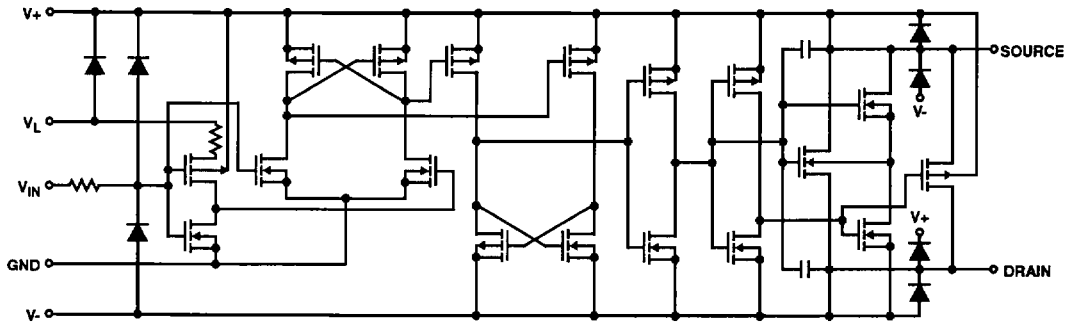
Pinouts



Functional Diagrams



Schematic Diagram



Truth Table

LOGIC	DG401/883	DG403/883		DG405/883
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" $\leq 0.8V$. Logic "1" $\geq 2.4V$.

Specifications DG401/883, DG403/883, DG405/883

Absolute Maximum Ratings

V+ to V-+44.0V
GND to V- 25V
V _L (GND - 0.3V) to (V _{C+}) +0.3V
Digital Inputs (Note 1), V _S , V _D (V-) -2V to (V+) + 2V or 30mA, Which ever Occurs First
Continuous (Any Terminal) Current, (Note 1) ±30mA
Peak Current, S or D (Note 1) (Pulsed 1ms, 10% Duty Cycle) ±100mA
Storage Temperature Range (A Suffix) -65°C to +125°C
Lead Temperature (Soldering 10s) +300°C

Reliability Information

Thermal Resistance (Max)	θ_{JC}	θ_{JA}
CerDIP Package	18°C/W	75°C/W
Operating Temperature (A Suffix) -55°C to +125°C	
Junction Temperature (CerDIP) +175°C	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ±20V Max	Input High Voltage 2.4V Min
Operating Temperature Range -55°C to +125°C	Input Rise and Fall Time 20ns
Input Low Voltage 0.8V Max		

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at V+ = +15V, V- = -15V, V_L = 5V, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Drain-to-Source ON Resistance	R _{DS(ON)}	V+ = +13.5V, V- = -13.5V, I _S = -10mA, V _D = ±10V	1	+25°C	-	35	Ω
			2, 3	+125°C, -55°C	-	45	Ω
Delta Drain-to-Source ON Resistance	Delta R _{DS(ON)}	V+ = +16.5V, V- = -16.5V, I _S = -10mA, V _D = +5V, 0V, -5V	1	+25°C	-	3	Ω
			2, 3	+125°C, -55°C	-	5	Ω
Source OFF Leakage Current	I _{S(OFF)}	V+ = +16.5V, V- = -16.5V, V _S = -15.5V, V _D = +15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
		V+ = +16.5V, V- = -16.5V, V _S = +15.5V, V _D = -15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
Drain OFF Leakage Current	I _{D(OFF)}	V+ = +16.5V, V- = -16.5V, V _S = -15.5V, V _D = +15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
		V+ = +16.5V, V- = -16.5V, V _S = +15.5V, V _D = -15.5V	1	+25°C	-	±0.25	nA
			2	+125°C	-	±20	nA
Channel ON Leakage Current	I _{D(ON)} + I _{S(ON)}	V+ = +16.5V, V- = -16.5V, V _S = V _D = ±15.5V	1	+25°C	-	±0.4	nA
			2	+125°C	-	±40	nA
Low Level Input Current	I _{IL}	V _{IN} Under Test = 0.8V, All Others = 2.4V	1, 2	+25°C, +125°C	-	±1.0	μA
High Level Input Current	I _{IH}	V _{IN} Under Test = 2.4V, All Others = 0.8V	1, 2	+25°C, +125°C	-	±1.0	μA
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5V, V _{IN} = 0V or 5.0V	1	+25°C	-	+1.0	μA
			2, 3	+125°C, -55°C	-	+5.0	μA
Negative Supply Current	I-	V+ = +16.5V, V- = -16.5V, V _{IN} = 0V or 5.0V	1	+25°C	-	-1.0	μA
			2, 3	+125°C, -55°C	-	-5.0	μA
Logic Supply Current	I _L	V+ = +16.5V, V- = -16.5V, V _{IN} 0V or 5V	1	+25°C	-	+1.0	μA
			2, 3	+125°C, -55°C	-	+5.0	μA
Ground Current	I _{GND}	V+ = +16.5V, V- = -16.5V, V _{IN} 0V or 5V	1	+25°C	-	-1.0	μA
			2, 3	+125°C, -55°C	-	-5.0	μA

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CMOS ANALOG
SWITCHES

Specifications DG401/883, DG403/883, DG405/883

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at $V_+ = +15V$, $V_- = -15V$, $V_L = 5V$, Unless Otherwise Specified

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Turn On Time	t_{ON}	$R_L = 300\Omega$, $C_L = 35pF$	9	+25°C	-	150	ns
			10, 11	+125°C, -55°C	-	275	ns
Turn Off Time	t_{OFF}	$R_L = 300\Omega$, $C_L = 35pF$	9	+25°C	-	100	ns
			10	+125°C	-	250	ns
			11	-55°C	-	175	ns
Break-Before-Make Time Delay (DG403 Only)	t_D	$R_L = 300\Omega$, $C_L = 35pF$	9	+25°C	10	150	ns

NOTE:

1. Signals on S_x , D_x , or IN_x exceeding V_+ or V_- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 3 Intentionally Left Blank.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C and D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

2150 μ m x 1720 μ m x 485 \pm 25 μ m

METALLIZATION:

Type: Si - Al

Thickness: 12k \AA \pm 1k \AA

GLASSIVATION:

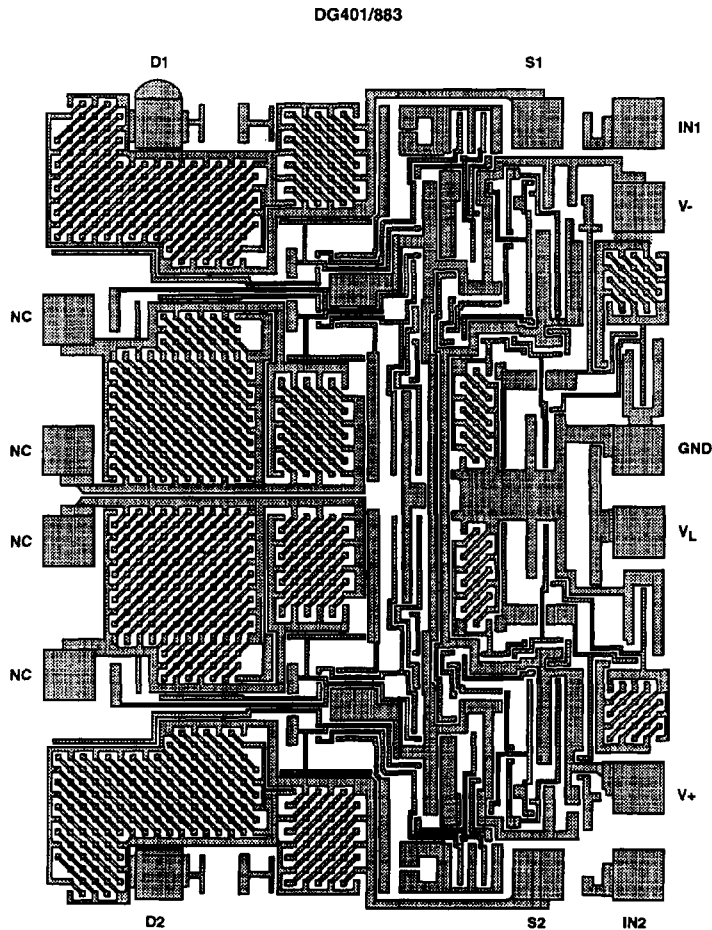
Type: Nitride

Thickness: 8k \AA \pm 1k \AA

WORST CASE CURRENT DENSITY:

1.5 x 10⁵ A/cm²

Metallization Mask Layout



DG403/883, DG405/883

Die Characteristics

DIE DIMENSIONS:

2150 μm x 1720 μm x 485 \pm 25 μm

METALLIZATION:

Type: Si - Al

Thickness: 12k \AA \pm 1k \AA

GLASSIVATION:

Type: Nitride

Thickness: 8k \AA \pm 1k \AA

WORST CASE CURRENT DENSITY:

1.5 x 10⁵ A/cm²

Metallization Mask Layout

DG403/883, DG405/883

