

# CD74HC175, CD74HCT175

## High Speed CMOS Logic Quad D-Type Flip-Flop with Reset

August 1997

### Features

- Common Clock and Asynchronous Reset on Four D-Type Flip-Flops
- Positive Edge Pulse Triggering
- Complementary Outputs
- Buffered Inputs
- Typical  $f_{MAX} = 50$  MHz at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC175 and CD74HCT175 are high speed Quad D-type Flip-Flops with individual D-inputs and Q,  $\bar{Q}$  complementary outputs. The devices are fabricated using silicon gate CMOS technology. They have the low power consumption advantage of standard CMOS ICs and the ability to drive 10 LSTTL devices.

Information at the D input is transferred to the Q,  $\bar{Q}$  outputs on the positive going edge of the clock pulse. All four Flip-Flops are controlled by a common clock (CP) and a common reset (MR). Resetting is accomplished by a low voltage level independent of the clock. All four Q outputs are reset to a logic 0 and all four  $\bar{Q}$  outputs to a logic 1.

### Ordering Information

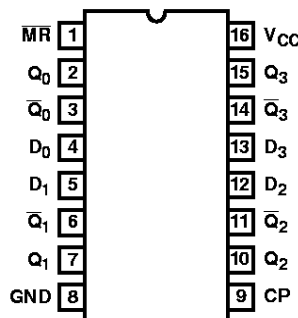
PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC175E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT175E	-55 to 125	16 Ld PDIP	E16.3
CD74HC175M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT175M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT175W	-55 to 125	Wafer	

NOTE:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

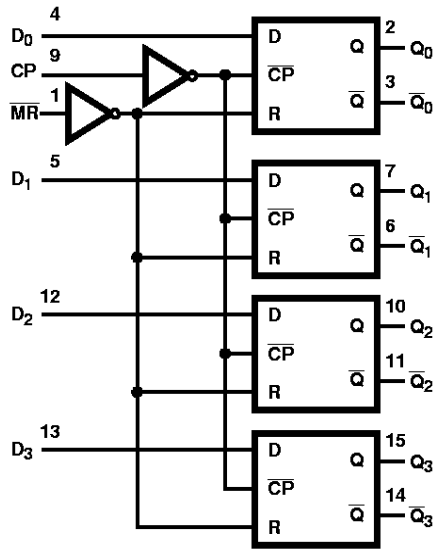
### Pinout

CD74HC175, CD74HCT175  
(PDIP, SOIC)  
TOP VIEW



# CD74HC175, CD74HCT175

## Functional Diagram

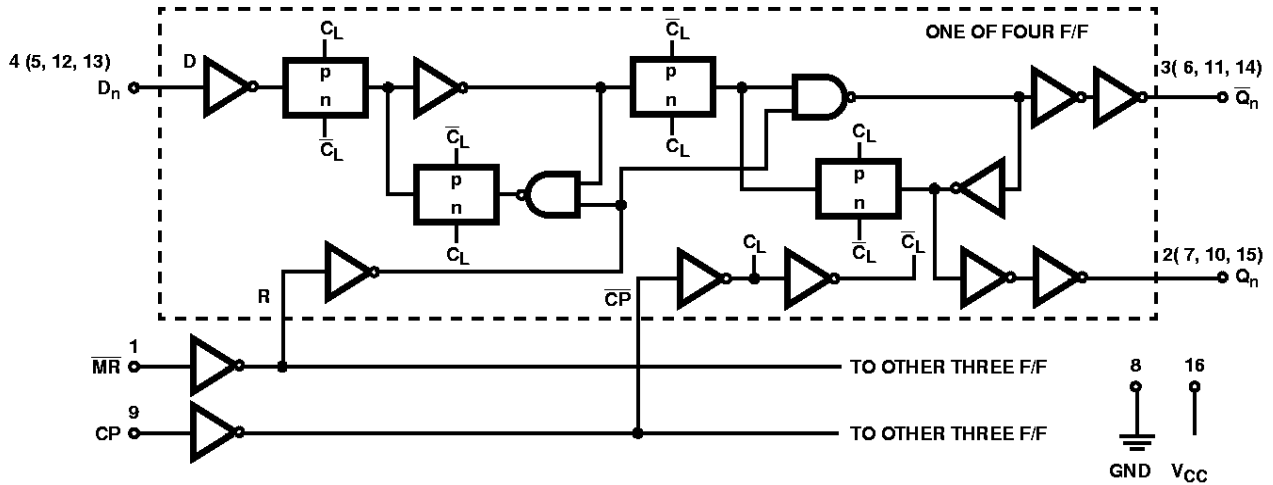


TRUTH TABLE

INPUTS			OUTPUTS	
RESET ( $\overline{MR}$ )	CLOCK CP	DATA $D_n$	$Q_n$	$\overline{Q}_n$
L	X	X	L	H
H	$\uparrow$	H	H	L
H	$\uparrow$	L	L	H
H	L	X	$Q_0$	$\overline{Q}_0$

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care,  $\uparrow$  = Transition from Low to High Level,  $Q_0$  = Level Before the Indicated Steady-State Input Conditions Were Established.

## Logic Diagram



## CD74HC175, CD74HCT175

### Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

### Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	110
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$ (SOIC - Lead Tips Only)

### Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

### DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO +85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	-5.2	6	5.48	-	-	5.34	-	5.2	-	V
			0.02	2	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu A$

## CD74HC175, CD74HCT175

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO +85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ to GND	0	5.5	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	$\mu A$
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	$\Delta I_{CC}$	$V_{CC}$ -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	$\mu A$

NOTE:

- For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.
- Die for this part number is available which meets all electrical specifications.

### HCT Input Loading Table

INPUT	UNIT LOADS
$\overline{MR}$	1
CP	0.60
D	0.15

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu A$  max at 25°C.

### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Clock Pulse Width	$t_w$	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
$\overline{MR}$ Pulse Width	$t_w$	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns

## CD74HC175, CD74HCT175

### Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Setup Time, Data to Clock	t <sub>SU</sub>	-	2	80	-	-	100	-	120	-	ns
			4.5	16	-	-	20	-	24	-	ns
			6	14	-	-	17	-	20	-	ns
Hold Time, Data to Clock	t <sub>H</sub>	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
Removal Time, $\overline{MR}$ to Clock	t <sub>REM</sub>	-	2	5	-	-	5	-	5	-	ns
			4.5	5	-	-	5	-	5	-	ns
			6	5	-	-	5	-	5	-	ns
Clock Frequency	f <sub>MAX</sub>	-	2	6	-	-	5	-	4	-	MHz
			4.5	30	-	-	25	-	20	-	MHz
			6	35	-	-	29	-	23	-	MHz

#### HCT TYPES

Clock Pulse Width	t <sub>w</sub>	-	4.5	20	-	-	25	-	30	-	ns
$\overline{MR}$ Pulse Width	t <sub>w</sub>	-	4.5	20	-	-	25	-	30	-	ns
Setup Time Data to Clock	t <sub>SU</sub>	-	4.5	20	-	-	25	-	30	-	ns
Hold Time Data to Clock	t <sub>H</sub>	-	4.5	5	-	-	5	-	5	-	ns
Removal Time $\overline{MR}$ to Clock	t <sub>REM</sub>	-	4.5	5	-	-	5	-	5	-	ns
Clock Frequency	f <sub>MAX</sub>	-	4.5	25	-	-	20	-	16	-	MHz

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay, Clock to Q or $\overline{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
		C <sub>L</sub> = 15pF	5	14	-	-	-	ns
Propagation Delay, $\overline{MR}$ to Q or $\overline{Q}$	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
			6	-	30	37	45	ns
		C <sub>L</sub> = 15pF	5	14	-	-	-	ns
Output Transition Times	t <sub>TLH</sub> , t <sub>THL</sub>	C <sub>L</sub> = 50pF	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	C <sub>IN</sub>	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 6, 7)	C <sub>PD</sub>	-	5	65	-	-	-	pF

## CD74HC175, CD74HCT175

### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C to 85°C	-55°C to 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HCT TYPES</b>								
Propagation Delay, Clock to Q or $\bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	33	41	50	ns
			5	13	-	-	-	ns
Propagation Delay, MR to Q or $\bar{Q}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	35	44	53	ns
			5	17	-	-	-	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Input Capacitance	$C_{IN}$	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 6, 7)	$C_{PD}$	-	5	67	-	-	-	pF

**NOTES:**

6.  $C_{PD}$  is used to determine the dynamic power consumption, per flip-flop.
7.  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

### Test Circuits and Waveforms

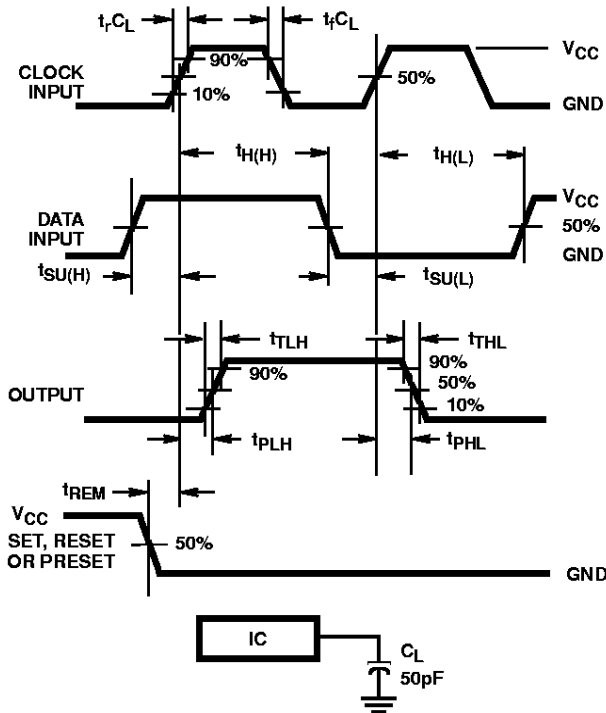


FIGURE 3. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

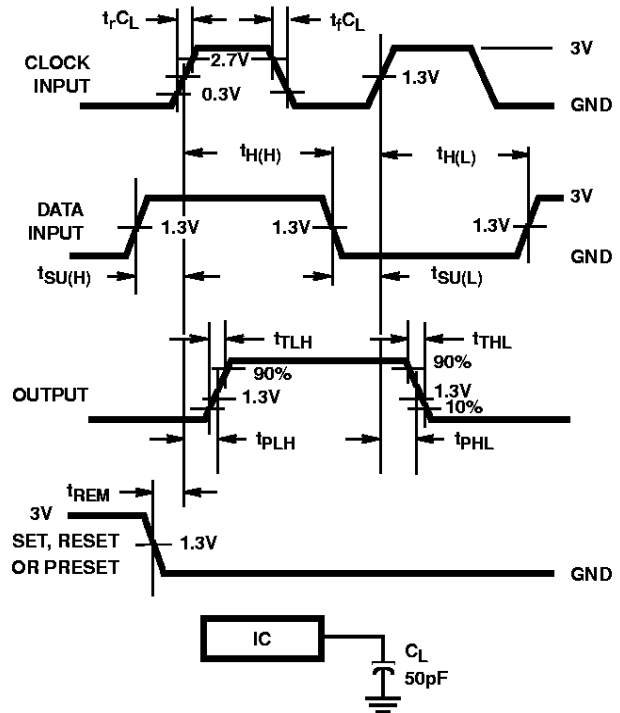


FIGURE 4. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS