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# FSA3157B

## Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

### Features

- Useful in Both Analog and Digital Applications
- Ultra-Small, MicroPak™ Leadless Package
- Low On Resistance: <math><10 \Omega</math> Typical at 3.3 V  $V_{CC}$
- Broad  $V_{CC}$  Operating Range: 1.65 V to 5.5 V
- Rail-to-Rail Signal Handling
- Power-Down, High-Impedance Control Input
- Over-Voltage Tolerance of Control Input to 7.0 V
- Break-Before-Make Enable Circuitry
- 250 MHz, 3 dB Bandwidth

### Description

The FSA3157B is a high-performance, Single-Pole / Double-Throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5 V  $V_{CC}$  operating range. The control input tolerates voltages up to 5.5 V, independent of the  $V_{CC}$  operating range.

### Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSA3157BL6X	-40 to +85°C	7G	6-Lead, MicroPak™ 1.0 mm Wide Package	5000 Units on Tape and Reel
FSA3157BFHX	-40 to +85°C	7G	6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch	5000 Units on Tape and Reel

## Analog Symbols

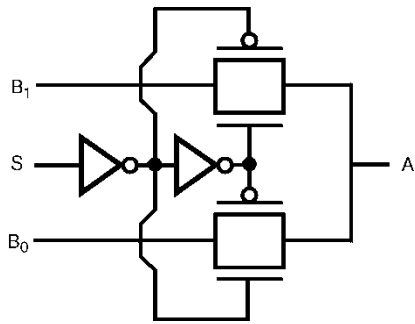


Figure 1. Logic Symbol

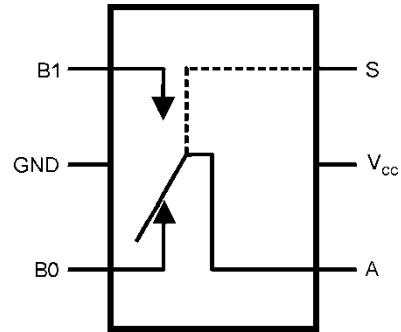


Figure 2. Analog Symbol

## Pin Configuration

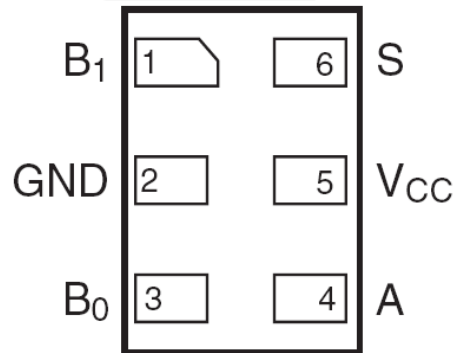


Figure 3. Pad Assignments

## Function Table

Input (S)	Function
Logic Level LOW	B <sub>0</sub> Connected to A
Logic Level HIGH	B <sub>1</sub> Connected to A

## Pin Descriptions

Pin#	Name	Description
1	B <sub>1</sub>	Data Ports
2	GND	Ground
3	B <sub>0</sub>	Data Ports
4	A	Data Ports
5	V <sub>CC</sub>	Power Supply
6	S	Control Input

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	7.0	V
$V_S$	DC Switch Voltage <sup>(1)</sup>	-0.5	$V_{CC}+0.5$	V
$V_{IN}$	DC Input Voltage <sup>(1)</sup>	-0.5	7.0	V
$I_{IK}$	DC Input Diode Current at $V_{IN} < 0$ V	-50		mA
$I_{OUT}$	DC Output Current		128	mA
$I_{CC/GND}$	DC $V_{CC}$ or Ground Current		$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Junction Temperature Under Bias		+150	°C
$T_L$	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
$P_D$	Power Dissipation at +85°C		180	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5 kV

### Note:

- Input and output negative voltage ratings may be exceeded if input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit	
$V_{CC}$	Supply Voltage Operating	1.65	5.50	V	
$V_{IN}$	Control Input Voltage <sup>(2)</sup>	0	$V_{CC}$	V	
$V_{IN}$	Switch Input Voltage <sup>(2)</sup>	0	$V_{CC}$	v	
$V_{OUT}$	Output Voltage <sup>(2)</sup>	0	$V_{CC}$	V	
$T_A$	Operating Temperature	-40	+85	°C	
$t_r, t_f$	Input Rise and Fall Time	Control Input $V_{CC}=2.3$ V– $3.6$ V	0	10	ns/V
		Control Input $V_{CC}=4.5$ V– $5.5$ V	0	5	

### Note:

- Control input must be held HIGH or LOW; it must not float.

## Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage		1.65 to 1.95	0.75 V <sub>CC</sub>			0.75 V <sub>CC</sub>		V
			2.30 to 5.50	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		
V <sub>IL</sub>	Low Level Input Voltage		1.65 to 1.95			0.25 V <sub>CC</sub>		0.25 V <sub>CC</sub>	V
			2.30 to 5.50			0.3 V <sub>CC</sub>		0.3 V <sub>CC</sub>	
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	0 to 5.50		±0.05	±0.1		±1	μA
I <sub>OFF</sub>	Off State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	1.65 to 5.50		±0.05	±0.10		±1.00	μA
R <sub>ON</sub>	Switch On Resistance <sup>(3)</sup>	V <sub>IN</sub> =0 V, I <sub>O</sub> =30 mA	4.50		3.0	7.0		7.0	Ω
		V <sub>IN</sub> =2.4 V, I <sub>O</sub> =-30 mA			5.0	12.0		12.0	
		V <sub>IN</sub> =4.5 V, I <sub>O</sub> =-30 mA			7.0	15.0		15.0	
		V <sub>IN</sub> =0 V, I <sub>O</sub> =24 mA	3.00		4.0	9.0		9.0	
		V <sub>IN</sub> =3 V, I <sub>O</sub> =-24 mA			10.0	20.0		20.0	
		V <sub>IN</sub> =0 V, I <sub>O</sub> =8 mA	2.30		5.0	12.0		12.0	
		V <sub>IN</sub> =2.3 V, I <sub>O</sub> =-8 mA			13.0	30.0		30.0	
		V <sub>IN</sub> =0 V, I <sub>O</sub> =4 mA	1.65		6.5	20.0		20.0	
V <sub>IN</sub> =1.65 V, I <sub>O</sub> =-4 mA		17.0		50.0		50.0			
I <sub>CC</sub>	Quiescent Supply Current: All Channels On or Off	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0	5.50			1		10	μA
	Analog Signal Range		V <sub>CC</sub>	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V
R <sub>RANGE</sub>	On Resistance Over Signal Range <sup>(3,7)</sup>	I <sub>A</sub> =-30 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	4.50					25	Ω
		I <sub>A</sub> =-24 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.00					50	
		I <sub>A</sub> =-8 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.30					100	
		I <sub>A</sub> =-4 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.65					300	
ΔR <sub>ON</sub>	On Resistance Match Between Channels <sup>(3,4)</sup>	I <sub>A</sub> =-30 mA, V <sub>Bn</sub> =3.15	4.50		0.15				Ω
		I <sub>A</sub> =-24 mA, V <sub>Bn</sub> =2.1	3.00		0.20				
		I <sub>A</sub> =-8 mA, V <sub>Bn</sub> =1.6	2.30		0.50				
		I <sub>A</sub> =-4 mA, V <sub>Bn</sub> =1.15	1.65		0.50				
R <sub>FLAT</sub>	On Resistance Flatness <sup>(3,4,6)</sup>	I <sub>A</sub> =-30 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	5.00		6				Ω
		I <sub>A</sub> =-24 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.00		12				
		I <sub>A</sub> =-8 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.50		28				
		I <sub>A</sub> =-4 mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.80		125				

### Notes:

- Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
- Parameter is characterized, but not tested in production.
- ΔR<sub>ON</sub> = R<sub>ON</sub> maximum – R<sub>ON</sub> minimum measured at identical V<sub>CC</sub>, temperature, and voltage levels.
- Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
- Guaranteed by design.

## AC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> =+25°C			T <sub>A</sub> =-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PLH</sub> , t <sub>PLH</sub>	Propagation Delay Bus-to-Bus <sup>(8)</sup>	V <sub>IN</sub> =OPEN	1.65 to 1.95			3.5		3.5	ns	Figure 10 Figure 11
			2.30 to 2.70			1.2		1.2		
			3.00 to 3.60			0.8		0.8		
			4.05 to 5.50			0.3		0.3		
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time Turn-On Time (A to B <sub>n</sub> )	V <sub>IN</sub> =2X V <sub>CC</sub> for t <sub>PZL</sub> V <sub>IN</sub> =0 V for t <sub>PZH</sub>	1.65 to 1.95	7.0		23.0		24.0	ns	Figure 10 Figure 11
			2.30 to 2.70	3.5		13.0		14.0		
			3.00 to 3.60	2.5		6.9		7.6		
			4.50 to 5.50	1.7		5.2		5.7		
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time Turn-Off Time (A Port to B Port)	V <sub>IN</sub> =2X V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>IN</sub> =0 V for t <sub>PHZ1</sub>	1.65 to 1.95	3.0		12.5		13.0	ns	Figure 10 Figure 11
			2.30 to 2.70	2.0		7.0		7.5		
			3.00 to 3.60	1.5		5.0		5.3		
			4.50 to 5.50	0.8		3.5		3.8		
t <sub>BBM</sub>	Break-Before-Make Time <sup>(9)</sup>		1.65 to 1.95	0.5			0.5	ns	Figure 12	
			2.30 to 2.70	0.5			0.5			
			3.00 to 3.60	0.5			0.5			
			4.50 to 5.50	0.5			0.5			
Q	Charge Injection <sup>(9)</sup>	C <sub>L</sub> =0.1 nF, V <sub>GEN</sub> =0 V	5.00		7			pC	Figure 13	
		R <sub>GEN</sub> =0 Ω	3.30		3					
OIRR	Off Isolation <sup>(10)</sup>	R <sub>L</sub> =50 Ω, f=10 MHz	1.65 to 5.50		-57			dB	Figure 14	
Xtalk	Crosstalk	R <sub>L</sub> =50 Ω, f=10 MHz	1.65 to 5.50		-54			dB	Figure 15	
BW	-3 dB Bandwidth	R <sub>L</sub> =50 Ω	1.65 to 5.50		250			MHz	Figure 18	
THD	Total Harmonic Distortion <sup>(9)</sup>	R <sub>L</sub> =600 Ω, 0.5 V <sub>PP</sub> , f=600 Hz to 20 KHz	5.00		.011			%		

### Notes:

8. This parameter is guaranteed by design, but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub> / V<sub>Bn</sub>].

## Capacitance

T<sub>A</sub> = +25°C, f=1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typical	Unit	Figure
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> =0 V	2.3	pF	
C <sub>IO-B</sub>	B Port Off Capacitance	V <sub>CC</sub> =5.0 V	6.5	pF	Figure 16
C <sub>IOA-ON</sub>	A Port Capacitance, Switch Enabled	V <sub>CC</sub> =5.0 V	18.5	pF	Figure 17

## Typical Performance Characteristics

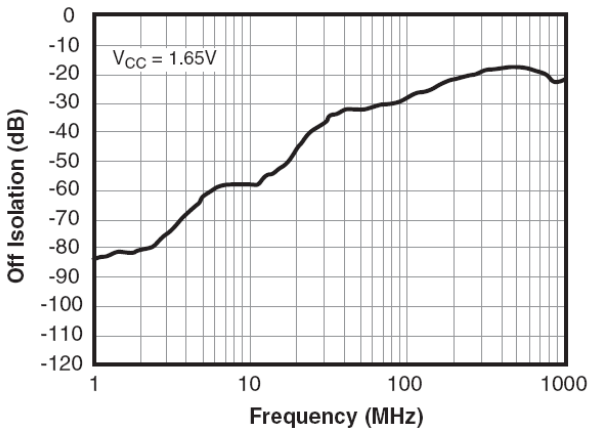


Figure 4. Off Isolation,  $V_{CC}=1.65 V$

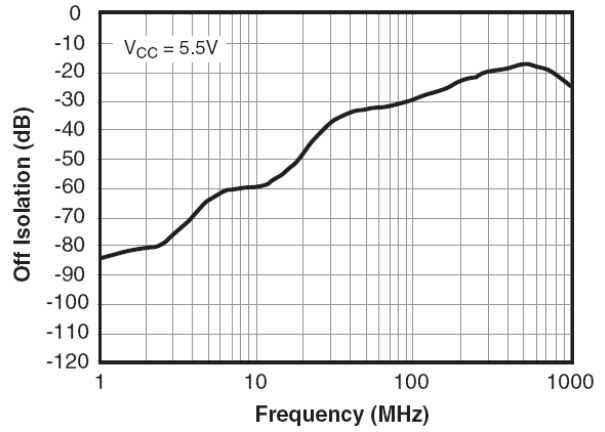


Figure 5. Off Isolation,  $V_{CC}=5.5 V$

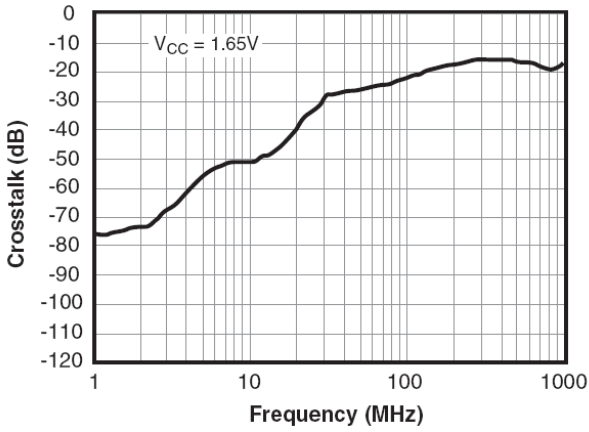


Figure 6. Crosstalk,  $V_{CC}=1.65 V$

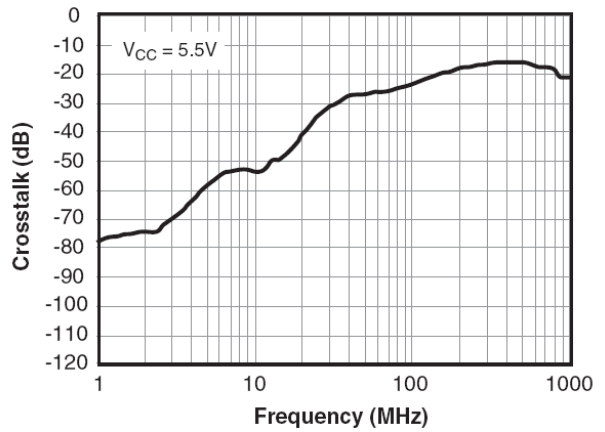


Figure 7. Crosstalk,  $V_{CC}=5.5 V$

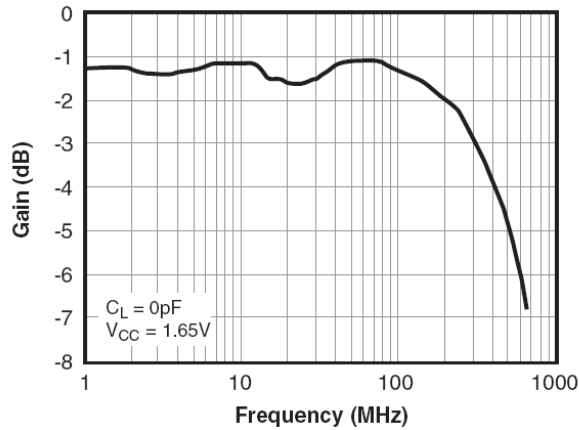


Figure 8. Bandwidth,  $V_{CC}=1.65 V$

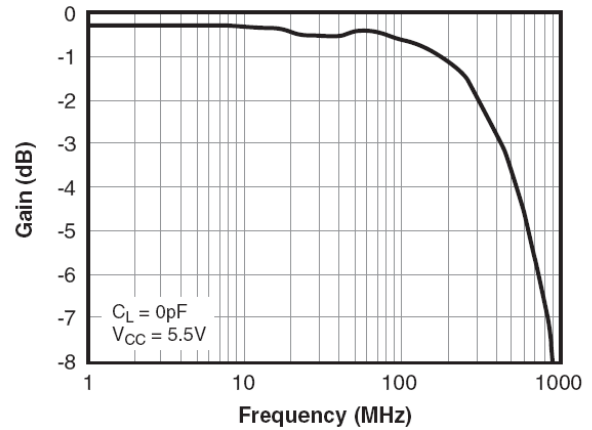
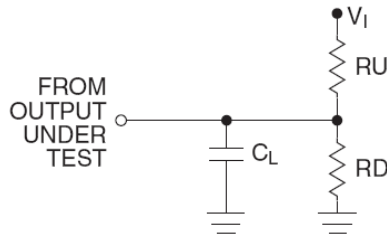


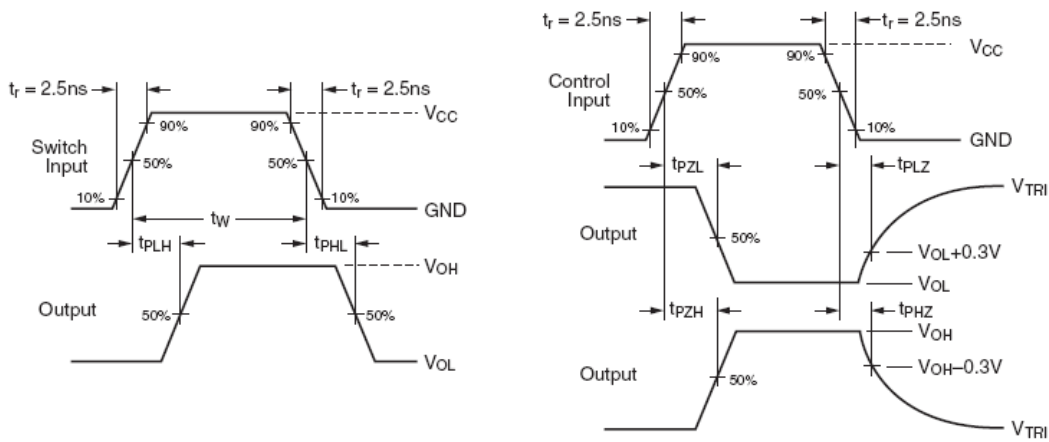
Figure 9. Bandwidth,  $V_{CC}=5.5 V$

## AC Loading and Waveforms

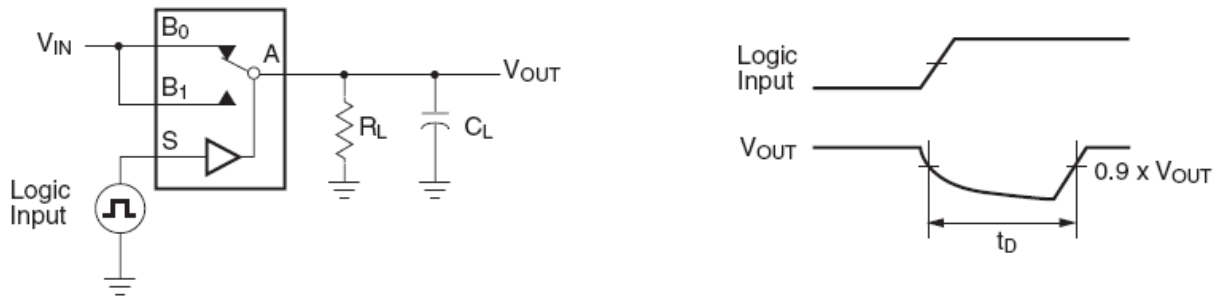


**Notes:**  
 Input driven by 50Ω source terminated in 50Ω  
 $C_L$  includes load and stray capacitance  
 Input PRR = 1.0 MHz;  $t_W = 500$  ns

**Figure 10. AC Test Circuit**



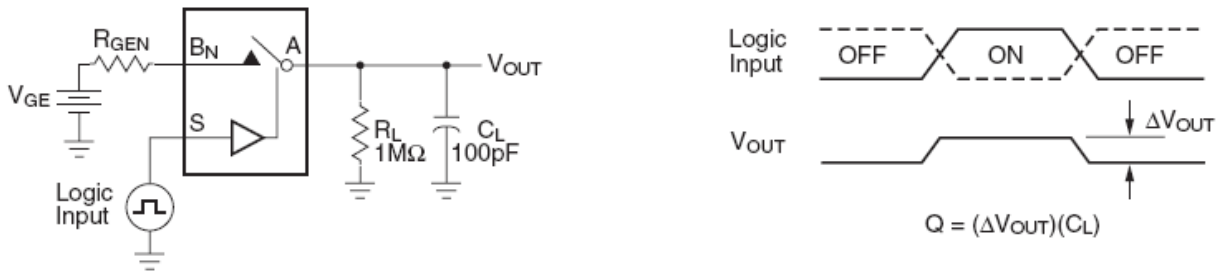
**Figure 11. AC Waveforms**



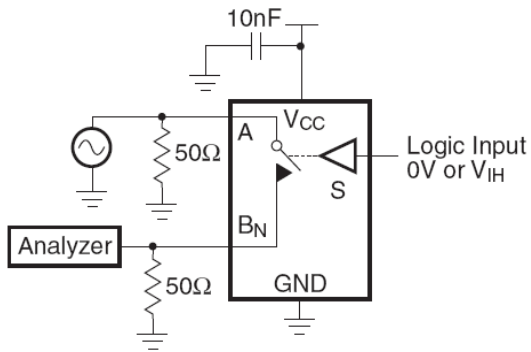
**Figure 12. Break-Before-Make Interval Timing**



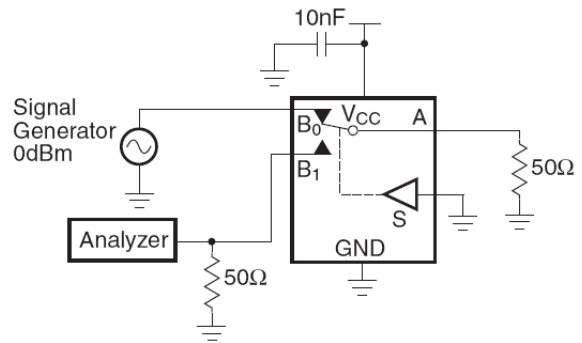
**AC Loading and Waveforms** (Continued)



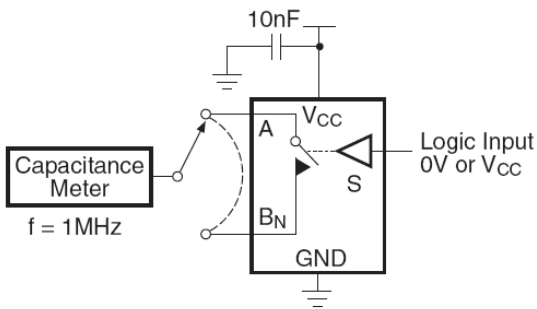
**Figure 13. Charge Injection Test**



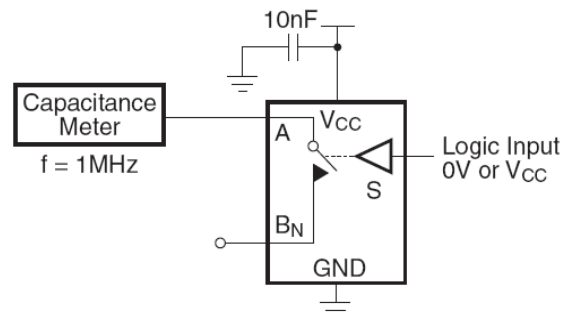
**Figure 14. Off Isolation**



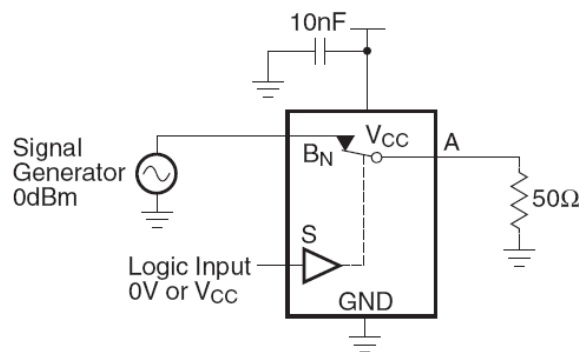
**Figure 15. Crosstalk**



**Figure 16. Channel Off Capacitance**

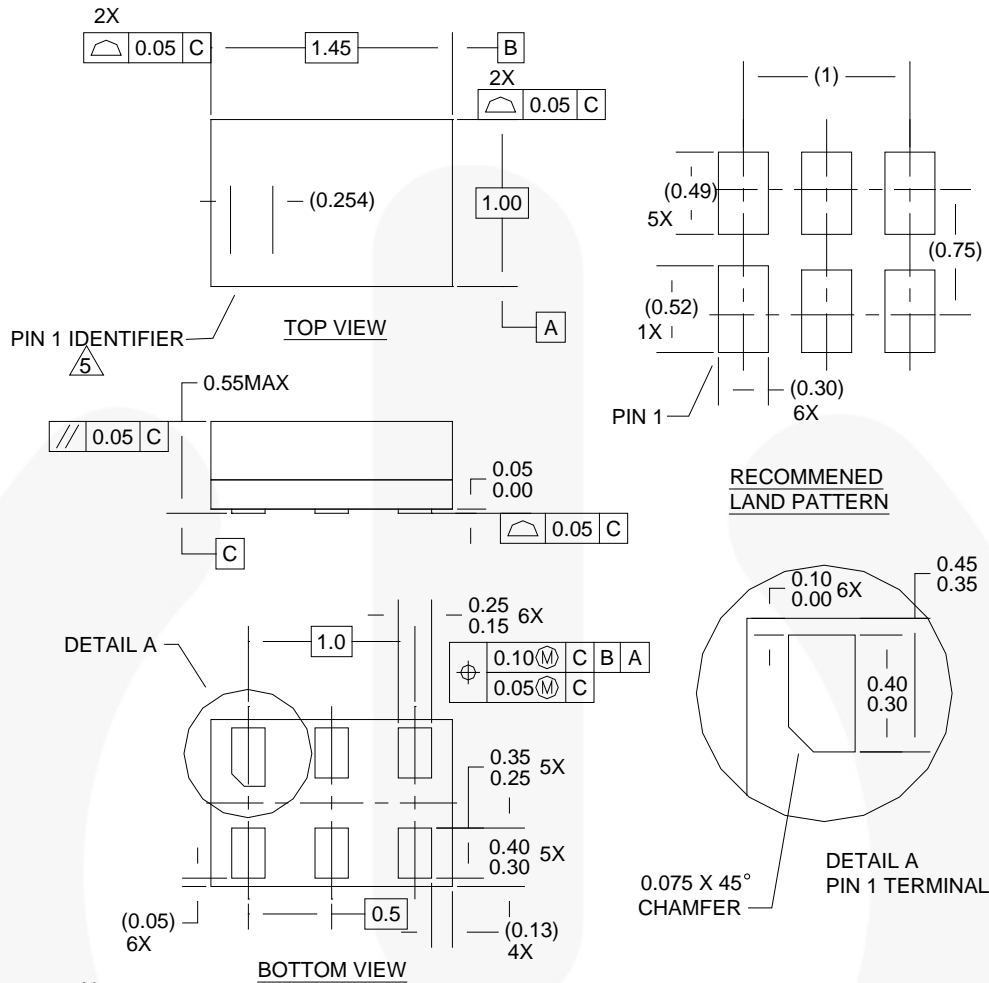


**Figure 17. Channel On Capacitance**



**Figure 18. Bandwidth**

## Physical Dimensions



**Notes:**

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

**Figure 19. 6-Lead, MicroPak™ 1.0 mm Wide Package**

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

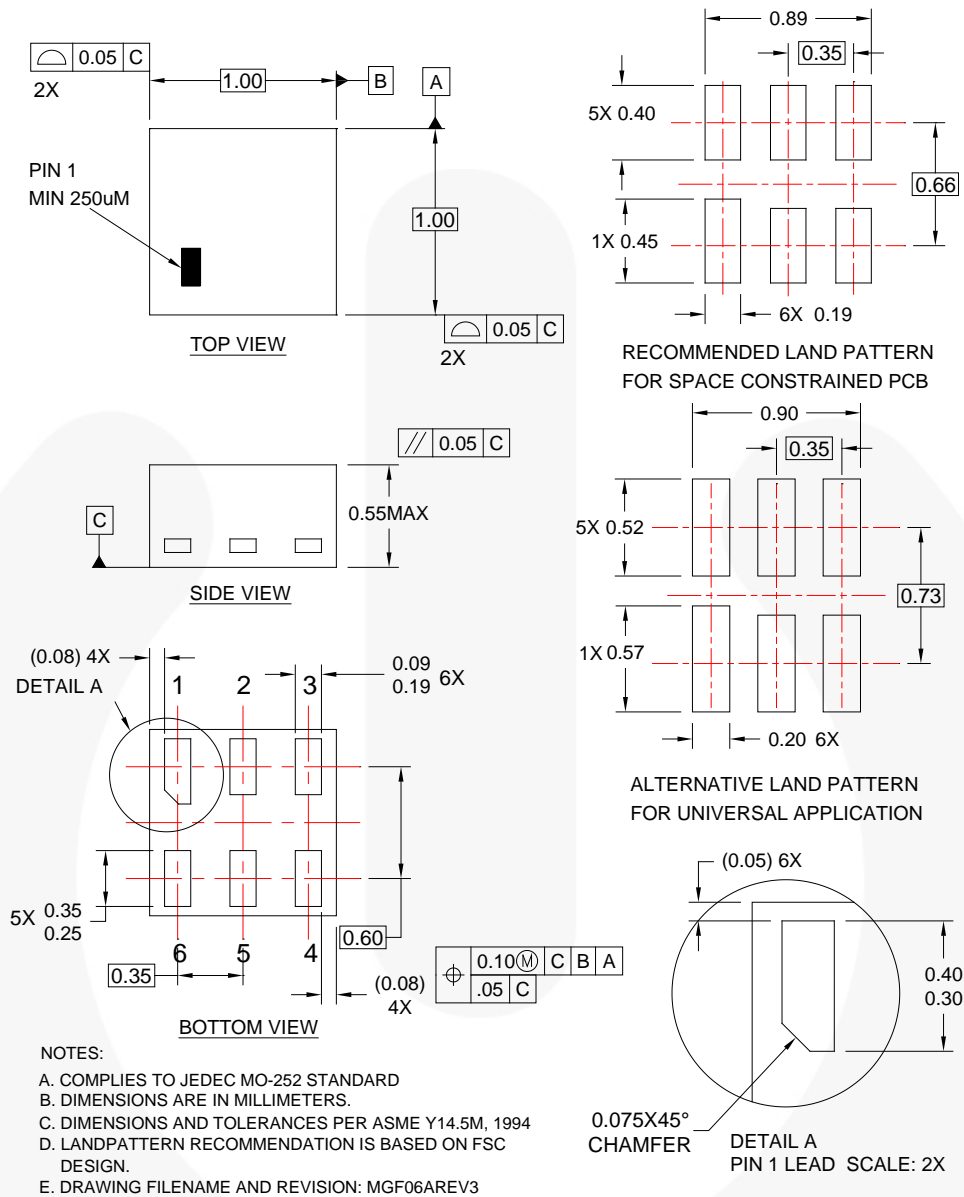
Always visit Fairchild Semiconductor's online packaging area for the most recent package drawings:  
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### Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/products/logic/pdf/micropak\\_tr.pdf](http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf)

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## Physical Dimensions



**Figure 20. 6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch**

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[http://www.fairchildsemi.com/packaging/MicroPAK2\\_6L\\_tr.pdf](http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf).

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed



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| BitSiC™  | Global Power Resource®                         | Programmable Active Droop™            | TinyBoost®  |
| Build it Now™  | GreenBridge™                                   | QFET®                                 | TinyBuck®   |
| CorePLUS™  | Green FPS™                                     | QST™                                  | TinyCalc™   |
| CorePOWER™   | Green FPS™ e-Series™                           | Quiet Series™                         | TinyLogic®  |
| CROSSVOLT™   | Gmax™  | RapidConfigure™                       | TINYOPTO™   |
| CTL™   | GTO™   | Saving our world, 1mW/W/kW at a time™ | TinyPower™  |
| Current Transfer Logic™  | IntelliMAX™                                    | SignalWise™                           | TinyPWM™  |
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