

5V ECL Differential Data and Clock D Flip-Flop

Features

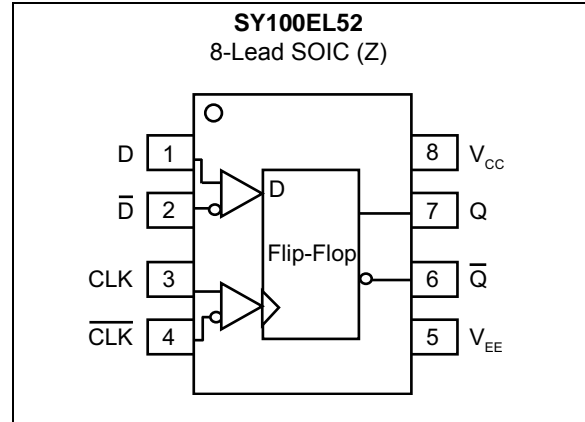
- 365 ps Propagation Delay (typical)
- 2.8 GHz Toggle Frequency (typical)
- Internal 75 k Ω Input Pull-Down Resistors
- Available in 8-Lead SOIC Package

General Description

The SY100EL52 is a differential data, differential clock D flip-flop. Data enters the master portion of the flip-flop when the clock is low and is transferred to the slave, then the outputs, upon a positive transition of the clock. The differential clock inputs also allow the EL52 to be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that, under open input conditions (pulled down to V_{EE}), the outputs of the device will remain stable.

Package Type



SY100EL52

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1).....	+8V
NECL Power Supply Voltage (V_{EE}) (Note 2).....	-8V
PECL Mode Input Voltage (V_{IN}) (Note 3).....	+6V
NECL Mode Input Voltage (V_{IN}) (Note 4).....	-6V
Continuous Output Current (I_{OUT}).....	50 mA
Surge Output Current (I_{OUT}).....	100 mA

† **Notice:** Stresses above those listed under “Absolute Maximum ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

- Note 1:** $V_{EE} = 0V$.
2: $V_{CC} = 0V$.
3: $V_{EE} = 0V, V_{IN} \leq V_{CC}$.
4: $V_{CC} = 0V, V_{IN} \geq V_{EE}$.

TABLE 1-1: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics PECL: $V_{CC} = 4.2V$ to $5.5V$; $V_{EE} = 0V$; $T_A = -40^\circ C$ to $+85^\circ C$, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{CC}	4.2	5.0	5.5	V	—
Power Supply Current	I_{EE}	—	21	25	mA	$T_A = -40^\circ C$ to $+25^\circ C$
		—	24	29		$T_A = +85^\circ C$
Output High Voltage (Note 2)	V_{OH}	$V_{CC} - 1.085$	$V_{CC} - 1.005$	$V_{CC} - 0.88$	V	$T_A = -40^\circ C$
		$V_{CC} - 1.025$	$V_{CC} - 0.955$	$V_{CC} - 0.88$		$T_A = 0^\circ C$ to $+85^\circ C$
Output Low Voltage (Note 2)	V_{OL}	$V_{CC} - 1.830$	$V_{CC} - 1.695$	$V_{CC} - 1.555$	V	$T_A = -40^\circ C$
		$V_{CC} - 1.810$	$V_{CC} - 1.705$	$V_{CC} - 1.620$		$T_A = 0^\circ C$ to $+85^\circ C$
Input High Voltage (Single-Ended)	V_{IH}	$V_{CC} - 1.165$	—	$V_{CC} - 0.88$	V	—
Input Low Voltage (Single-Ended)	V_{IL}	$V_{CC} - 1.810$	—	$V_{CC} - 1.475$	V	—
Common Mode Range (Note 3)	V_{IHCMR}	$V_{CC} - 1.2$	—	$V_{CC} - 0.4$	V	D, /D
		3.0	—	$V_{CC} - 0.8$		CLK, /CLK
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL(MIN)}$

- Note 1:** Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
- 2:** Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$.
- 3:** The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

TABLE 1-2: DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics NECL: $V_{EE} = -5.5V$ to $-4.2V$; $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Voltage	V_{EE}	-5.5	-5.0	-4.2	V	—
Power Supply Current	I_{EE}	—	21	25	mA	$T_A = -40^{\circ}C$ to $+25^{\circ}C$
		—	24	29		$T_A = +85^{\circ}C$
Output High Voltage (Note 2)	V_{OH}	-1.085	-1.005	-0.88	V	$T_A = -40^{\circ}C$
		-1.025	-0.955	-0.88		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Output Low Voltage (Note 2)	V_{OL}	-1.830	-1.695	-1.555	V	$T_A = -40^{\circ}C$
		-1.810	-1.705	-1.620		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Input High Voltage (Single-Ended)	V_{IH}	-1.165	—	-0.88	V	—
Output High Voltage (Single-Ended)	V_{IL}	-1.810	—	-1.475	V	—
Common Mode Range (Note 3)	V_{IHCMR}	-1.2	—	-0.4	V	D, /D
		$V_{EE} + 3.0$	—	-0.8		CLK, /CLK
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL(MIN)}$

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2: Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$.

3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1V.

TABLE 1-3: AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = +4.2V$ to $+5.5V$, $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-4.2V$, $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Toggle Frequency	f_{MAX}	1.8	2.5	—	GHz	$T_A = -40^{\circ}C$
		2.2	2.8	—		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Propagation Delay to Output CLK	t_{PD}	235	335	515	ps	$T_A = -40^{\circ}C$
		275	365	465		$T_A = 0^{\circ}C$ to $+25^{\circ}C$
		320	410	510		$T_A = +85^{\circ}C$
Set-Up Time	t_S	125	0	—	ps	—
Hold Time	t_H	150	50	—	ps	—
Minimum Pulse Width	t_{PW}	400	—	—	ps	—
Input Swing (Note 1)	V_{PP}	150	—	1000	mV	—
Output Rise/Fall Time Q (20% to 80%)	t_r/t_f	100	225	350	ps	—

Note 1: Input swing for which AC parameters are guaranteed.

SY100EL52

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	—
Storage Temperature	T_S	-65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
D, /D	1, 2	Data input.
CLK, /CLK	3, 4	Clock input.
V _{EE}	5	Negative Power Supply.
/Q, Q	6, 7	Data output.
V _{CC}	8	Positive Power Supply.

2.1 Truth Table

TABLE 2-2: TRUTH TABLE

D	CLK	Q
L	Z	L
H	Z	H

Note: Z = Low-to-high transition.

SY100EL52

3.0 PACKAGING INFORMATION

3.1 Package Marking Information

8-Lead SOIC*



Example



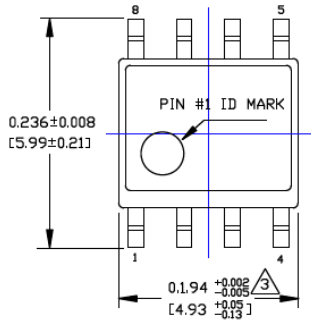
Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	•, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (̄) and/or Overbar (¯) symbol may not be to scale.	

8-Lead SOIC Package Outline and Recommended Land Pattern

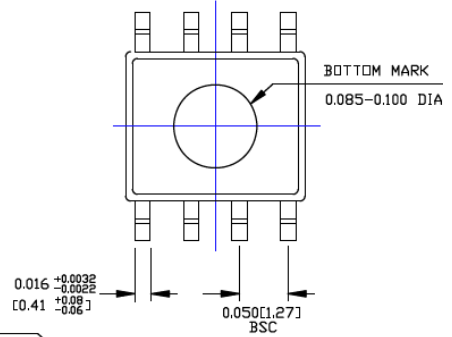
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8 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

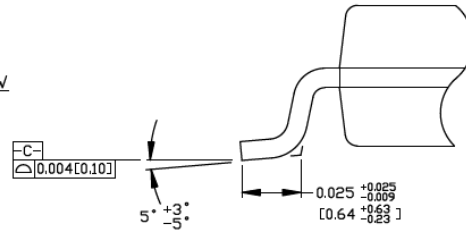
DRAWING #	SOICN-8LD-PL-1	UNIT	INCH [MM]
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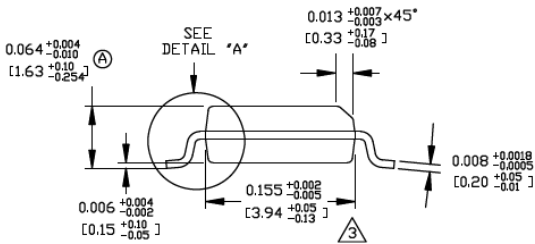
TOP VIEW



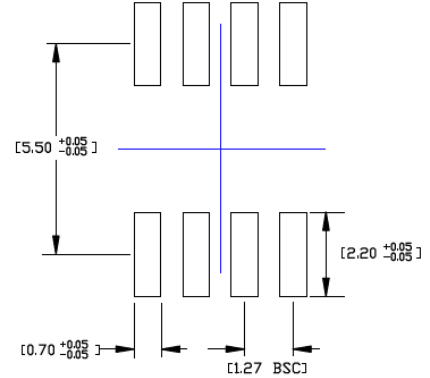
BOTTOM VIEW



DETAIL "A"



END VIEW



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES[MM].
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.010[0.25] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

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NOTES:

APPENDIX A: REVISION HISTORY

Revision A (September 2018)

- Converted Micrel document SY100EL52 to Microchip data sheet DS20006066A.
- Minor text changes throughout.
- Removed all reference to the EOL SY10EL52 version.

SY100EL52

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.		X	X	-XX
Device		Package	Temperature Range	Special Processing
Device:	SY100EL52: Differential Data and Clock D Flip-Flop			
Package:	Z	=	8-Lead SOIC	
Temperature Range:	G	=	-40°C to +85°C (Pb-Free NiPdAu)	
Special Processing:	<blank>	=	95/Tube	
	TR	=	1,000/Reel	

Examples:	
a) SY100EL52ZG:	SY100EL52, 8-Lead SOIC, -40°C to +85°C (Pb-Free NiPdAu), 95/Tube
b) SY100EL52ZG-TR:	SY100EL52, 8-Lead SOIC, -40°C to +85°C (Pb-Free NiPdAu), 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

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