

74ABT373

Octal Transparent Latch with 3-STATE Outputs

Features

- 3-STATE outputs for bus interfacing
- Output sink capability of 64mA, source capability of 32mA
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Output switching specified for both 50pF and 250pF loads
- Guaranteed simultaneous switching, noise level and dynamic threshold performance
- Guaranteed latchup protection
- High-impedance, glitch-free bus loading during entire power up and power down
- Nondestructive, hot-insertion capability

General Description

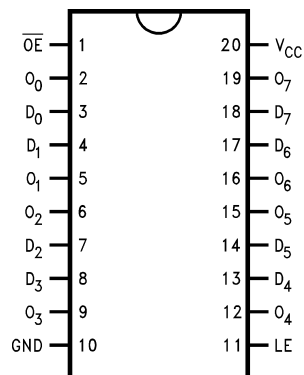
The ABT373 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (\overline{OE}) is LOW. When \overline{OE} is HIGH the bus output is in the high impedance state.

Ordering Information

Order Number	Package Number	Package Description
74ABT373CSC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ABT373CSJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ABT373CMSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide
74ABT373CMTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Pin Descriptions

Pin Names	Description
D ₀ –D ₇	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
O ₀ –O ₇	3-STATE Latch Outputs

Functional Description

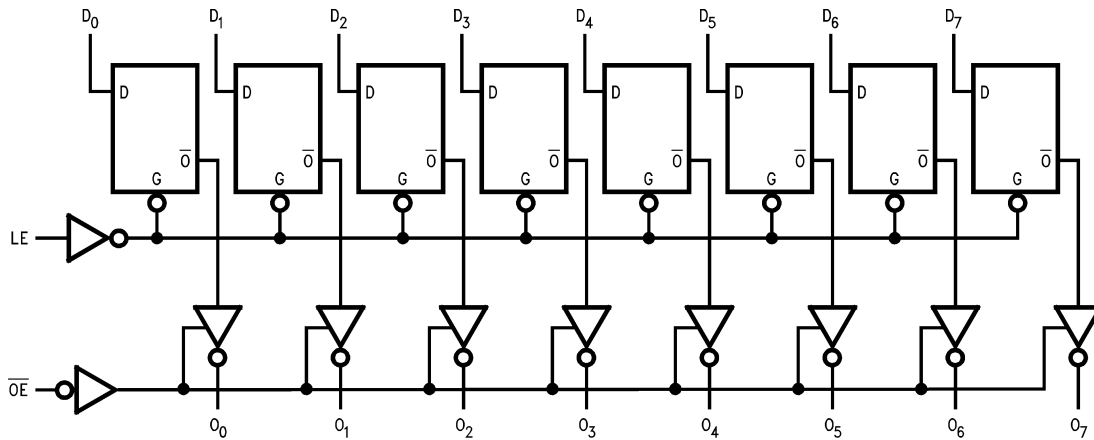
The ABT373 contains eight D-type latches with 3-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE buffers are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the buffers are in the bi-state mode. When \overline{OE} is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Output
LE	\overline{OE}	D_n	O_n
H	L	H	H
H	L	L	L
L	L	X	O_n (no change)
X	H	X	Z

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = HIGH Impedance State

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
T_{STG}	Storage Temperature	-65°C to +150°C
T_A	Ambient Temperature Under Bias	-55°C to +125°C
T_J	Junction Temperature Under Bias	-55°C to +150°C
V_{CC}	V_{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
V_{IN}	Input Voltage ⁽¹⁾	-0.5V to +7.0V
I_{IN}	Input Current ⁽¹⁾	-30mA to +5.0mA
V_O	Voltage Applied to Any Output Disabled or Power-Off State HIGH State	-0.5V to +5.5V -0.5V to V_{CC}
	Current Applied to Output in LOW State (Max.)	twice the rated I_{OL} (mA)
	DC Latchup Source Current Across Common Operating Range \overline{OE} Pin Other Pins	-150mA -500mA
	Over Voltage Latchup (I/O)	10V

Note:

1. Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
T_A	Free Air Ambient Temperature	-40°C to +85°C
V_{CC}	Supply Voltage	+4.5V to +5.5V
$\Delta V / \Delta t$	Minimum Input Edge Rate Data Input Enable Input	50mV/ns 20mV/ns

DC Electrical Characteristics

Symbol	Parameter		V _{CC}	Conditions	Min.	Typ.	Max.	Units
V _{IH}	Input HIGH Voltage			Recognized HIGH Signal	2.0			V
V _{IL}	Input LOW Voltage			Recognized LOW Signal			0.8	V
V _{CD}	Input Clamp Diode Voltage		Min.	I _{IN} = -18mA			-1.2	V
V _{OH}	Output HIGH Voltage		Min.	I _{OH} = -3mA	2.5			V
				I _{OH} = -32mA	2.0			
V _{OL}	Output LOW Voltage		Min.	I _{OL} = 64mA			0.55	V
I _{IH}	Input HIGH Current		Max.	V _{IN} = 2.7V ⁽³⁾			1	μA
				V _{IN} = V _{CC}			1	
I _{BVI}	Input HIGH Current Breakdown Test		Max.	V _{IN} = 7.0V			7	μA
I _{IL}	Input LOW Current		Max.	V _{IN} = 0.5V ⁽³⁾			-1	μA
				V _{IN} = 0.0V			-1	
V _{ID}	Input Leakage Test		0.0	I _{ID} = 1.9μA, All Other Pins Grounded	4.75			V
I _{OZH}	Output Leakage Current		0-5.5V	V _{OUT} = 2.7V, \overline{OE} = 2.0V			10	μA
I _{OZL}	Output Leakage Current		0-5.5V	V _{OUT} = 0.5V, \overline{OE} = 2.0V			-10	μA
I _{OS}	Output Short-Circuit Current		Max.	V _{OUT} = 0.0V	-100		-275	mA
I _{CEX}	Output HIGH Leakage Current		Max.	V _{OUT} = V _{CC}			50	μA
I _{ZZ}	Bus Drainage Test		0.0	V _{OUT} = 5.5V, All Others GND			100	μA
I _{CCH}	Power Supply Current		Max.	All Outputs HIGH			50	μA
I _{CCL}	Power Supply Current		Max.	All Outputs LOW			30	mA
I _{CCZ}	Power Supply Current		Max.	\overline{OE} = V _{CC} , All Others at V _{CC} or Ground			50	μA
I _{CCT}	Additional I _{CC} /Input	Outputs Enabled	Max.	V _I = V _{CC} - 2.1V			2.5	mA
		Outputs 3-STATE		Enable Input V _I = V _{CC} - 2.1V			2.5	mA
		Outputs 3-STATE		Data Input V _I = V _{CC} - 2.1V, All Others at V _{CC} or Ground			2.5	mA
I _{CCD}	Dynamic I _{CC} No Load ⁽³⁾		Max.	Outputs OPEN, LE = V _{CC} , \overline{OE} = GND ⁽²⁾ , One-Bit Toggling, 50% Duty Cycle			0.12	mA/MHz

Notes:

- For 8-bit toggling, I_{CCD} < 0.8mA/MHz.
- Guaranteed, but not tested.

DC Electrical Characteristics

SOIC package.

Symbol	Parameter	V _{CC}	Conditions		Min.	Typ.	Max.	Units
			C _L = 50pF, R _L = 500Ω	T _A				
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	5.0		T _A = 25°C ⁽⁴⁾		0.4	0.8	V
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	5.0		T _A = 25°C ⁽⁴⁾	-1.2	-0.8		V
V _{OHV}	Minimum HIGH Level Dynamic Output Voltage	5.0		T _A = 25°C ⁽⁵⁾	2.5	3.0		V
V _{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0		T _A = 25°C ⁽⁶⁾	2.0	1.7		V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0		T _A = 25°C ⁽⁶⁾		0.9	0.6	V

Notes:

- Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output at Low. Guaranteed, but not tested.
- Max number of outputs defined as (n). n – 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.
- Max number of data inputs (n) switching. n – 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}). Guaranteed, but not tested.

AC Electrical Characteristics

SOIC and SSOP package.

Symbol	Parameter	T _A = +25°C, V _{CC} = +5.0V, C _L = 50pF			T _A = -55°C to +125°C, V _{CC} = 4.5V to 5.5V, C _L = 50pF		T _A = -40°C to +85°C, V _{CC} = 4.5V to 5.5V, C _L = 50pF		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t _{PLH}	Propagation Delay	1.9	2.7	4.5	1.0	6.8	1.9	4.5	ns
t _{PHL}	D _n to O _n	1.9	2.8	4.5	1.0	7.0	1.9	4.5	
t _{PLH}	Propagation Delay	2.0	3.1	5.0	1.0	7.7	2.0	5.0	ns
t _{PHL}	LE to O _n	2.0	3.0	5.0	1.5	7.7	2.0	5.0	
t _{PZH}	Output Enable Time	1.5	3.1	5.3	1.0	6.7	1.5	5.3	ns
t _{PZL}		1.5	3.1	5.3	1.5	7.2	1.5	5.3	
t _{PHZ}	Output Disable Time	2.0	3.6	5.4	1.7	8.0	2.0	5.4	ns
t _{PLZ}		2.0	3.4	5.4	1.0	7.0	2.0	5.4	

AC Operating Requirements

SOIC and SSOP packages.

Symbol	Parameter	$T_A = +25^\circ\text{C}$, $V_{CC} = +5.0\text{V}$, $C_L = 50\text{pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$, $V_{CC} = 4.5\text{V to } 5.5\text{V}$, $C_L = 50\text{pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 4.5\text{V to } 5.5\text{V}$, $C_L = 50\text{pF}$		Units
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
f_{TOGGLE}	Max Toggle Frequency		100		100				MHz
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW, D_n to LE	1.5			2.5		1.5		ns
$t_{\text{S}}(\text{L})$		1.5			2.5		1.5		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW, D_n to LE	1.0			2.5		1.0		ns
$t_{\text{H}}(\text{L})$		1.0			2.5		1.0		
$t_{\text{W}}(\text{H})$	Pulse Width, LE HIGH	3.0			3.3		3.0		ns

Extended AC Electrical Characteristics

SOIC package.

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 4.5\text{V to } 5.5\text{V}$, $C_L = 50\text{pF}$, 8 Outputs Switching ⁽⁷⁾		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 4.5\text{V to } 5.5\text{V}$, $C_L = 250\text{pF}$ ⁽⁸⁾		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$, $V_{CC} = 4.5\text{V to } 5.5\text{V}$, $C_L = 250\text{pF}$, 8 Outputs Switching ⁽⁹⁾		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH}	Propagation Delay, D_n to O_n	1.5	5.2	2.0	6.8	2.0	9.0	ns
t_{PHL}		1.5	5.2	2.0	6.8	2.0	9.0	
t_{PLH}	Propagation Delay, LE to O_n	1.5	5.5	2.0	7.5	2.0	9.5	ns
t_{PHL}		1.5	5.5	2.0	7.5	2.0	9.5	
t_{PZH}	Output Enable Time	1.5	6.2	2.0	8.0	2.0	10.5	ns
t_{PZL}			1.5	6.2	2.0	8.0	2.0	
t_{PHZ}	Output Disable Time	1.0	5.5	(10)		(10)		ns
t_{PZL}			1.0	5.5				

Notes:

- This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
- This specification is guaranteed but not tested. The limits represent propagation delay with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load. This specification pertains to single output switching only.
- This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250pF load capacitors in place of the 50pF load capacitors in the standard AC load.
- The 3-STATE delay times are dominated by the RC network (500Ω, 250pF) on the output and has been excluded from the datasheet.

Skew

SOIC package.

Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C},$ $V_{CC} = 4.5\text{V} - 5.5\text{V},$ $C_L = 50\text{pF},$ 8 Outputs Switching ⁽¹¹⁾	$T_A = -40^\circ\text{C to } +85^\circ\text{C},$ $V_{CC} = 4.5\text{V} - 5.5\text{V},$ $C_L = 250\text{pF},$ 8 Outputs Switching ⁽¹²⁾	Units
		Max.	Max.	
$t_{OSHL}^{(13)}$	Pin to Pin Skew, HL Transitions	1.0	1.5	ns
$t_{OSLH}^{(13)}$	Pin to Pin Skew, LH Transitions	1.0	1.5	ns
$t_{PS}^{(15)}$	Duty Cycle, LH–HL Skew	1.4	3.5	ns
$t_{OST}^{(13)}$	Pin to Pin Skew, LH/HL Transitions	1.5	3.9	ns
$t_{PV}^{(14)}$	Device to Device Skew, LH/HL Transitions	2.0	4.0	ns

Notes:

- This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50pF load capacitors in the standard AC load.
- This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).
- Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW (t_{OSHL}), LOW-to-HIGH (t_{OSLH}), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW (t_{OST}). This specification is guaranteed but not tested.
- Propagation delay variation is for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.
- This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

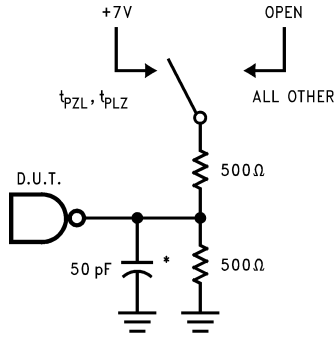
Capacitance

Symbol	Parameter	Conditions $T_A = 25^\circ\text{C}$	Typ.	Units
C_{IN}	Input Capacitance	$V_{CC} = 0\text{V}$	5	pF
$C_{OUT}^{(16)}$	Output Capacitance	$V_{CC} = 5.0\text{V}$	9	pF

Note:

- C_{OUT} is measured at frequency $f = 1\text{MHz}$, per MIL-STD-883, Method 3012.

AC Loading



*Includes jig and probe capacitance

Figure 1. Standard AC Test Load

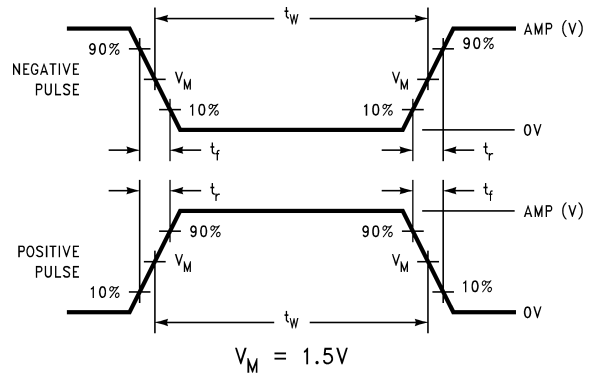


Figure 2. Test Input Signal Levels

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1MHz	500ns	2.5ns	2.5ns

Figure 3. Test Input Signal Requirements

AC Waveforms

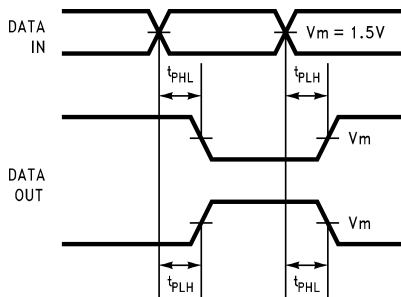


Figure 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

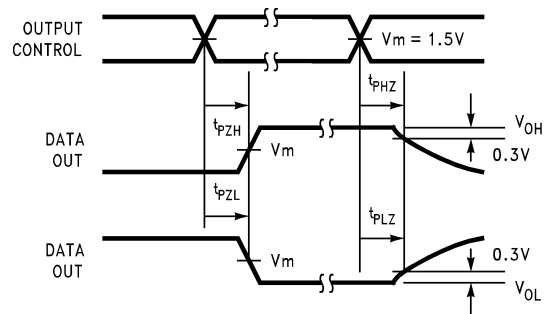


Figure 6. 3-STATE Output HIGH and LOW Enable and Disable Times

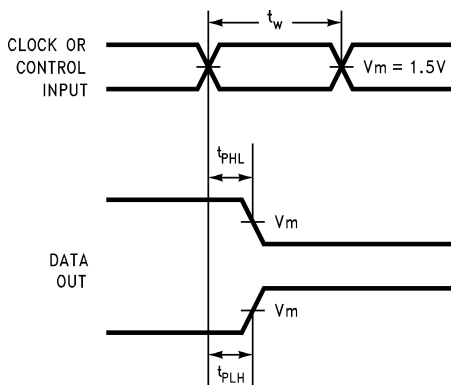


Figure 5. Propagation Delay, Pulse Width Waveforms

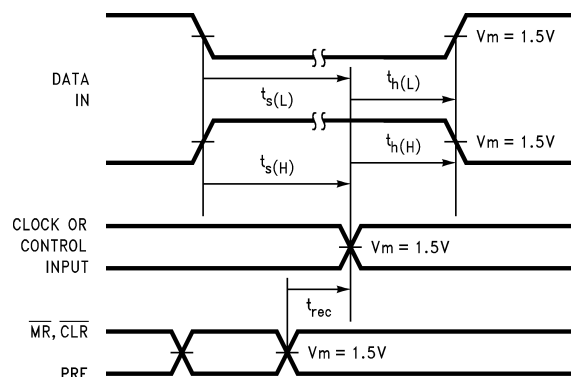


Figure 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions

Dimensions are in inches (millimeters) unless otherwise noted.

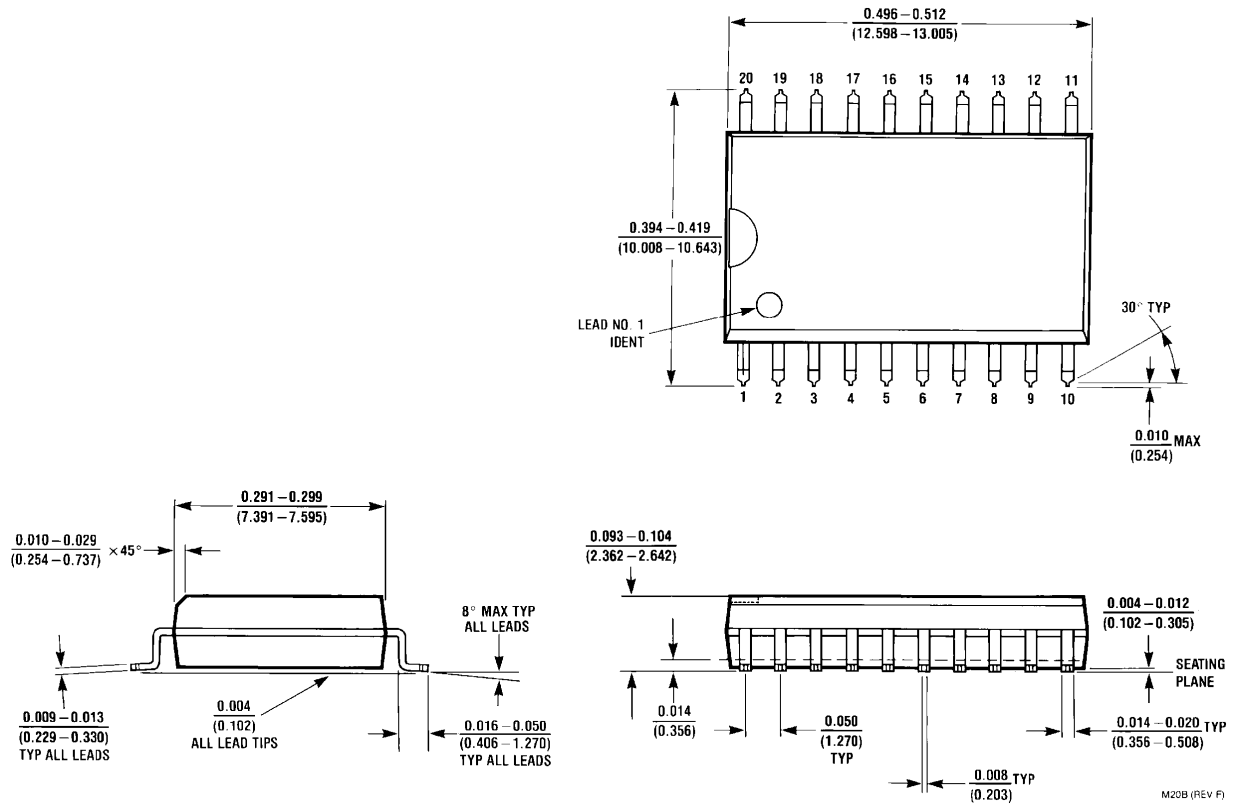
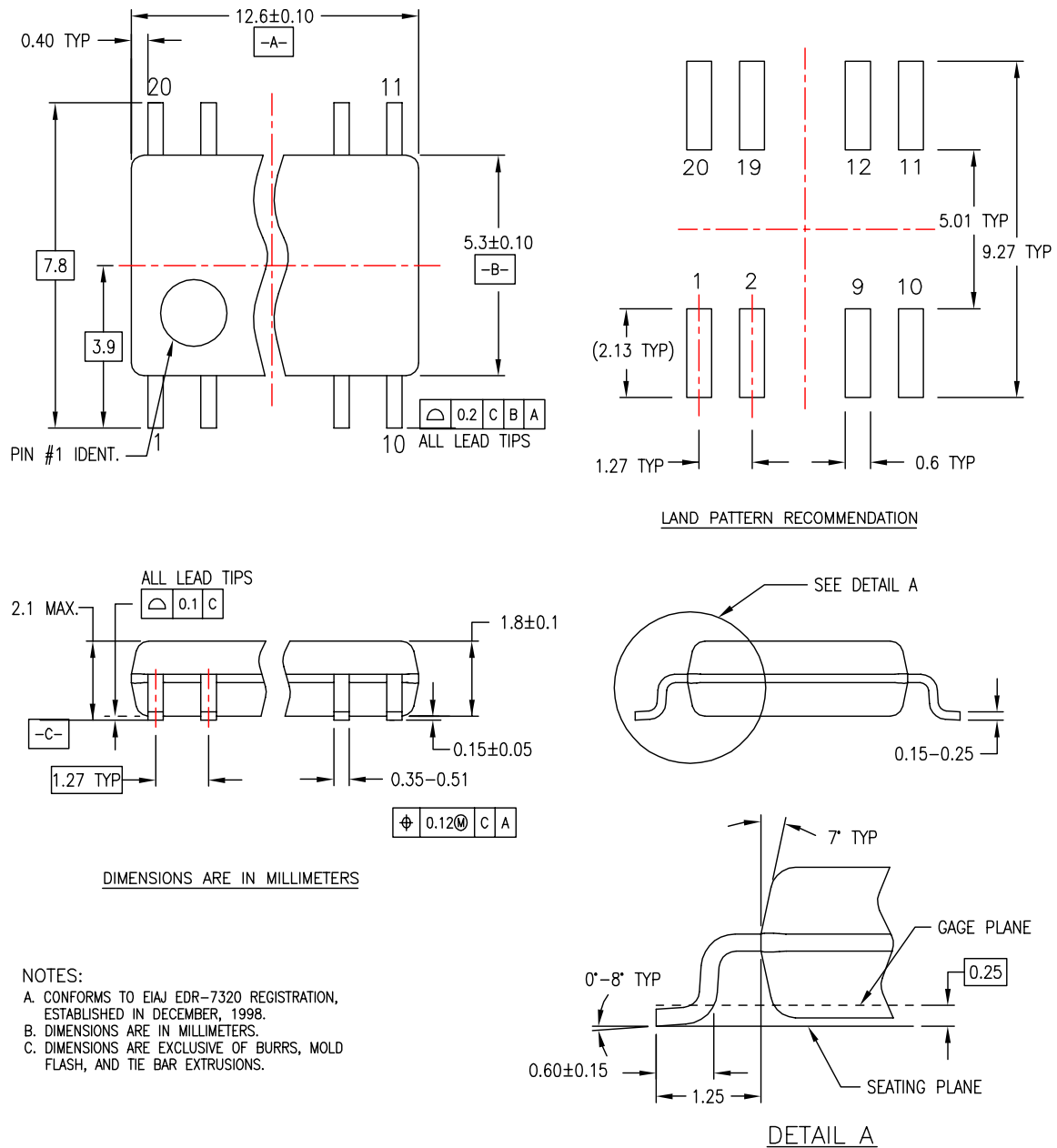


Figure 8. 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



NOTES:

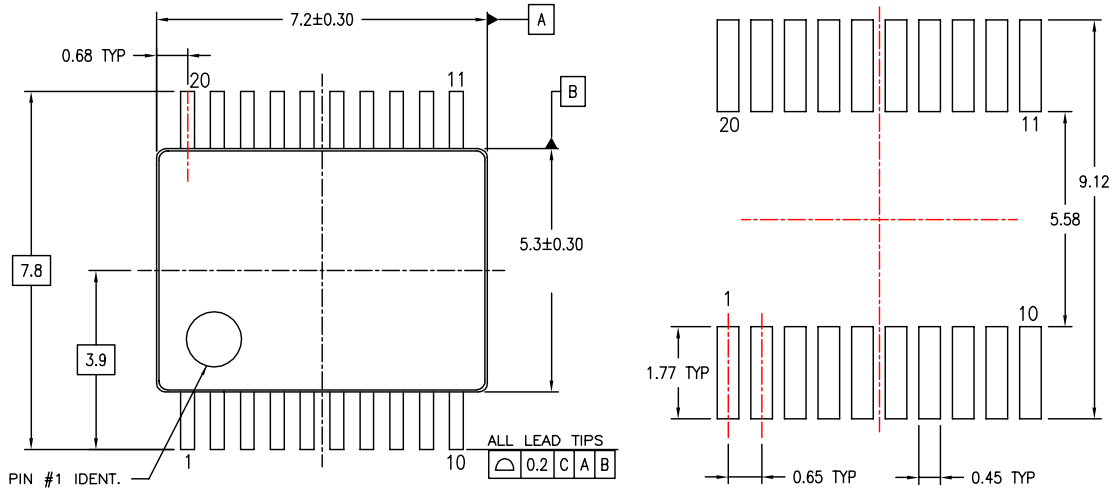
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DREVC

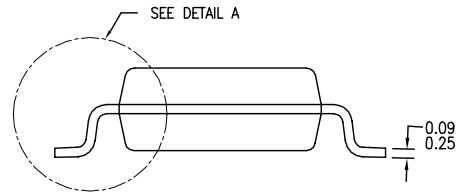
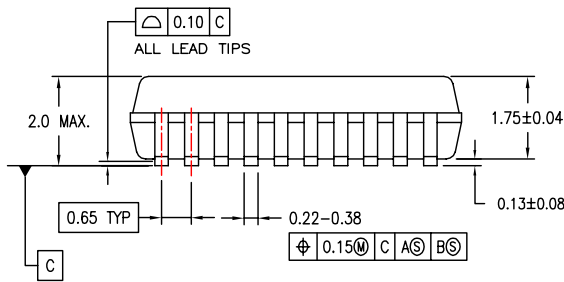
**Figure 9. 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D**

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



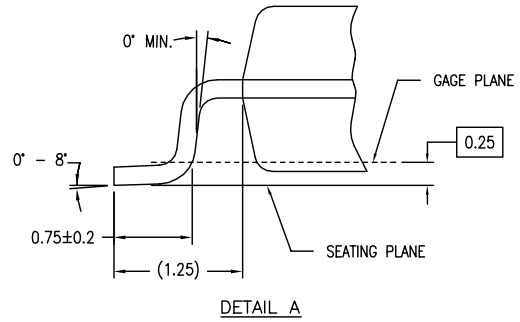
LAND PATTERN RECOMMENDATIONS



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-150, VARIATION AE, DATE 1/94.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M - 1994.

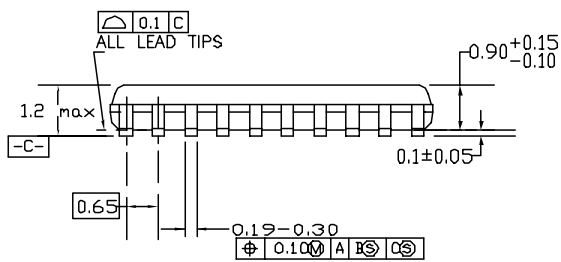
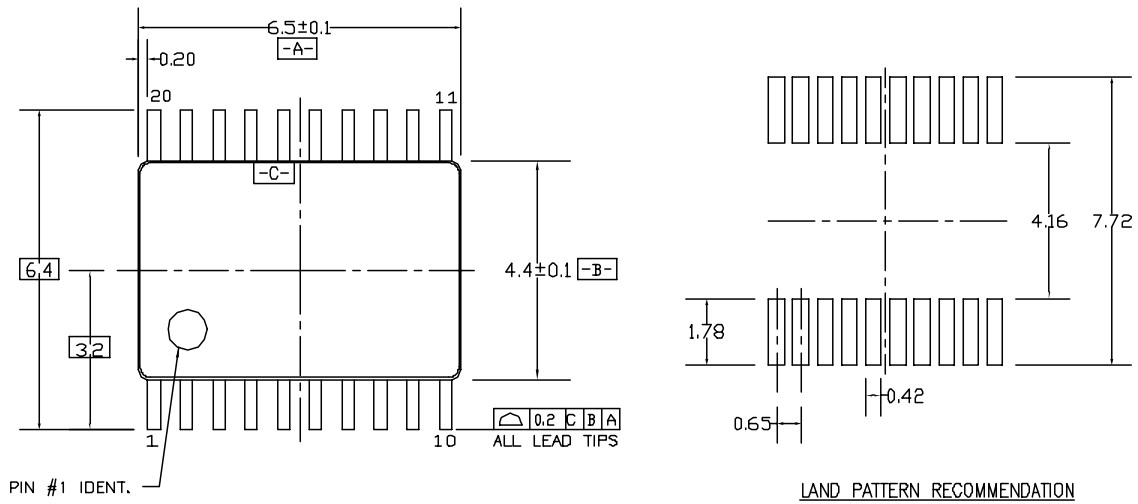


MSA20REVB

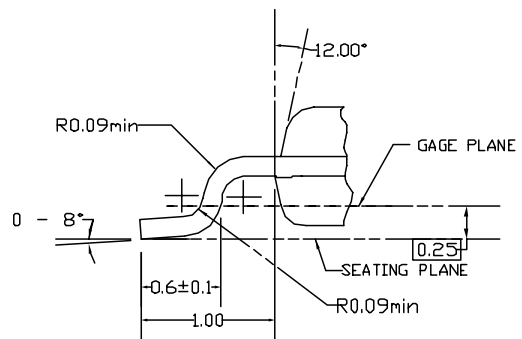
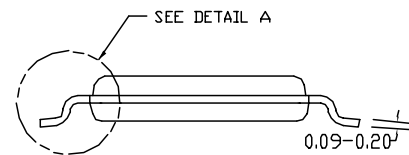
Figure 10. 20-Lead Shrink Small Outline Package (SSOP), JEDEC MO-150, 5.3mm Wide Package Number MSA20

Physical Dimensions (Continued)

Dimensions are in millimeters unless otherwise noted.



DIMENSIONS ARE IN MILLIMETERS



DETAIL A

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MD-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.


MTC20REV D1

Figure 11. 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20



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EnSigna [™]	OPTOLOGIC [®]	SuperSOT [™] -3	
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FACT [®]	PACMAN [™]	SuperSOT [™] -8	
FAST [®]	POP [™]	SyncFET [™]	
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FPS [™]	Power247 [®]	The Power Franchise [®]	
FRFET [®]	PowerEdge [™]	 ™	
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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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Rev. I24