

MC74HC174A

Hex D Flip-Flop with Common Clock and Reset High-Performance Silicon-Gate CMOS

The MC74HC174A is identical in pinout to the LS174. The device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs.

This device consists of six D flip-flops with common Clock and Reset inputs. Each flip-flop is loaded with a low-to-high transition of the Clock input. Reset is asynchronous and active-low.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 162 FETs or 40.5 Equivalent Gates

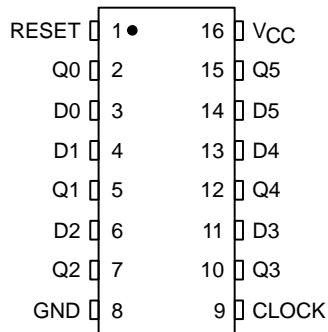


Figure 5. Pin Assignment

FUNCTION TABLE

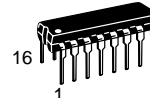
Inputs			Output
Reset	Clock	D	Q
L	X	X	L
H	\nearrow	H	H
H	\nearrow	L	L
H	L	X	No Change
H	\searrow	X	No Change



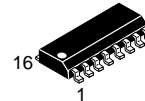
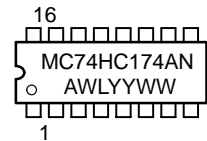
ON Semiconductor

<http://onsemi.com>

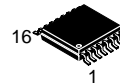
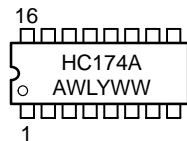
MARKING DIAGRAMS



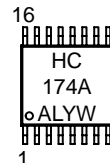
PDIP-16
N SUFFIX
CASE 648



SO-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



A = Assembly Location
L, WL = Wafer Lot
Y, YY = Year
W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC74HC174AN	PDIP-16	2000/Box
MC74HC174AD	SOIC-16	48/Rail
MC74HC174ADR2	SOIC-16	2500/Reel
MC74HC174ADT	TSSOP-16	96/Rail
MC74HC174ADTR2	TSSOP-16	2500/Reel

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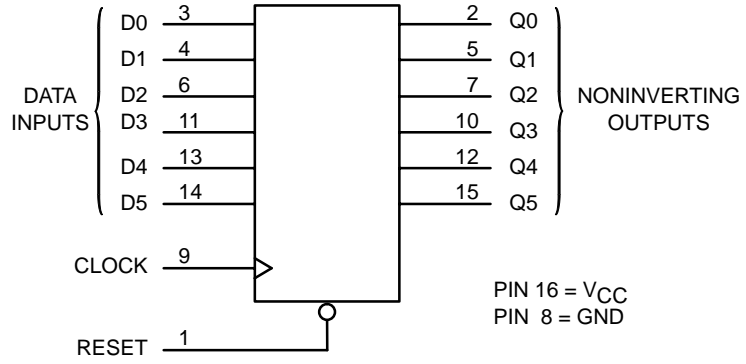


Figure 6. Logic Diagram

DESIGN/VALUE TABLE

Design Criteria	Value	Units
Internal Gate Count*	40.5	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μ W
Speed Power Product	.0075	μ J

*Equivalent to a two-input NAND gate.

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MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} + 1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND) (Note 2)	-0.5 to V _{CC} + 0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
T _{STG}	Storage Temperature Range	-65 to +150	C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds PDIP, SOIC, TSSOP	260	C
T _J	Junction Temperature Under Bias	+150	C
θ _{JA}	Thermal Resistance PDIP SOIC TSSOP	78 112 148	C/W
P _D	Power Dissipation in Still Air at 85 C PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL-94-V0 (0.125 in)	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	> 2000 > 100 > 500	V
I _{LATCH-UP}	Latch-Up Performance Above V _{CC} and Below GND at 85 C (Note 6)	±300	mA

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated conditions is not implied.
2. I_O absolute maximum rating must be observed.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.
6. Tested to EIA/JESD78.
7. For high frequency or heavy load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND) (Note 8)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	C
t _r , t _f	Input Rise and Fall Time (Figure 8) V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	0 0 0	1000 500 400	ns

8. Unused inputs may not be left open. All inputs must be tied to a high- or low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				-55°C to 25°C	≤85°C	≤125°C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} = 0.1 V or V _{CC} - 0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I _{IN}	Maximum Input Leakage Current	V _{IN} = V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0	4.0	40	160	μA

9. Information on typical parametric values, along with high frequency or heavy load considerations, can be found in the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, Input t_r = t_f = 6.0 ns)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			-55°C to 25°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 8 and 11)	2.0	6.0	4.8	4.0	MHz
		4.5	30	24	20	
		6.0	35	28	24	
t _{PLH} t _{PHL}	Maximum Propagation Delay, Clock to Q (Figures 9 and 11)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t _{PLH} t _{PHL}	Maximum Propagation Delay, Reset to Q (Figures 2 and 11)	2.0	110	140	160	ns
		4.5	21	28	32	
		6.0	19	24	27	
t _{TLH} t _{THL}	Maximum Output Transition Time, Any Output (Figures 8 and 11)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{in}	Maximum Input Capacitance		10	10	10	pF

10. For propagation delays with loads other than 50 pF, and information on typical parametric values, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

C _{PD}	Power Dissipation Capacitance, per Enabled Output (Note 11)	Typical @ 25°C, V _{CC} = 5.0 V		pF
		62		

11. Used to determine the no-load dynamic power consumption: P_D = C_{PD} V_{CC}²f + I_{CC} V_{CC}. For load considerations, see the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

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TIMING REQUIREMENTS ($C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	Figure	VCC V	Guaranteed Limit						Unit
				-55°C to 25°C		≤85°C		≤125°C		
				Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Data to Clock	10	2.0 4.5 6.0	50 10 9.0		65 13 11		75 15 13		ns
t_h	Minimum Hold Time, Clock to Data	10	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_{rec}	Minimum Recovery Time, Reset Inactive to Clock	9	2.0 4.5 6.0	5.0 5.0 5.0		5.0 5.0 5.0		5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Clock	8	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_w	Minimum Pulse Width, Reset	9	2.0 4.5 6.0	75 15 13		95 19 16		110 22 19		ns
t_r, t_f	Maximum Input Rise and Fall Times	8	2.0 4.5 6.0		1000 500 400		1000 500 400		1000 500 400	ns

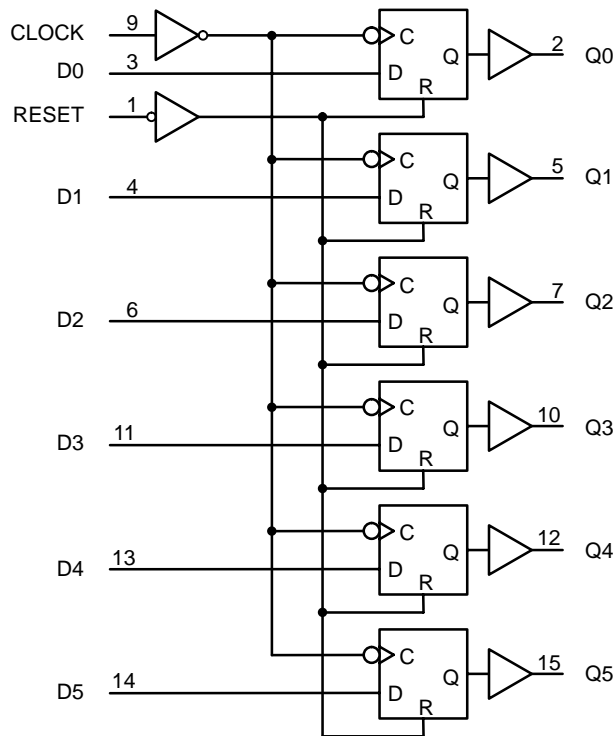


Figure 7. Expanded Logic Diagram

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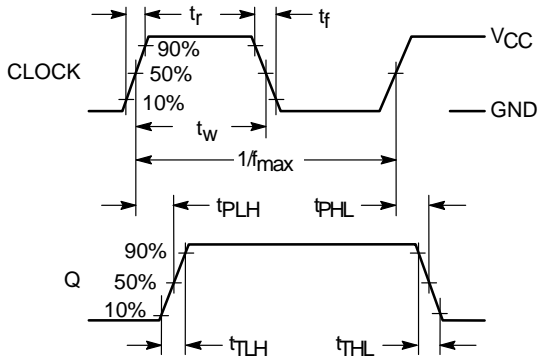


Figure 8. Switching Waveform

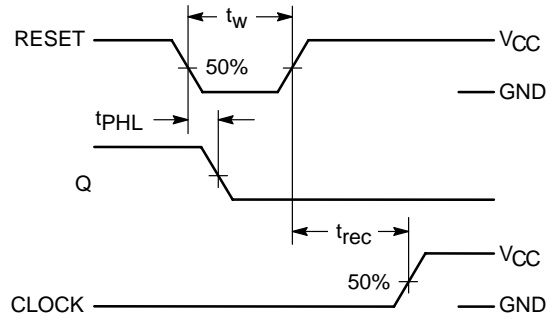


Figure 9. Switching Waveform

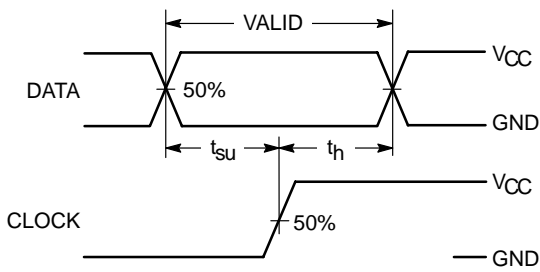
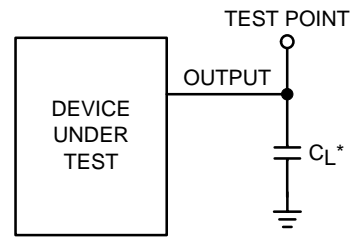


Figure 10. Switching Waveform



*Includes all probe and jig capacitance

Figure 11. Test Circuit