

MC14555B, MC14556B

Dual Binary to 1-of-4 Decoder/Demultiplexer

The MC14555B and MC14556B are constructed with complementary MOS (CMOS) enhancement mode devices. Each Decoder/Demultiplexer has two select inputs (A and B), an active low Enable input (E), and four mutually exclusive outputs (Q0, Q1, Q2, Q3). The MC14555B has the selected output go to the “high” state, and the MC14556B has the selected output go to the “low” state. Expanded decoding such as binary-to-hexadecimal (1-of-16), etc., can be achieved by using other MC14555B or MC14556B devices.

Applications include code conversion, address decoding, memory selection control, and demultiplexing (using the Enable input as a data input) in digital data transmission systems.

Features

- Diode Protection on All Inputs
- Active High or Active Low Outputs
- Expandable
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pb-Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Input or Output Current (DC or Transient) per Pin	I _{in} , I _{out}	±10	mA
Power Dissipation, per Package (Note 1)	P _D	500	mW
Ambient Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range	T _{stg}	-65 to +150	°C
Lead Temperature (8-Second Soldering)	T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating: Plastic “P and D/DW”
Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

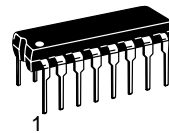
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



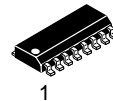
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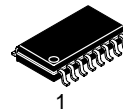
MARKING DIAGRAMS



PDIP-16
P SUFFIX
CASE 648



SOIC-16
D SUFFIX
CASE 751B

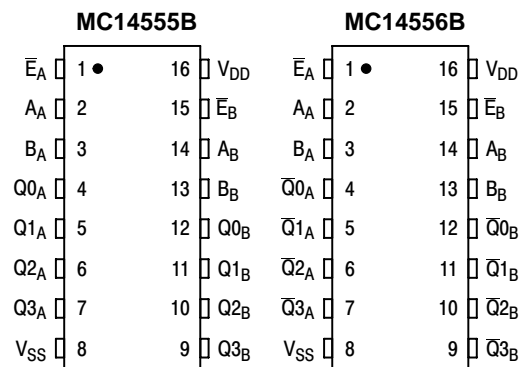


SOEIAJ-16
F SUFFIX
CASE 966



x = 5 or 6
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

PIN ASSIGNMENTS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

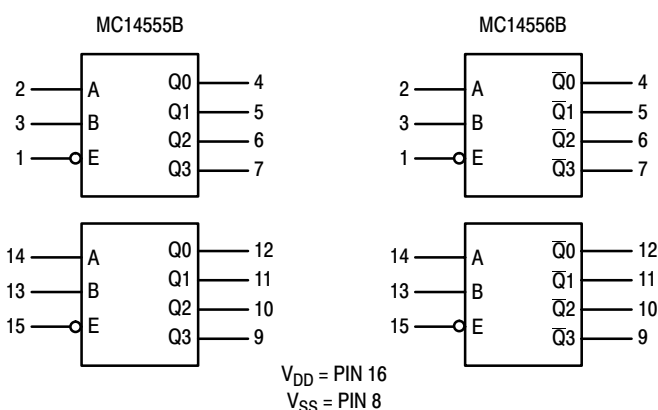
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TRUTH TABLE

Inputs			Outputs							
Enable	Select		MC14555B				MC14556B			
\bar{E}	B	A	Q3	Q2	Q1	Q0	$\bar{Q}3$	$\bar{Q}2$	$\bar{Q}1$	$\bar{Q}0$
0	0	0	0	0	0	1	1	1	1	0
0	0	1	0	0	1	0	1	1	0	1
0	1	0	0	1	0	0	1	0	1	1
0	1	1	1	0	0	0	0	1	1	1
1	X	X	0	0	0	0	1	1	1	1

X = Don't Care

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage $V_{in} = V_{DD}$ or 0	“0” Level V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
$V_{in} = 0$ or V_{DD}	“1” Level V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
Input Voltage ($V_O = 4.5$ or 0.5 Vdc) ($V_O = 9.0$ or 1.0 Vdc) ($V_O = 13.5$ or 1.5 Vdc)	“0” Level V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
$V_O = 0.5$ or 4.5 Vdc) ($V_O = 1.0$ or 9.0 Vdc) ($V_O = 1.5$ or 13.5 Vdc)	“1” Level V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
Output Drive Current ($V_{OH} = 2.5$ Vdc) ($V_{OH} = 4.6$ Vdc) ($V_{OH} = 9.5$ Vdc) ($V_{OH} = 13.5$ Vdc)	Source I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
	5.0	–0.64	–	–0.51	–0.88	–	–0.36	–		
$V_{OL} = 0.4$ Vdc) ($V_{OL} = 0.5$ Vdc) ($V_{OL} = 1.5$ Vdc)	Sink I_{OL}	10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
Input Current	I_{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 1.0	μ Adc
Input Capacitance, ($V_{in} = 0$)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μ Adc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) ($C_L = 50$ pF on all outputs, all buffers switching)	I_T	5.0	$I_T = (0.85 \mu A/kHz) f + I_{DD}$							μ Adc
10	$I_T = (1.70 \mu A/kHz) f + I_{DD}$									
15	$I_T = (2.60 \mu A/kHz) f + I_{DD}$									

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$ where: I_T is in μA (per package), C_L in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and $k = 0.002$.

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SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time – A, B to Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 62 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 45 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	– – –	220 95 70	440 190 140	ns
Propagation Delay Time – E to Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 52 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	– – –	200 85 65	400 170 130	ns

- The formulas given are for the typical characteristics only at 25°C .
- Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

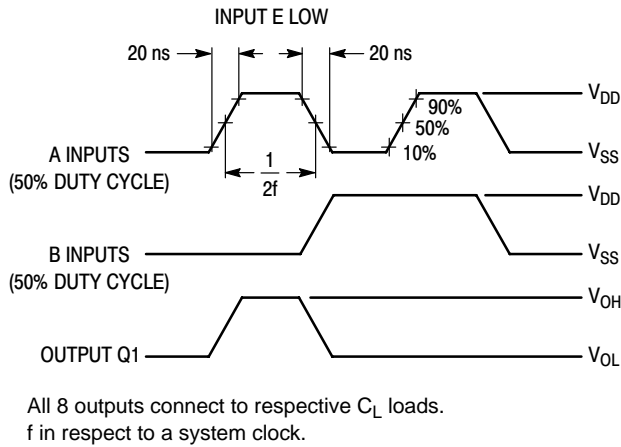


Figure 1. Dynamic Power Dissipation Signal Waveforms

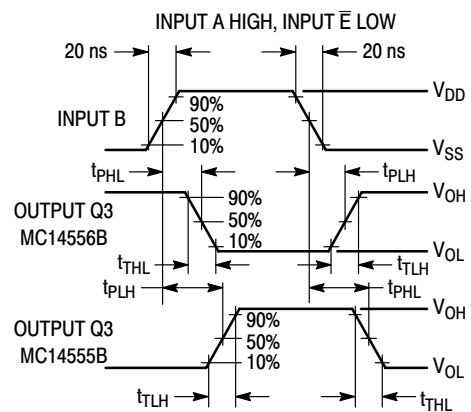
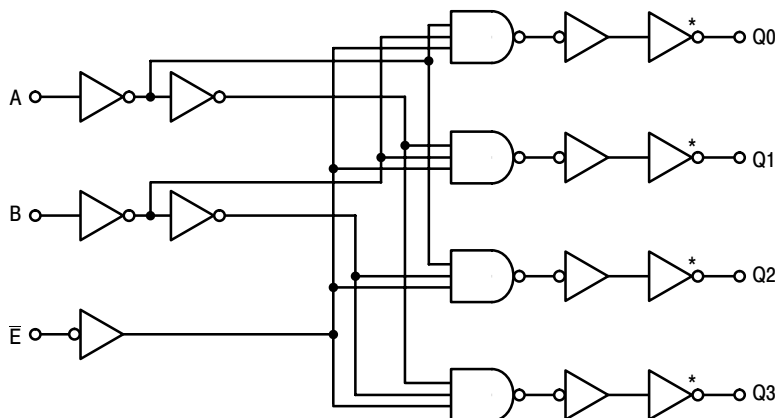


Figure 2. Dynamic Signal Waveforms

LOGIC DIAGRAM (1/2 of Dual)



*Eliminated for MC14555B

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ORDERING INFORMATION

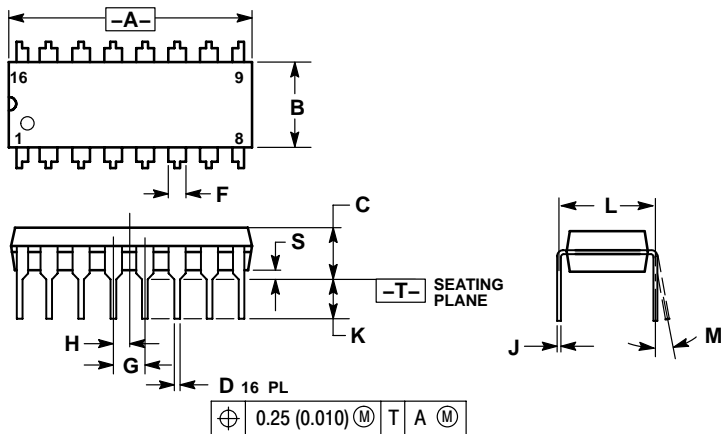
Device	Package	Shipping†
MC14555BCP	PDIP-16	25 Units / Rail
MC14555BCPG	PDIP-16 (Pb-Free)	
MC14555BD	SOIC-16	48 Units / Rail
MC14555BDG	SOIC-16 (Pb-Free)	
MC14555BDR2	SOIC-16	2500 / Tape & Reel
MC14555BDR2G	SOIC-16 (Pb-Free)	
MC14555BFEL	SOEIAJ-16	2000 / Tape & Reel
MC14555BFELG	SOEIAJ-16 (Pb-Free)	
MC14556BCP	PDIP-16	25 Units / Rail
MC14556BCPG	PDIP-16 (Pb-Free)	
MC14556BD	SOIC-16	48 Units / Rail
MC14556BDR2	SOIC-16	2500 / Tape & Reel
MC14556BDR2G	SOIC-16 (Pb-Free)	
MC14556BF	SOEIAJ-16	50 Units / Tube
MC14556BFEL	SOEIAJ-16	2000 / Tape & Reel
MC14556BFELG	SOEIAJ-16 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

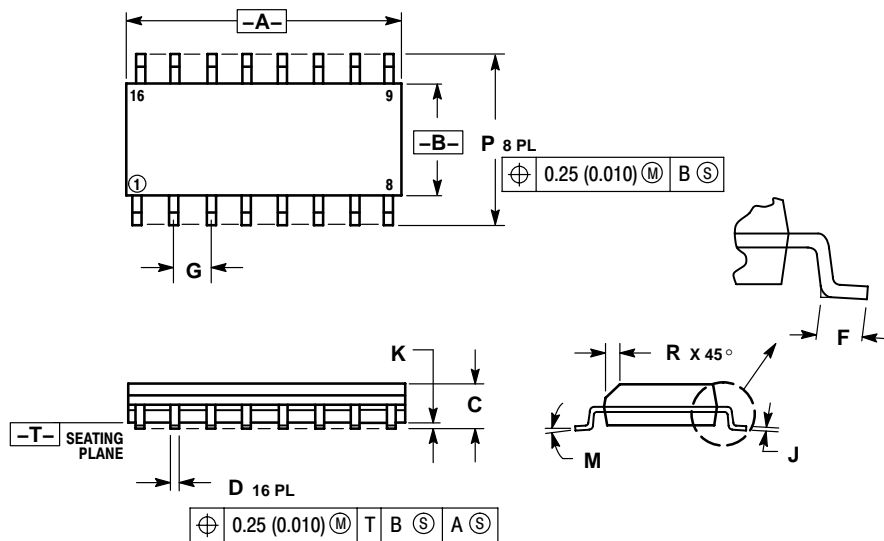
PDIP-16 CASE 648-08 ISSUE T



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
 5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

SOIC-16 CASE 751B-05 ISSUE J



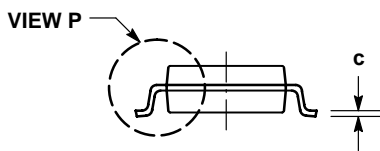
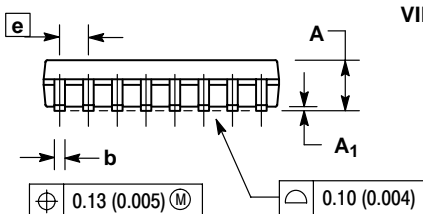
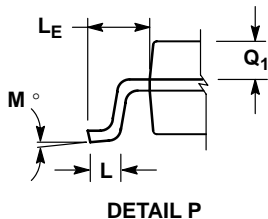
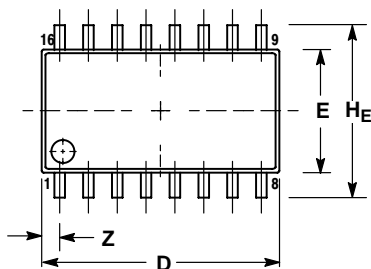
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

MC14555B, MC14556B

PACKAGE DIMENSIONS

SOEIAJ-16
CASE 966-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	0.78	---	0.031

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