

# 74LVT244B; 74LVTH244B

3.3 V octal buffer/line driver; 3-state

Rev. 6 — 12 August 2021

Product data sheet

## 1. General description

The 74LVT244B; 74LVTH244B is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables ( $1\overline{OE}$  and  $2\overline{OE}$ ), each controlling four of the 3-state outputs. A HIGH on  $n\overline{OE}$  causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs

## 2. Features and benefits

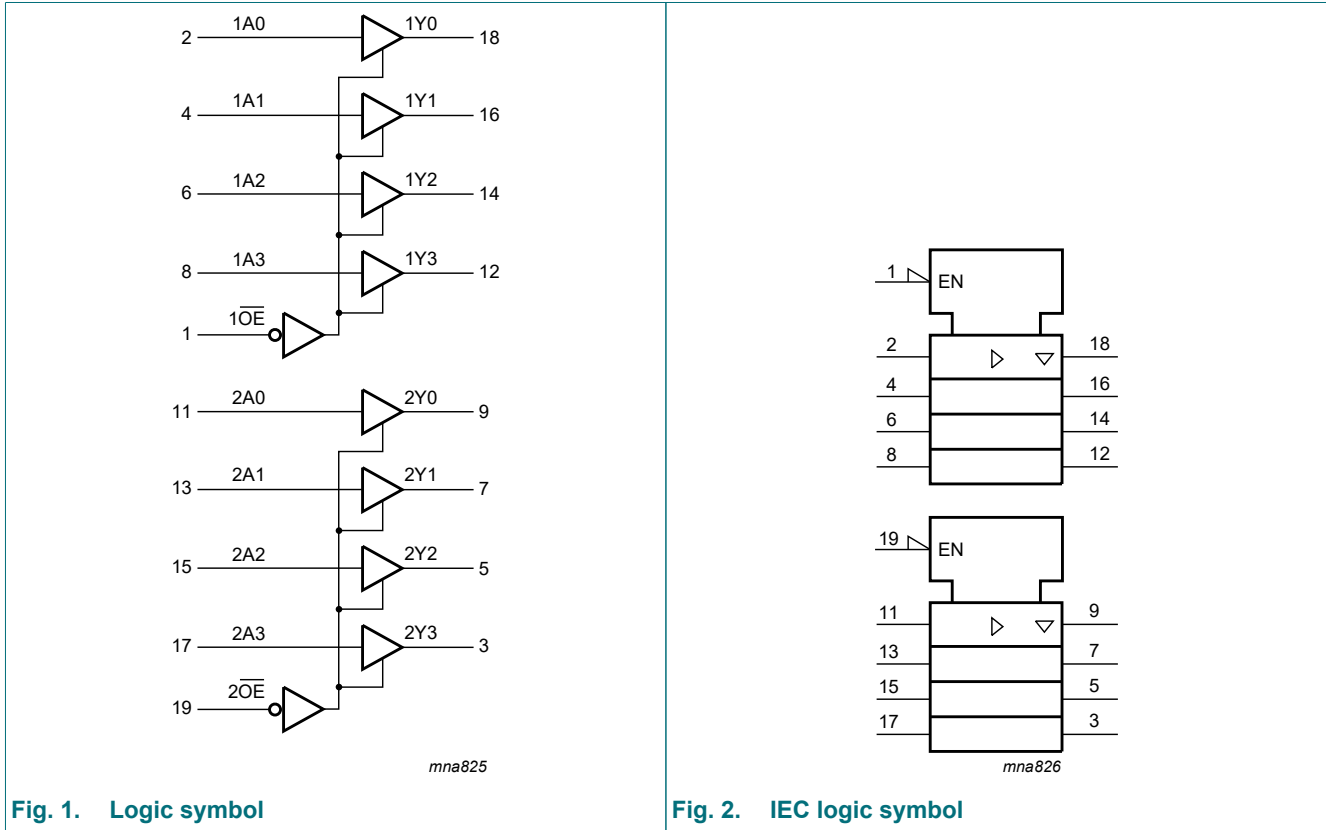
- Octal bus interface
- 3-state buffers
- Speed upgrade of 74LVT244A
- Wide supply voltage range from 2.7 to 3.6 V
- BiCMOS high speed and output drive
- Output capability: +64 mA and -32 mA
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Live insertion and extraction permitted
- $I_{OFF}$  circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
- ESD protection:
  - HBM EIA/JESD22-A114-C exceeds 2000 V
  - MM EIA/JESD22-A115-A 200 V
- Specified from -40 °C to +85 °C

## 3. Ordering information

Table 1. Ordering information

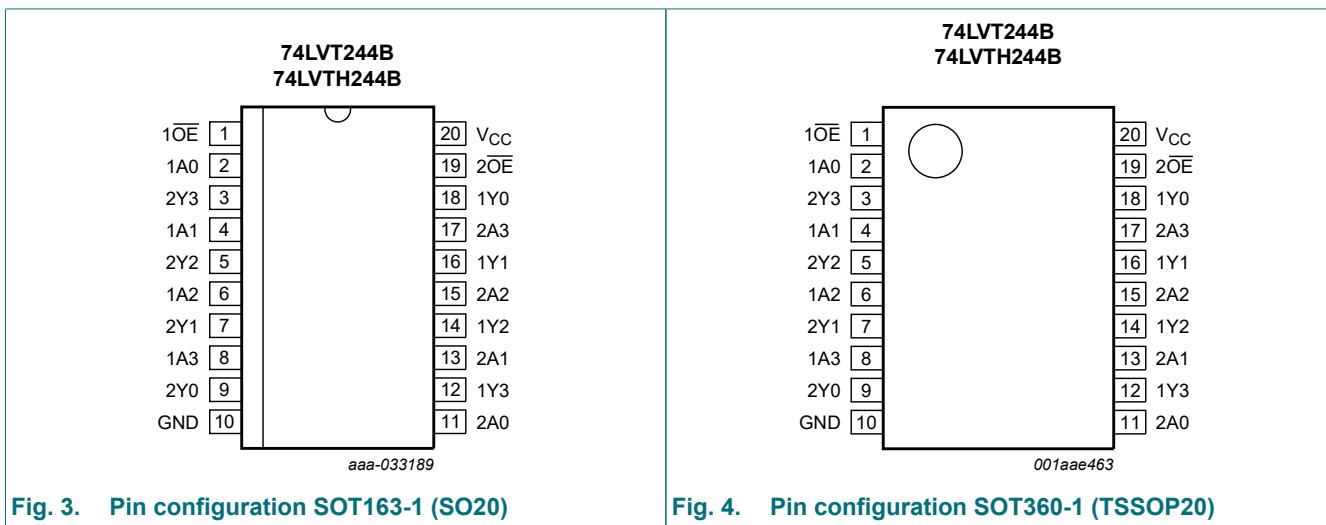
Type number	Package			
	Temperature range	Name	Description	Version
74LVT244BD	-40 °C to +85 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVTH244BD				
74LVT244BPW	-40 °C to +85 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVTH244BPW				

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 19	output enable input (active low)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2Y0, 2Y1, 2Y2, 2Y3	9, 7, 5, 3	data output
GND	10	ground (0 V)
2A0, 2A1, 2A2, 2A3	11, 13, 15, 17	data input
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
V <sub>CC</sub>	20	supply voltage

## 6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage		[1] -0.5	+7.0	V
V <sub>O</sub>	output voltage	output in OFF-state or HIGH-state	[1] -0.5	+7.0	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
I <sub>O</sub>	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		[2] -	150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 to +85 °C	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.7	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$I_{OH}$	HIGH-level output current		-32	-	-	mA
$I_{OL}$	LOW-level output current	none	-	-	32	mA
		current duty cycle $\leq 50\%$ ; $f_i \geq 1$ kHz	-	-	64	mA
$T_{amb}$	ambient temperature	in free-air	-40	-	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b><math>T_{amb} = -40\text{ }^{\circ}\text{C}</math> to <math>+85\text{ }^{\circ}\text{C}</math></b>						
$V_{IK}$	input clamping voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{IK} = -18\text{ mA}$	-1.2	-0.9	-	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC} - 2.0$	$V_{CC} - 2.1$	-	V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OH} = -8\text{ mA}$	2.4	2.5	-	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OH} = -32\text{ mA}$	2.0	2.2	-	V
$V_{OL}$	LOW-level output voltage	$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 100\text{ }\mu\text{A}$	-	0.1	0.2	V
		$V_{CC} = 2.7\text{ V}$ ; $I_{OL} = 24\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 16\text{ mA}$	-	0.25	0.4	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 32\text{ mA}$	-	0.3	0.5	V
		$V_{CC} = 3.0\text{ V}$ ; $I_{OL} = 64\text{ mA}$	-	0.4	0.55	V
$I_I$	input leakage current	all input pins				
		$V_{CC} = 0\text{ V}$ or $3.6\text{ V}$ ; $V_I = 5.5\text{ V}$	-	0.1	10	$\mu\text{A}$
		control pins				
		$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$ or GND	-1	$\pm 0.1$	1	$\mu\text{A}$
		data pins [2]				
	$V_{CC} = 3.6\text{ V}$ ; $V_I = V_{CC}$	-	0.1	1	$\mu\text{A}$	
	$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$	-5	-1	-	$\mu\text{A}$	
$I_{OFF}$	power-off leakage current	$V_{CC} = 0\text{ V}$ ; $V_I$ or $V_O = 0\text{ V}$ to $4.5\text{ V}$	-100	1	+100	$\mu\text{A}$
$I_{BHL}$	bus hold LOW current	$V_{CC} = 3\text{ V}$ ; $V_I = 0.8\text{ V}$	75	130	-	$\mu\text{A}$
$I_{BHH}$	bus hold HIGH current	$V_{CC} = 3\text{ V}$ ; $V_I = 2.0\text{ V}$	-	-140	-75	$\mu\text{A}$
$I_{BHLO}$	bus hold LOW overdrive current	$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$ [3]	500	-	-	$\mu\text{A}$
$I_{BHHO}$	bus hold HIGH overdrive current	$V_{CC} = 3.6\text{ V}$ ; $V_I = 0\text{ V}$ to $3.6\text{ V}$	-	-	-500	$\mu\text{A}$
$I_{EX}$	external current	nYn output in HIGH-state when $V_O > V_{CC}$ ; $V_O = 5.5\text{ V}$ ; $V_{CC} = 3.3\text{ V}$	-	60	125	$\mu\text{A}$

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$I_{O(pu/pd)}$	power-up/power-down output current	$V_{CC} \leq 1.2 \text{ V}$ ; $V_O = 0.5 \text{ V to } V_{CC}$ ; $V_I = \text{GND or } V_{CC}$ ; $n\overline{OE} = \text{don't care}$	[4] -100	$\pm 1$	+100	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = V_{IH} \text{ or } V_{IL}$				
		$V_O = 3.0 \text{ V}$	-	1	5	$\mu\text{A}$
		$V_O = 0.5 \text{ V}$	-5	-1	-	$\mu\text{A}$
$I_{CC}$	supply current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = \text{GND or } V_{CC}$ ; $I_O = 0 \text{ A}$				
		output HIGH	-	0.13	0.19	mA
		output LOW	-	2	5	mA
		outputs disabled	[5] -	0.13	0.19	mA
$\Delta I_{CC}$	additional supply current	per input pin; $V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ ; one input at $V_{CC} - 0.6 \text{ V}$ and other inputs at $V_{CC}$ or GND	[6] -	0.1	0.2	mA
$C_I$	input capacitance	$V_I = 0 \text{ V or } 3.0 \text{ V}$	-	4	-	pF
$C_O$	output capacitance	outputs disabled; $V_O = 0 \text{ V or } 3.0 \text{ V}$	-	8	-	pF

[1] Typical values are measured at  $T_{amb} = 25 \text{ }^\circ\text{C}$ .

[2] Unused pins at  $V_{CC}$  or GND.

[3] This is the bus hold overdrive current required to force the input to the opposite logic state.

[4] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms.

From  $V_{CC} = 1.2 \text{ V to } V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  a transition time of 100  $\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25 \text{ }^\circ\text{C}$  only.

[5]  $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.

[6] This is the increase in supply current for each input at  $V_{CC} - 0.6 \text{ V}$ .

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

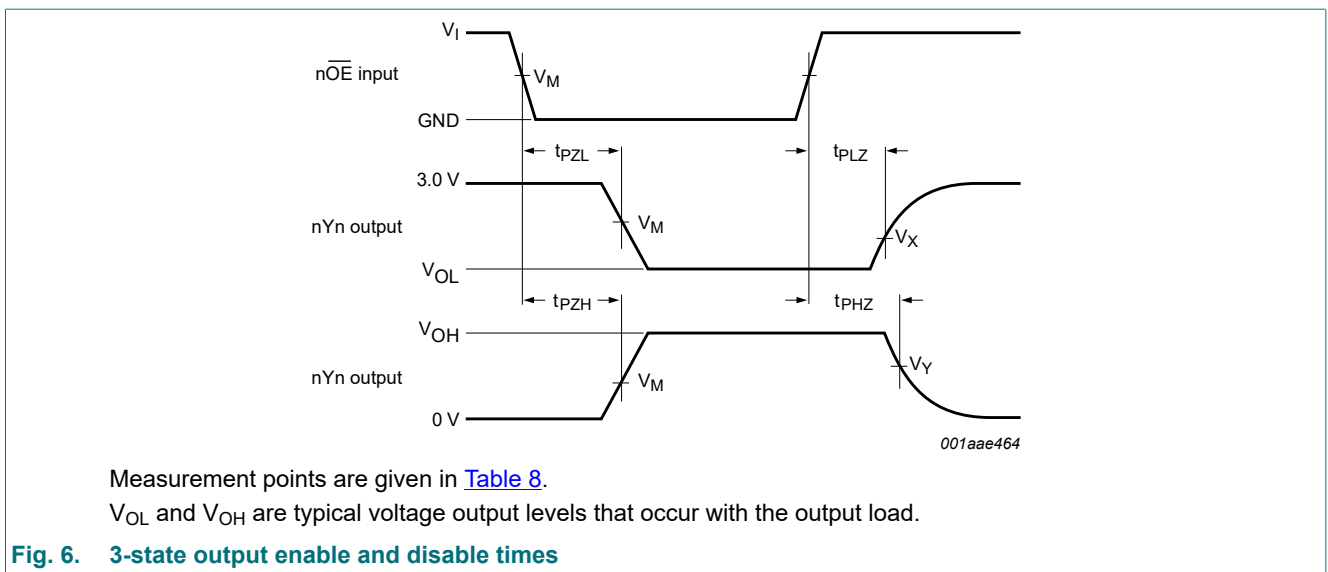
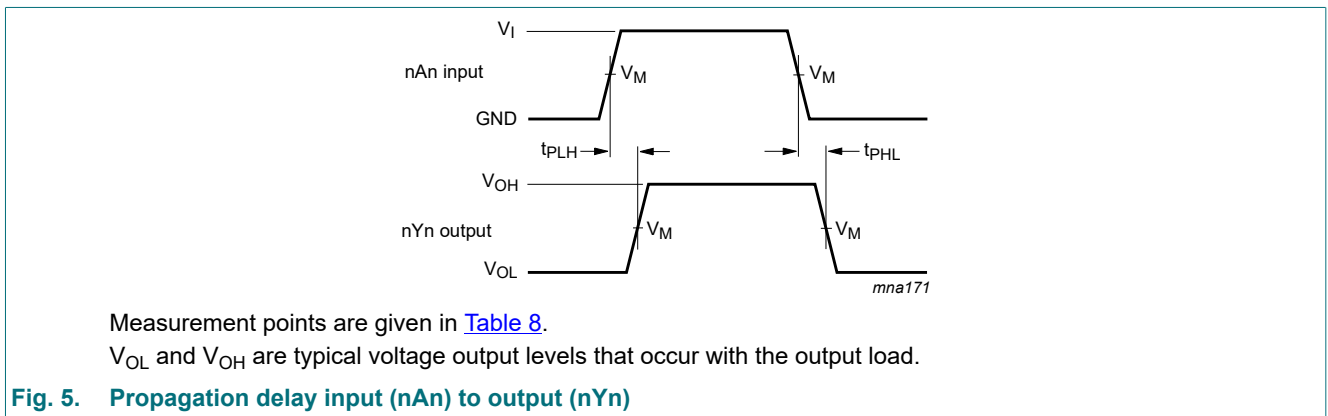
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
<b><math>T_{amb} = -40 \text{ }^\circ\text{C to } +85 \text{ }^\circ\text{C}</math></b>						
$t_{PLH}$	LOW to HIGH propagation delay	$nA_n$ to $nY_n$ ; see Fig. 5				
		$V_{CC} = 2.7 \text{ V}$	-	-	3.8	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.1	1.9	3.5	ns
$t_{PHL}$	HIGH to LOW propagation delay	$nA_n$ to $nY_n$ ; see Fig. 5				
		$V_{CC} = 2.7 \text{ V}$	-	-	3.6	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.3	2.0	3.3	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$n\overline{OE}$ to $nY_n$ ; see Fig. 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	5.3	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.1	2.8	4.5	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$n\overline{OE}$ to $nY_n$ ; see Fig. 6				
		$V_{CC} = 2.7 \text{ V}$	-	-	4.9	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.4	2.3	4.4	ns

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
t <sub>PHZ</sub>	HIGH to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 6				
		V <sub>CC</sub> = 2.7 V	-	-	4.5	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 6				
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.9	2.9	4.4	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 6				
		V <sub>CC</sub> = 2.7 V	-	-	4.4	ns
t <sub>PLZ</sub>	LOW to OFF-state propagation delay	n $\overline{\text{OE}}$ to nYn; see Fig. 6				
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.8	2.5	4.4	ns

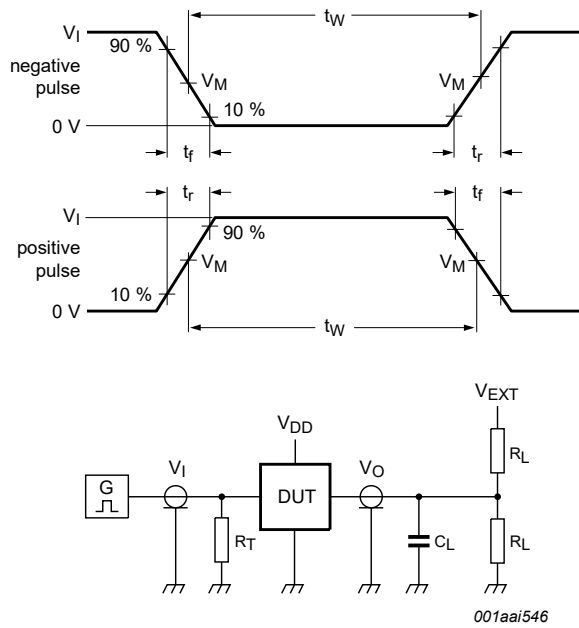
[1] Typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

### 10.1. Waveforms and test circuit



**Table 8. Measurement points**

Input	Output		
V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V



Test data is given in [Table 9](#).

Definitions test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = Test voltage for switching times.

**Fig. 7. Test circuit for measuring switching times**

**Table 9. Test data**

Input				Load		$V_{EXT}$		
$V_I$	$f_i$	$t_w$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



Fig. 8. Package outline SOT163-1 (SO20)



TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

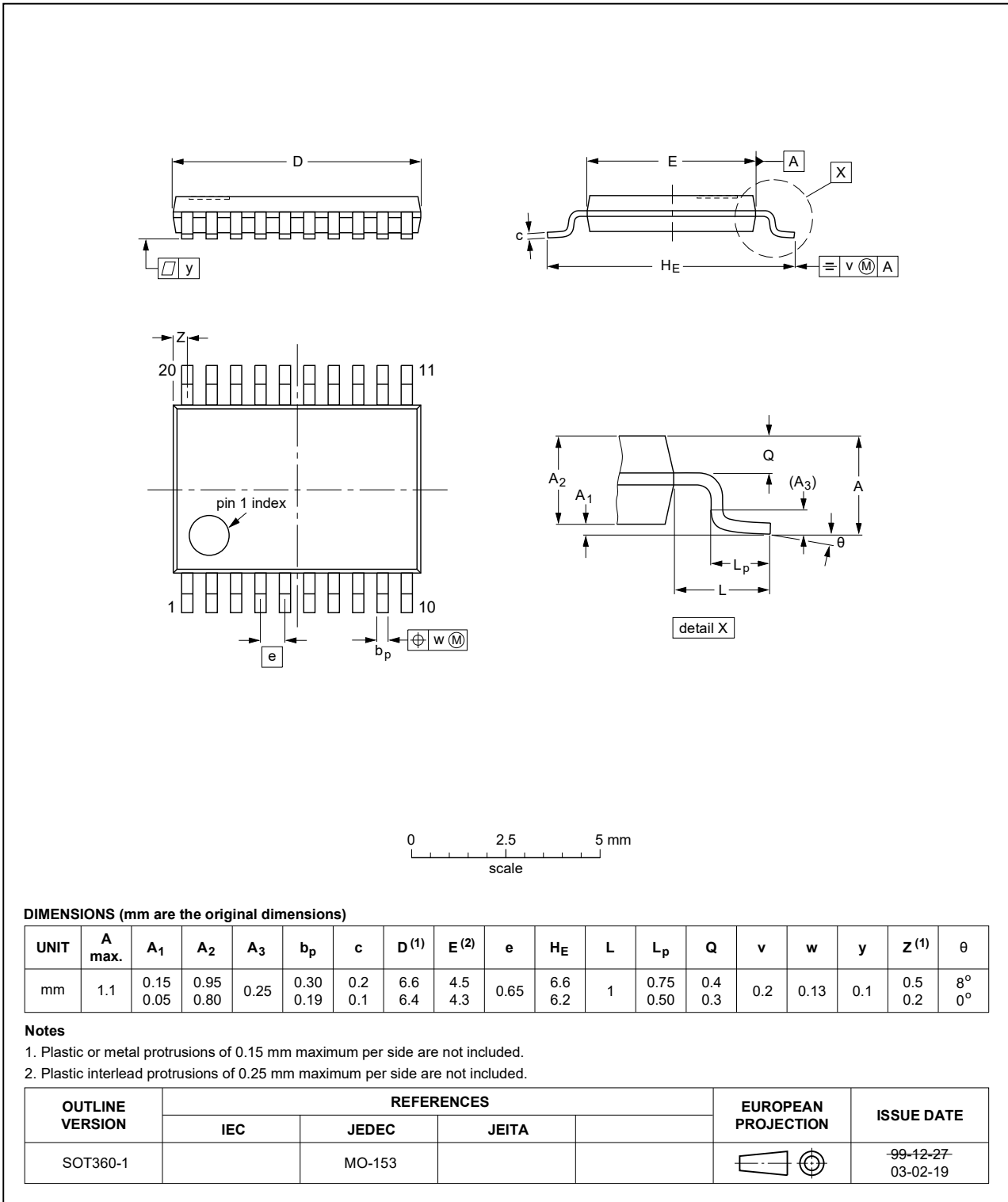


Fig. 9. Package outline SOT360-1 (TSSOP20)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH244B v.6	20210812	Product data sheet	-	74LVT_LVTH244B v.5
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVT244BDB (SOT339-1/SSOP20) removed.</li> </ul>			
74LVT_LVTH244B v.5	20210212	Product data sheet	-	74LVT_LVTH244B v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number 74LVTH244BDB (SOT339-1 / SSOP20) removed.</li> <li><a href="#">Section 1</a> and <a href="#">Section 2</a> updated.</li> </ul>			
74LVT_LVTH244B v.4	20170614	Product data sheet	-	74LVT_LVTH244B v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
74LVT_LVTH244B v.3	20060303	Product data sheet	-	74LVT244B v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li> <li><a href="#">Section 3</a>: Added type numbers 74LVTH244BD, 74LVTH244BDB and 74LVTH244BPW.</li> </ul>			
74LVT244B v.2	20030919	Product specification	-	74LVT244B v.1
74LVT244B v.1	19981101	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
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