

SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE BCD TO 10-LINE DECIMAL DECODERS

SDLS109 – MARCH 1974 – REVISED MARCH 1988

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
4-Line-to-16-Line Decoders
3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

TYPES	TYPICAL POWER DISSIPATION	TYPICAL PROPAGATION DELAYS
'42A	140 mW	17 ns
'LS42	35 mW	17 ns

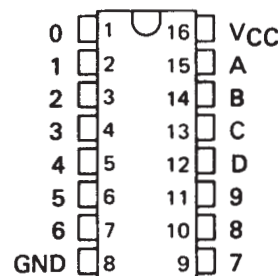
description

These monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

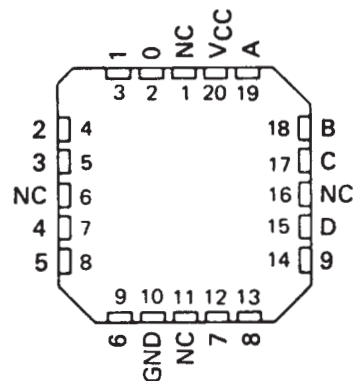
The '42A and 'LS42 feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

The SN5442A and SN54LS42 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN7442A and SN74LS42 are characterized for operation from 0°C to 70°C .

SN5442A, SN54LS42 . . . J OR W PACKAGE
SN7442A . . . N PACKAGE
SN74LS42 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS42 . . . FK PACKAGE
(TOP VIEW)

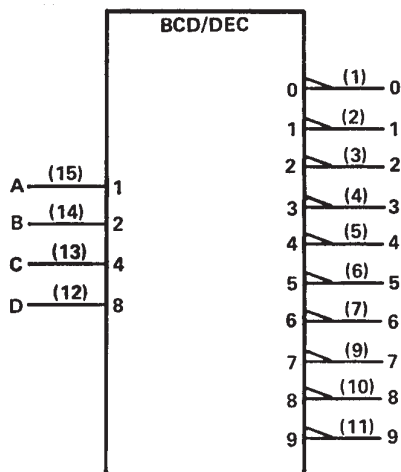


NC - No internal connection

SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE BCD TO 10-LINE DECIMAL DECODERS

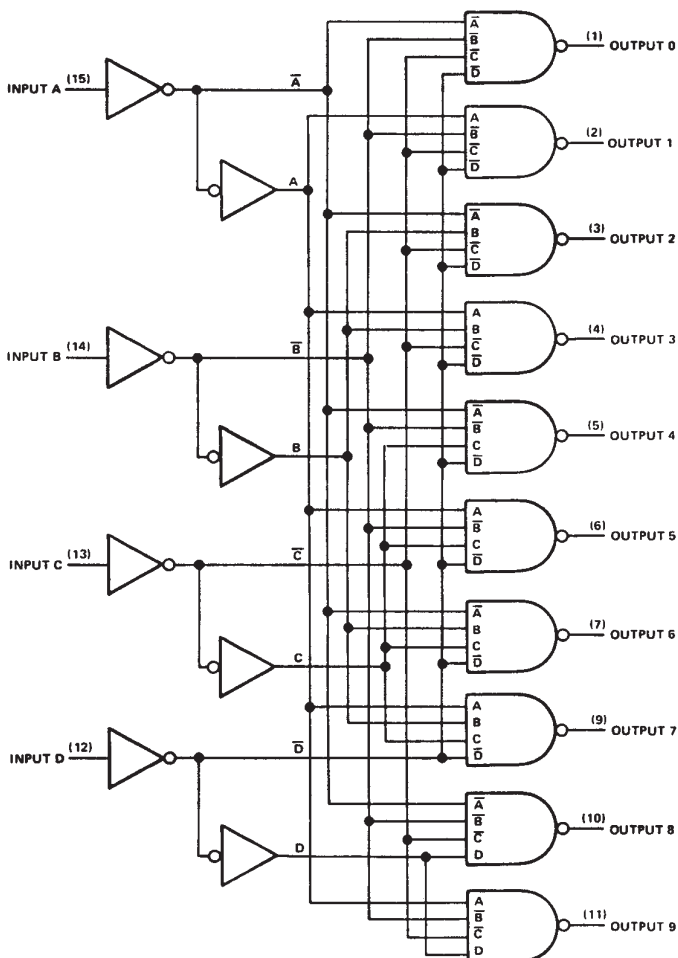
SDLS109 – MARCH 1974 – REVISED MARCH 1988

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



Pin numbers shown are for D, J, N, and W packages.

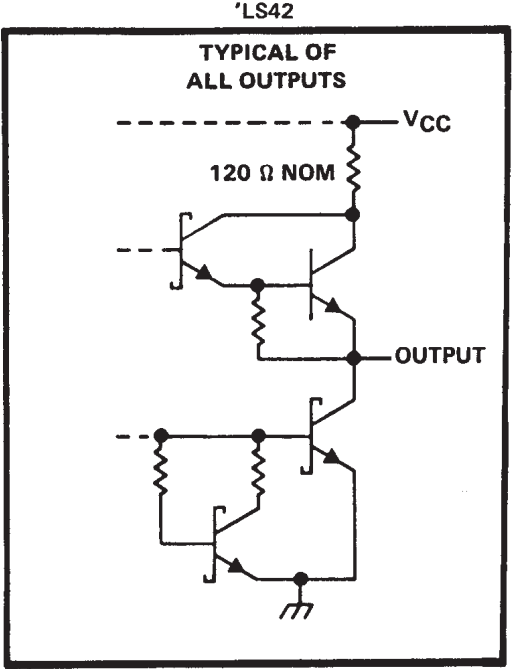
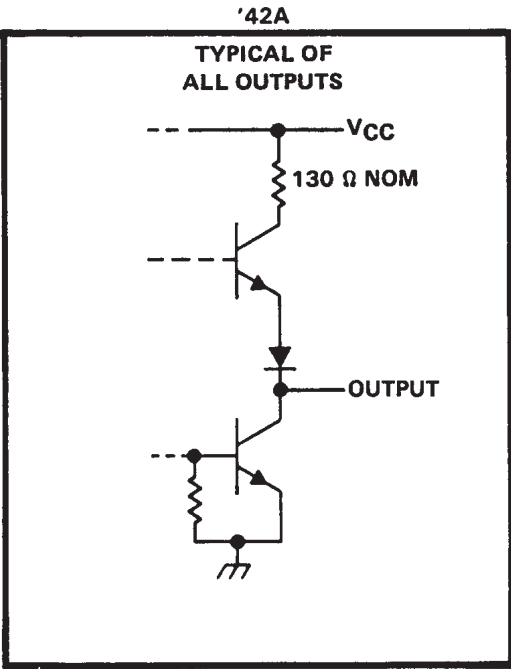
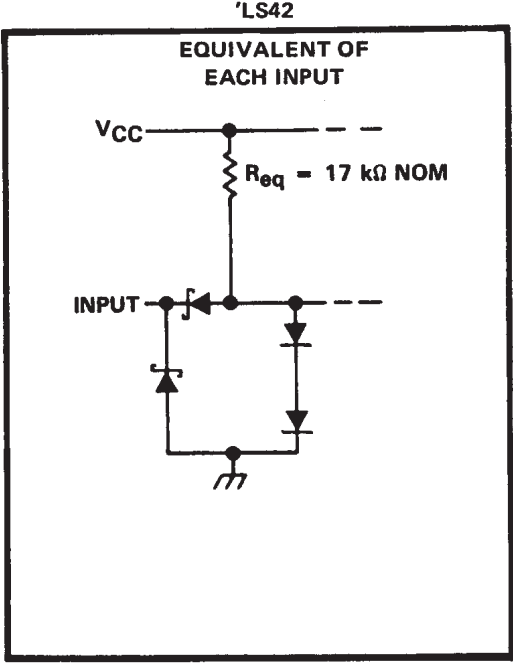
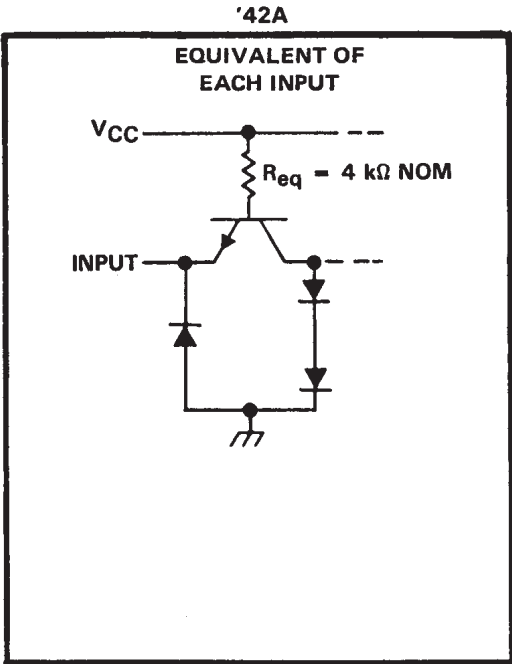


POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5442A, SN54LS42, SN7442A, SN74LS42
 4-LINE BCD TO 10-LINE DECIMAL DECODERS

SDLS109 – MARCH 1974 – REVISED MARCH 1988

schematics of inputs and outputs



SN5442A, SN54LS42, SN7442A, SN74LS42

4-LINE BCD TO 10-LINE DECIMAL DECODERS

SDLS109 – MARCH 1974 – REVISED MARCH 1988

FUNCTION TABLE

NO.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

- Supply voltage, V_{CC} (see Note 1) 7 V
- Input voltage: '42A 5.5 V
- 'LS42 7 V
- Operating free-air temperature range: SN5442A, SN54LS42 -55°C to 125°C
- SN7442A, SN74LS42 0°C to 70°C
- Storage temperature range -65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN5442A, SN54LS42, SN7442A, SN74LS42

4-LINE BCD TO 10-LINE DECIMAL DECODERS

SDLS109 – MARCH 1974 – REVISED MARCH 1988

recommended operating conditions

	SN5442A			SN7442A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN5442A			SN7442A			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.8			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = 0.8 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.4 \text{ V}$			40			40	μ A
I_{IL} Low level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-1.6			-1.6	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-55	-18		-55	mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		28	41		28	56	mA

[†] For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 2: I_{CC} is measured with all outputs open and all inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF}, R_L = 400 \Omega, \text{ See Note 3}$		14	25	ns
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			17	30	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic			10	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic			17	30	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

SN5442A, SN54LS42, SN7442A, SN74LS42 4-LINE BCD TO 10-LINE DECIMAL DECODERS

SDLS109 – MARCH 1974 – REVISED MARCH 1988

recommended operating conditions

	SN54LS42			SN74LS42			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN54LS42			SN74LS42			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V
		$I_{OL} = 8 \text{ mA}$				0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current §	$V_{CC} = \text{MAX}$	-20		-100		-20		mA
I_{CC} Supply current	$V_{CC} = \text{MAX}, \text{ See Note 2}$		7	13		7	13	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2. I_{CC} is measured with all outputs open and inputs grounded.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega, \text{ See Note 3}$		15	25	ns	
t_{PHL} Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic			20	30	ns	
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic				15	25	ns
t_{PLH} Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic				20	30	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.



IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

PRODUCT FOLDER | PRODUCT INFO: [FEATURES](#) | [DESCRIPTION](#) | [DATASHEETS](#) | [PRICING/AVAILABILITY/PKG](#) | [APPLICATION NOTES](#) | [RELATED DOCUMENTS](#)

PRODUCT SUPPORT: [TRAINING](#)

SN74LS42, 4-Line BCD To 10-Line Decimal Decoders

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN74LS42
Voltage Nodes (V)	5
Vcc range (V)	4.75 to 5.25
Input Level	TTL
Output Level	TTL
Output Drive (mA)	-0.4/8
Output	2S
From	4
To	10

FEATURES

[▲Back to Top](#)

- All Outputs Are High for Invalid Input Conditions
- Also for Application as
 - 4-Line-to-16-Line Decoders
 - 3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

DESCRIPTION

[▲Back to Top](#)

These monolithic BCD-to-decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A and 'LS42 feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

The SN5442A and SN54LS42 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN7442A and SN74LS42 are characterized for operation from 0°C to 70°C.

TECHNICAL DOCUMENTS

[▲Back to Top](#)

To view the following documents, [Acrobat Reader 4.0](#) is required.

To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

[▲Back to Top](#)

Full datasheet in Acrobat PDF: [sn74ls42.pdf](#) (213 KB) (Updated: 03/01/1988)

View Application Notes for [Digital Logic](#)

- [Designing With Logic \(Rev. C\)](#) (SDYA009C - Updated: 06/01/1997)
- [Designing with the SN54/74LS123 \(Rev. A\)](#) (SDLA006A - Updated: 03/01/1997)
- [Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits](#) (SZZA026 - Updated: 06/20/2001)
- [Input and Output Characteristics of Digital Integrated Circuits](#) (SDYA010 - Updated: 10/01/1996)
- [Live Insertion](#) (SDYA012 - Updated: 10/01/1996)

RELATED DOCUMENTSView Related Documentation for [Digital Logic](#)

- [Logic Reference Guide](#) (SCYB004, 1032 KB - Updated: 10/23/2001)
- [Logic Selection Guide Second Half 2002 \(Rev. R\)](#) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- [Military Semiconductors Selection Guide 2002 \(Rev. B\)](#) (SGYC003B, 1648 KB - Updated: 04/22/2002)

PRICING/AVAILABILITY/PKG

DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY \$US	STD PACK QTY	IN STOCK	IN PROGRESS QTY DATE	LEAD TIME	DISTRIBUTOR COMPANY REGION	IN STOCK	PURCHASE
SN74LS42D	ACTIVE	SOP (D) 16	0 TO 70	View Contents	1KU 0.69	40	N/A*	3634 03 Oct	4 WKS			
								> 10k 10 Oct				
								> 10k 17 Oct				
SN74LS42DR	OBSOLETE	SOP (D) 16	0 TO 70	View Contents	1KU		N/A*		Not Available			
SN74LS42N	ACTIVE	PDIP (N) 16	0 TO 70	View Contents	1KU 0.69	25	15	4075 24 Sep	4 WKS	Avnet AMERICA	> 1k	BUY NOW
								645 02 Oct				
								898 03 Oct				
								4531 04 Oct				
								> 10k 11 Oct				
SN74LS42NSR	ACTIVE	SOP (NS) 16		View Contents	1KU 0.69	2000	N/A*	4508 04 Oct	4 WKS			
								2302 11 Oct				
								> 10k 18 Oct				

Table Data Updated on: 9/26/2002

