High Fidelity, Low Power, Integrated Stereo Audio Amplifier

Data Sheet

SSM6322

FEATURES

- Flexible architecture to interface with all digital-to-analog converters (DACs)
  - Accepts differential current or voltage input (provides single-ended voltage output)
- High output current drive capability
  - Greater than 100 mA rms output current
  - Accurately reproduces large music transients into heavy loads (16 Ω to 32 Ω)
- Excellent audio fidelity
  - −121 dB total harmonic distortion plus noise (THD + N) at 1 kHz, 2 V rms output with ±5 V supply and 32 Ω load
  - Low output integrated noise (10 Hz to 22 kHz) of 1.8 μV rms with A-weighted filter
- Supply range: ±3.3 V to ±6 V (typical)
- Low power operation
  - Enabled: 60 mW, V_{CC} = +5 V, V_{EE} = −5 V
  - Disabled/voice select: <30 μA
- Low power disable mode with high output impedance
  - High-Z in power-down mode eliminating voice mode switch from the high fidelity path
- Greater than 87 dB power supply rejection ratio (PSRR) at 20 kHz
- Adjustable input common-mode voltage with resistor programmable reference voltage
  - 1.45 V (typical) with no external components
- Capable of two single-pole, low-pass filters in series
  - 2.2 nF maximum input capacitor
  - Second filter between the GAINx and FILTx pins
- Pop and click noise suppression
- Signal chain integration supports small printed circuit board (PCB) area
  - Compact 4 mm × 4 mm LFCSP package

APPLICATIONS

- High fidelity headphone drivers
  - Mobile phones
  - Bluetooth speakers and headphones
  - Gaming notebooks and tablets
- A/V receivers
- Professional audio equipment
- Audio test equipment
- Automobile infotainment systems

FUNCTIONAL BLOCK DIAGRAM

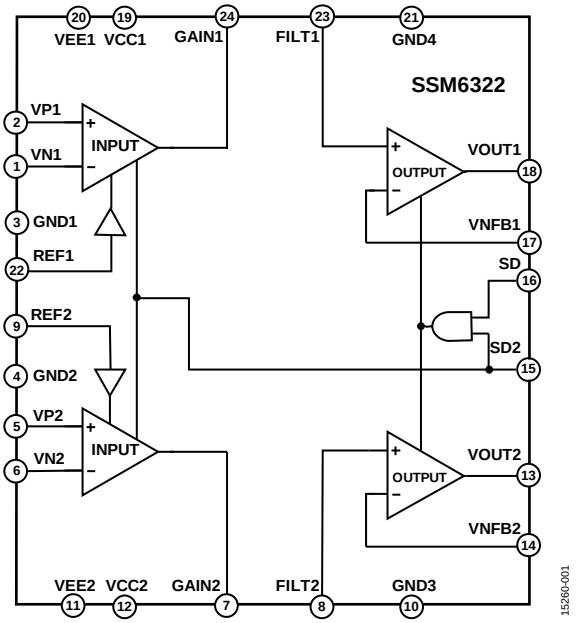

Figure 1.

GENERAL DESCRIPTION

The SSM6322 is an integrated, dual-channel audio amplifier solution that interfaces directly with audio DAC/CODEC, maximizing the fidelity of high fidelity audio signal chains. The highly efficient design of the SSM6322 delivers outstanding audio performance while minimizing power dissipation for maximum battery life in portable applications.

The SSM6322 features −121 dB THD + N at 1 kHz, along with very low output noise from 20 Hz to 20 kHz. The low power operation, high peak output current, and high PSRR make the SSM6322 an ideal candidate for applications that require high fidelity audio, high dynamic range, precision, and low power. This highly integrated drive solution also reduces development time while reducing board space and minimizing external components.

The SSM6322 is available in a 24-lead LFCSP package. The SSM6322 operates over the industrial temperature of −40°C to +85°C.

Rev. 0

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REVISION HISTORY

3/2017—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, reference voltage (V_{REF}) = 0 V, feedback resistor (R_F) = gain resistor (R_G) = 1 kΩ (see Figure 38), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Gain Bandwidth	R_{IN1} = 1 kΩ, R_{IN2} = 1 kΩ (see Figure 38), output voltage (V_{OUT}) = 0.2 V p-p		25		MHz
Slew Rate	Gain = 1, V_{OUT} = 2 V step		18		V/µs
Channel Separation	1 kHz to 10 kHz, input voltage (V_{IN}) = 5 V p-p, R_L = 600 Ω, 32 Ω, 16 Ω		−140		dB
DISTORTION PERFORMANCE					
THD + N	1 kHz, V_{OUT} = 2 V rms, low-pass filter = 80 kHz, R_L = 600 Ω		−122		dB
	1 kHz, V_{OUT} =2 V rms, low-pass filter = 80 kHz, R_L = 32 Ω		−121		dB
	1 kHz, V_{OUT} = 1.6 V rms, low-pass filter = 80 kHz, R_L = 16 Ω		−118		dB
Intermodulation Distortion (IMD)	SMPTE two-tone, 4:1 (60 Hz and 7 kHz), gain = 1, V_{OUT} = 2 V rms, R_L = 600 Ω, 90 kHz measurement bandwidth		−125		dB
	CCIF two-tone (19 kHz and 20 kHz), gain = 1, V_{OUT} = 2 V rms, R_L = 600 Ω, 90 kHz measurement bandwidth		−131		dB
NOISE PERFORMANCE					
A-Weight Output Noise	f = 10 Hz to 22 kHz		1.8		µV rms
Input Voltage Noise	f = 10 Hz		5.2		nV/√Hz
	f = 100 kHz		3.6		nV/√Hz
Input Current Noise	f = 10 Hz		10		pA/√Hz
	f = 100 kHz		1.2		pA/√Hz
DC PERFORMANCE					
Output Offset Voltage			90	250	µV
Output Offset Voltage Drift			1.5	7.5	µV/°C
Input Bias Current		−2.4	−1.8	−1	µA
Input Offset Current			60	320	nA
Open-Loop Gain	V_{OUT} = ±2.3 V, R_L = 600 Ω	107	120		dB
INPUT CHARACTERISTICS					
Input Capacitance			2		pF
Input Common-Mode Voltage Range	I_{DIFF} = 3 mA		±1.5		V
Common-Mode Rejection	V_{CM} = ±1 V	113	140		dB
V_{REF1}/V_{REF2}					
Open Circuit Voltage	Referenced to ground		1.45		V
Output Current			15		µA
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
Each Output	R_L = 600 Ω	±3.3	±3.4		V
	R_L = 32 Ω	±2.8	±2.9		V
	R_L = 16 Ω	±2.0	±2.6		V
Output Current	R_L = 16 Ω, rms voltage (V_{RMS}) = 1.6 V, THD + N= −118 dB		100		mA rms
Short-Circuit Current	R_L = 10 Ω; source/sink		+240/−190		mA
Closed-Loop Output Impedance	10 Hz to 20 kHz		0.04		Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			±3.3 to ±6		V
Quiescent Current	$V_{SD} = V_{SD2} = V_{CCx}$, V_{REF} = 0 V, per channel		3	3.35	mA
	−40°C ≤ T_A ≤ +85°C		3.1		mA
Quiescent Current Power-Down Mode	V_{SD} = 0 V, $V_{SD2} = V_{CCx}$, per channel		1.4		mA
	$V_{SD} = V_{SD2}$ = 0 V, per channel		15		µA
DC Power Supply Rejection Ratio	Supply voltage (V_{SY}) = 3.3 V to 5.5 V	115	140		dB
AC Power Supply Rejection Ratio	20 kHz		87		dB
POWER-DOWN INPUTS					
Logic High	Chip on, referenced to ground		>1.5		V
Logic Low	Chip off, referenced to ground		<0.75		V

±3.3 V SUPPLY

T_A = 25°C, V_{REF} = 0 V, $R_F = R_G$ = 1 kΩ (see Figure 38), unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Gain Bandwidth	R_{IN1} = 1 kΩ, R_{IN2} = 1 kΩ (see Figure 38), V_{OUT} = 0.2 V p-p		25		MHz
Slew Rate	Gain = 1, V_{OUT} = 2 V step		14		V/µs
Channel Separation	1 kHz to 10 kHz, V_{IN} = 1 V p-p, R_L = 600 Ω, 32 Ω, and 16 Ω		−140		dB
DISTORTION PERFORMANCE					
THD + N	1 kHz, V_{OUT} = 1 V rms, low-pass filter = 80 kHz, R_L = 600 Ω		−116		dB
	1 kHz, V_{OUT} = 1 V rms, low-pass filter = 80 kHz, R_L = 32 Ω		−116		dB
	1 kHz, V_{OUT} = 0.9 V rms, low-pass filter = 80 kHz, R_L = 16 Ω		−111		dB
NOISE PERFORMANCE					
A-Weight Output Noise	f = 10 Hz to 22 kHz		1.8		µV rms
Input Voltage Noise	f = 10 Hz		5.2		nV/√Hz
	f = 100 kHz		3.6		nV/√Hz
Input Current Noise	f = 10 Hz		10		pA/√Hz
	f = 100 kHz		1.2		pA/√Hz
DC PERFORMANCE					
Output Offset Voltage			90	250	µV
Output Offset Voltage Drift			1.5	7.5	µV/°C
Input Bias Current		−2.4	−1.8	−1	µA
Input Offset Current			60	300	nA
Open-Loop Gain	V_{OUT} = ±2.3 V, R_L = 600 Ω	106	120		dB
INPUT CHARACTERISTICS					
Input Capacitance			2		pF
Input Common-Mode Voltage Range	Differential current (I_{DIFF}) = 3 mA		±0.3		V
Common-Mode Rejection	Common-mode voltage (V_{CM}) = ±0.3 V	109	135		dB
V_{REF1}/V_{REF2}					V
Open Circuit Voltage	Referenced to ground		1.45		V
Output Current			15		µA
OUTPUT CHARACTERISTICS					
Output Voltage Swing					
Each Output	R_L = 600 Ω	±1.6	±1.7		V
	R_L = 32 Ω	±1.4	±1.45		V
	R_L = 16 Ω	±1.2	±1.4		V
Output Current	R_L = 16 Ω, V_{RMS} = 0.9 V, THD + N = −111 dB		56		mA rms
Short-Circuit Current	R_L = 10 Ω		+115/−120		mA
Closed-Loop Output Impedance	10 Hz to 20 kHz		0.04		Ω

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			±3.3 to ±6		V
Quiescent Current	$V_{SD} = V_{SD2} = V_{CCx}$, V_{REF} = 0 V, per channel		2.9	3.35	mA
	−40°C ≤ T_A ≤ +85°C		3.0		mA
Quiescent Current Power-Down Mode	V_{SD} = 0 V, $V_{SD2} = V_{CCx}$		1.3		mA
	$V_{SD} = V_{SD2}$ = 0 V		10		µA
DC Power Supply Rejection Ratio	V_{SY} = 3.3 V to 5.5 V	115	140		dB
AC Power Supply Rejection Ratio	20 kHz		85		dB
POWER-DOWN INPUTS					
Logic High	Chip on, referenced to ground		>1.5		V
Logic Low	Chip off, referenced to ground		<0.75		V

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	
Single Supply	12.6 V
Dual Supply	±6.3 V
Exposed Pad Voltage	$-V_{SY}$ or ground
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to + 85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required. The values in Table 4 were obtained per JEDEC standard JESD51-12.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-24-15	47	3.3	°C/W

Board layout impacts thermal characteristics, such as θ_{JA}. When proper thermal management techniques are used, a better θ_{JA} value can be achieved.

Although the exposed pad can be left floating, it must be connected to an external V− plane or ground plane for proper thermal management.

Maximum Power Dissipation

The maximum safe power dissipation for the SSM6322 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the SSM6322. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality. The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the SSM6322 drive at the output.

The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{V_{OUT}^{\ 2}}{R_L}$$

Consider the rms output voltages. If R_L is referenced to $-V_{SY}$, as in single-supply operation, the total drive power is $V_{SY} \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_{SY}/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduce θ_{JA}.

Figure 2 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 24-lead LFCSP package on a JEDEC standard 4-layer board.

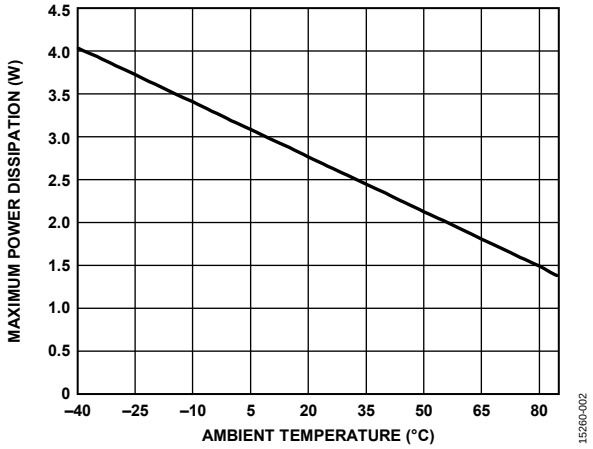


Figure 2. Maximum Power Dissipation vs. Ambient Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

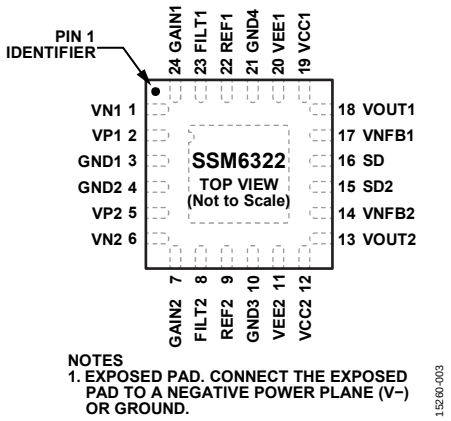


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VN1	Negative Input of Channel 1 Input Stage.
2	VP1	Positive Input of Channel 1 Input Stage.
3	GND1	Ground 1.
4	GND2	Ground 2.
5	VP2	Positive Input of Channel 2 Input Stage.
6	VN2	Negative Input of Channel 2 Input Stage.
7	GAIN2	Output of Channel 2 Input Stage.
9	FILT2	Positive Input of Channel 2 Output Stage.
9	REF2	Input Common-Mode Voltage of Channel 2 Input Stage.
10	GND3	Ground 3.
11	VEE2	Negative Supply 2. This pin is internally shorted to Pin 20.
12	VCC2	Positive Supply 2. This pin is internally shorted to Pin 19.
13	VOUT2	Output of Channel 2 Output Stage.
14	VNFB2	Negative Feedback of Channel 2 Output Stage.
15	SD2	Shuts Down Power for the Entire Device. This pin is referenced to ground.
16	SD	Shuts Down Power for the Output Stage. This pin is referenced to ground.
17	VNFB1	Negative Feedback of Channel 1 Output Stage.
18	VOUT1	Output of Channel 1 Output Stage.
19	VCC1	Positive Supply 1. This pin is internally shorted to Pin 12.
20	VEE1	Negative Supply 1. This pin is internally shorted to Pin 11.
21	GND4	Ground 4.
22	REF1	Input Common-Mode Voltage of Channel 1 Input Stage.
23	FILT1	Positive Input of Channel 1 Output Stage.
24	GAIN1	Output of Channel 1 Input Stage.
	EPAD	Exposed Pad. Connect the exposed pad to a negative power plane (V–) or ground.

TYPICAL PERFORMANCE CHARACTERISTICS

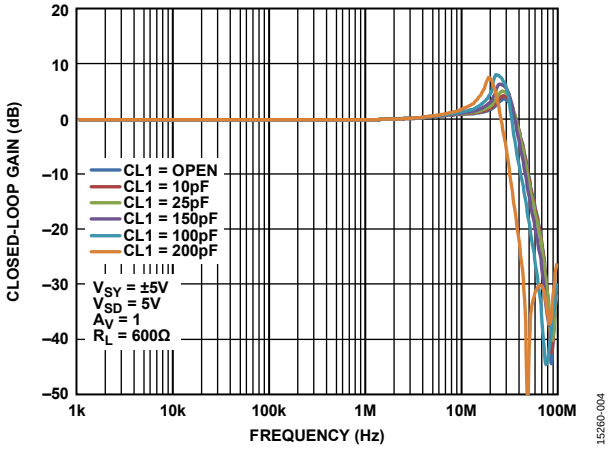


Figure 4. Frequency Response for Various Capacitive Loads, V_{SY} = ±5 V

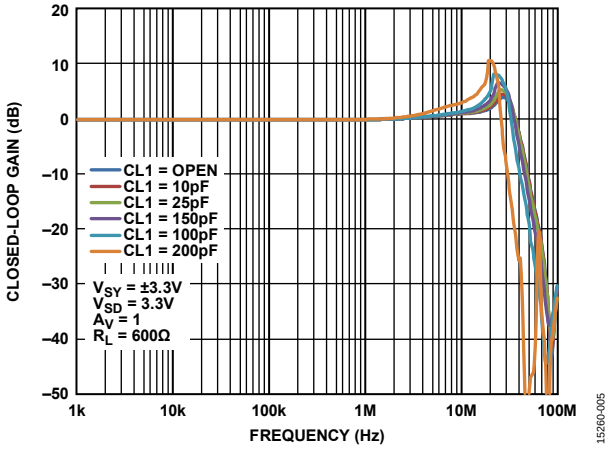


Figure 5. Frequency Response for Various Capacitive Loads, V_{SY} = ±3.3 V

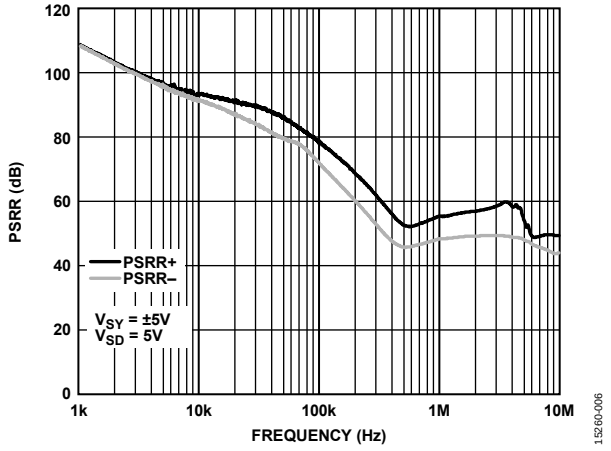


Figure 6. PSRR vs. Frequency, V_{SY} = ±5 V

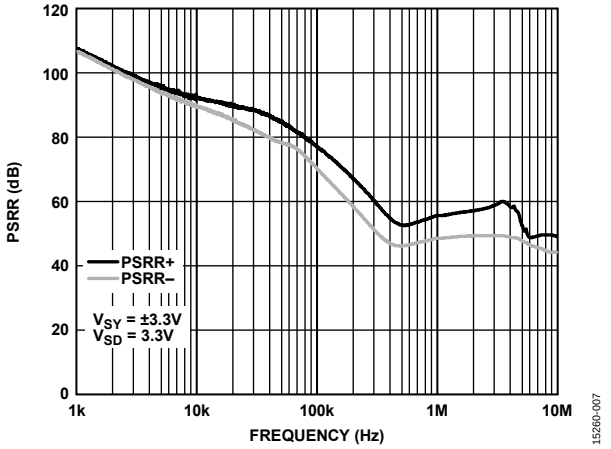


Figure 7. PSRR vs. Frequency, V_{SY} = ±3.3 V

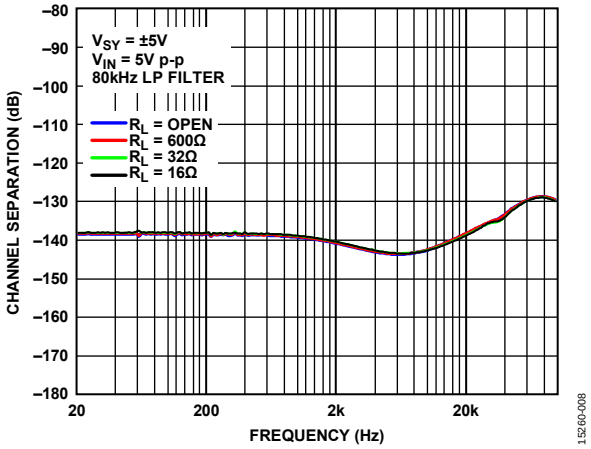


Figure 8. Channel Separation vs. Frequency, V_{SY} = ±5 V

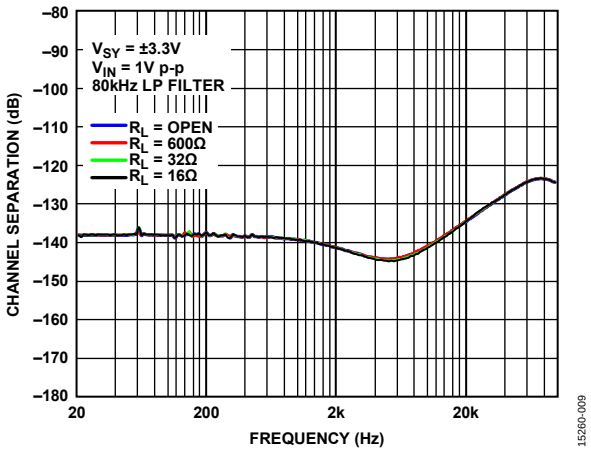


Figure 9. Channel Separation vs. Frequency, V_{SY} = ±3.3 V

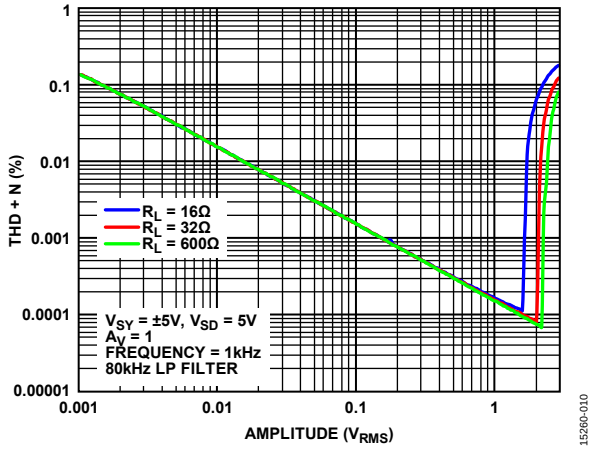


Figure 10. THD + N vs. Amplitude, V_{SY} = ±5 V

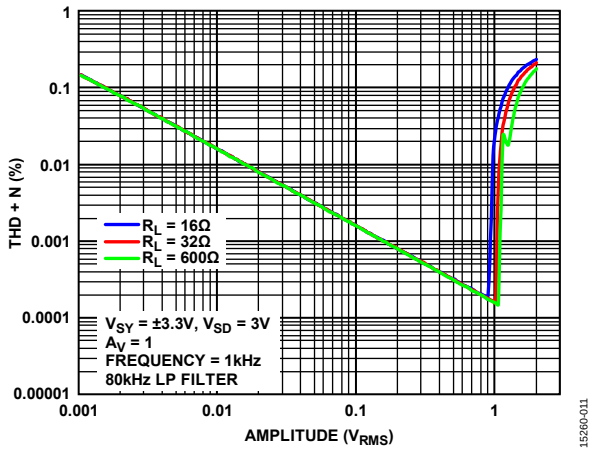


Figure 11. THD + N vs. Amplitude, V_{SY} = ±3.3 V

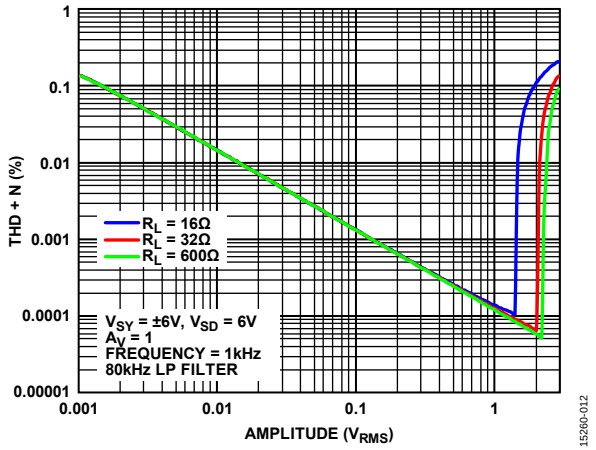


Figure 12. THD + N vs. Amplitude, V_{SY} = ±6 V

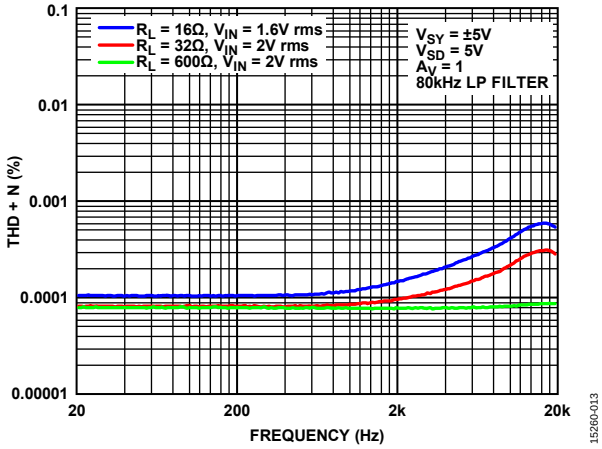


Figure 13. THD + N vs. Frequency, V_{SY} = ±5 V

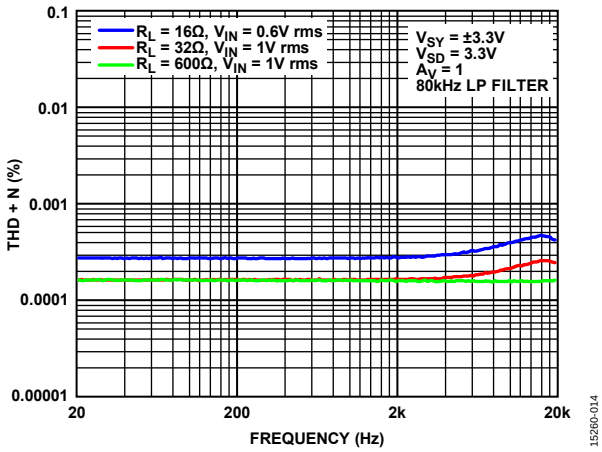


Figure 14. THD + N vs. Frequency, V_{SY} = ±3.3 V

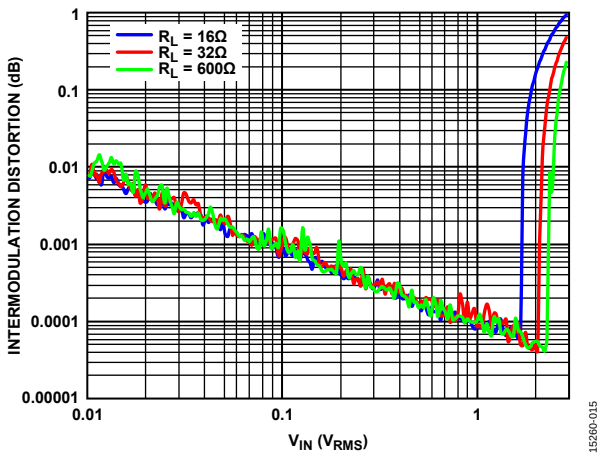


Figure 15. SMPTE vs. Input Voltage (V_{IN}), V_{SY} = ±5 V

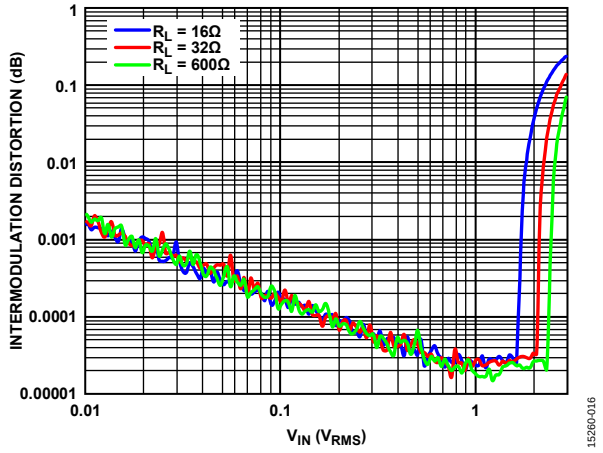


Figure 16. CCIF vs. Input Voltage (V_{IN}), V_{SY} = ±5 V

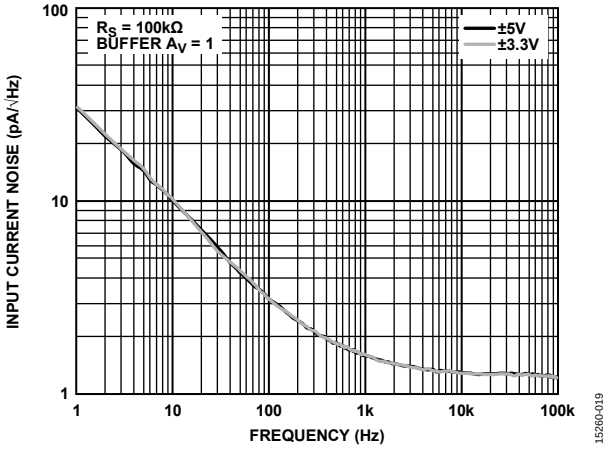


Figure 19. Input Current Noise vs. Frequency

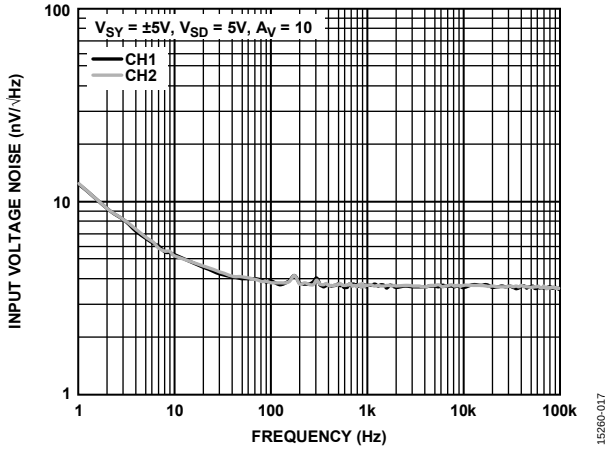


Figure 17. Input Voltage Noise vs. Frequency, V_{SY} = ±5 V

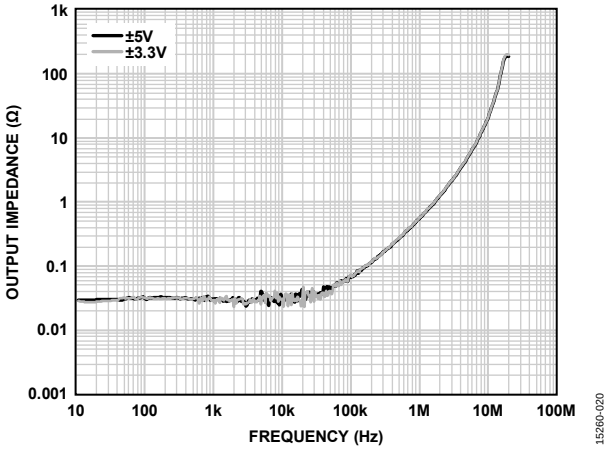


Figure 20. Enabled Output Impedance vs. Frequency

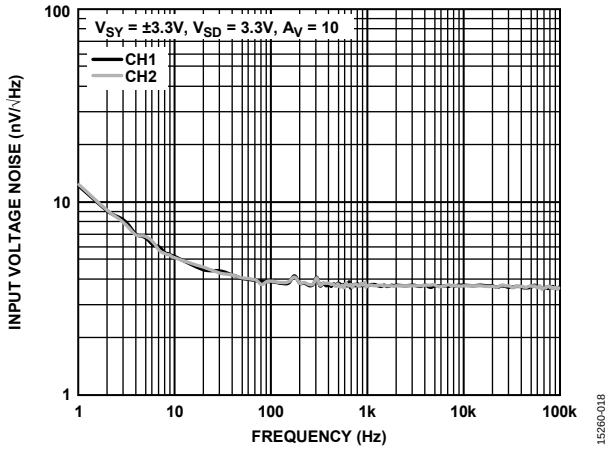


Figure 18. Input Voltage Noise vs. Frequency, V_{SY} = ±3.3 V

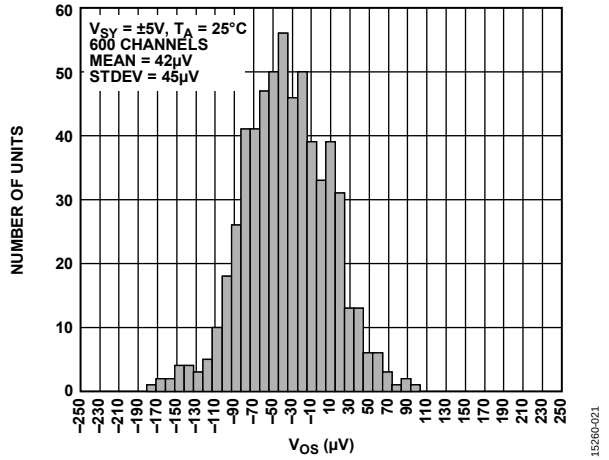


Figure 21. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±5 V

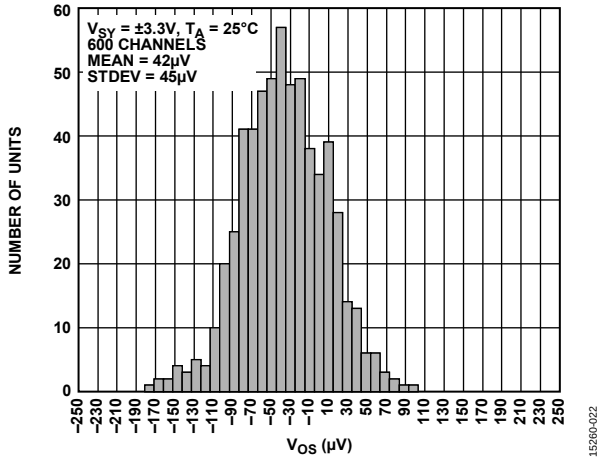


Figure 22. Input Offset Voltage (V_{OS}) Distribution, V_{SY} = ±3.3 V

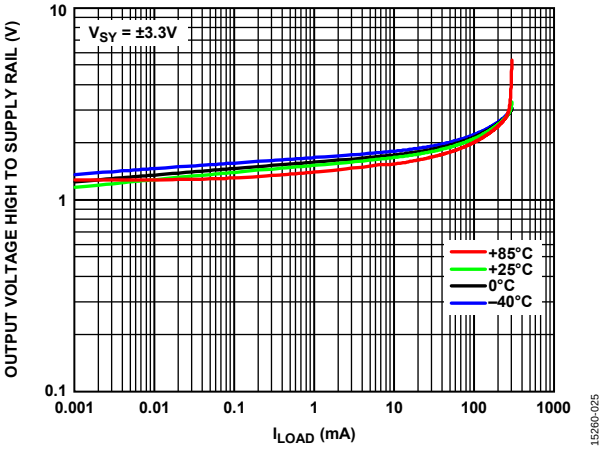


Figure 25. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = ±3.3 V

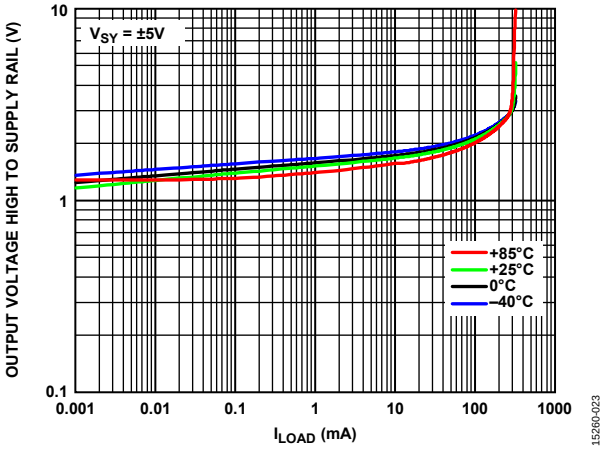


Figure 23. Output Voltage High (V_{OH}) to Supply Rail vs. Load Current (I_{LOAD}), V_{SY} = ±5 V

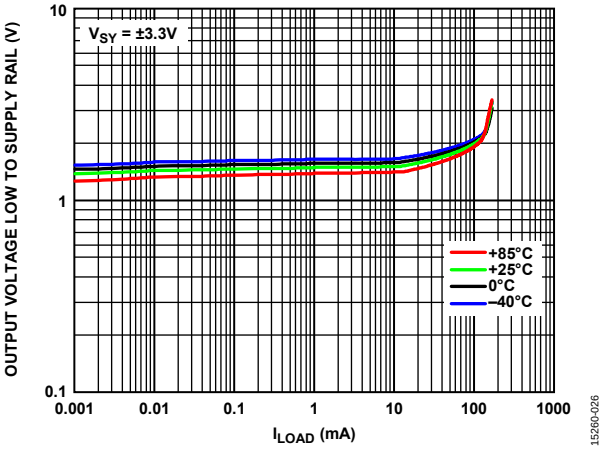


Figure 26. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) , V_{SY} = ±3.3 V

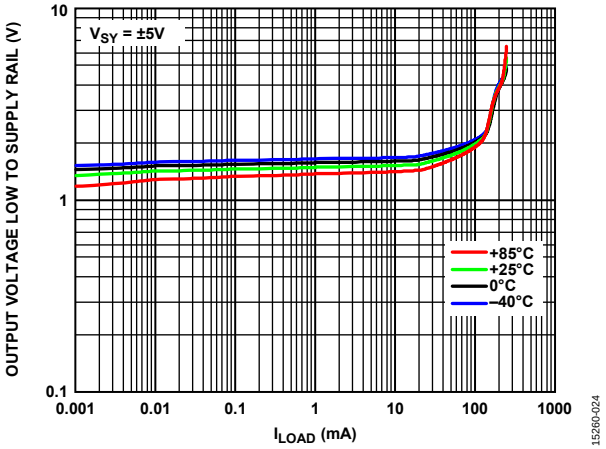


Figure 24. Output Voltage Low (V_{OL}) to Supply Rail vs. Load Current (I_{LOAD}) V_{SY} = ±5 V

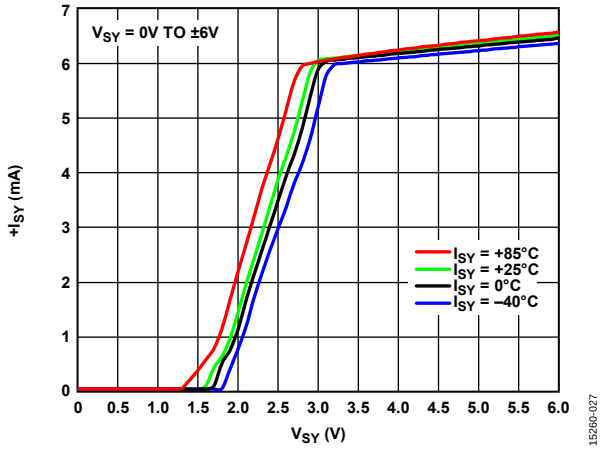


Figure 27. Positive Supply Current (+I_{SY}) vs. Supply Voltage (V_{SY})

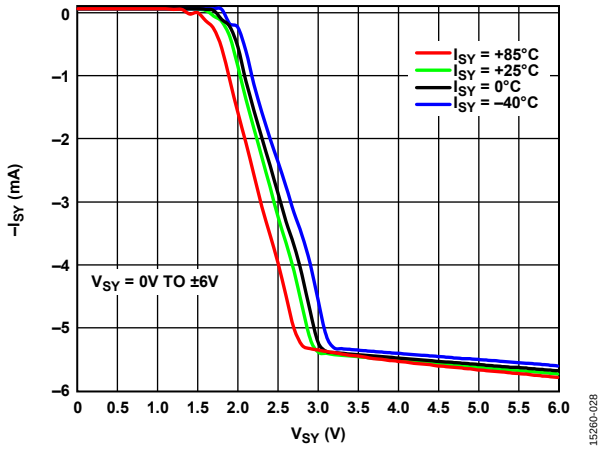


Figure 28. Supply Current ($-I_{SY}$) vs. Supply Voltage (V_{SY})

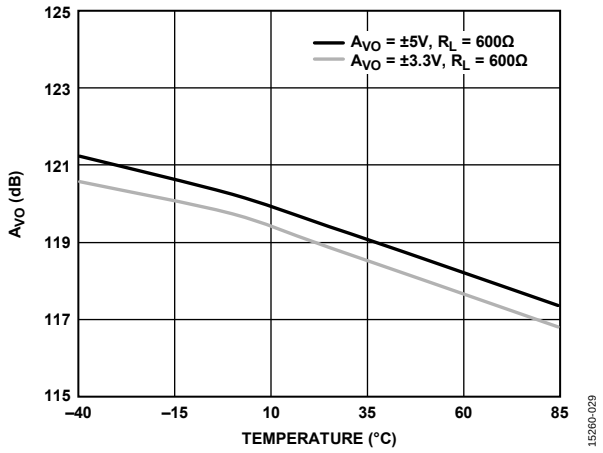


Figure 29. Open-Loop Gain (A_{VO}) vs. Temperature

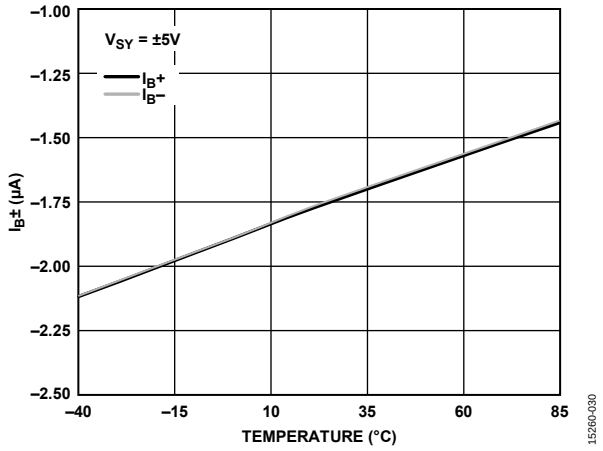


Figure 30. Input Bias Current (I_B±) vs. Temperature, V_{SY} = ±5 V

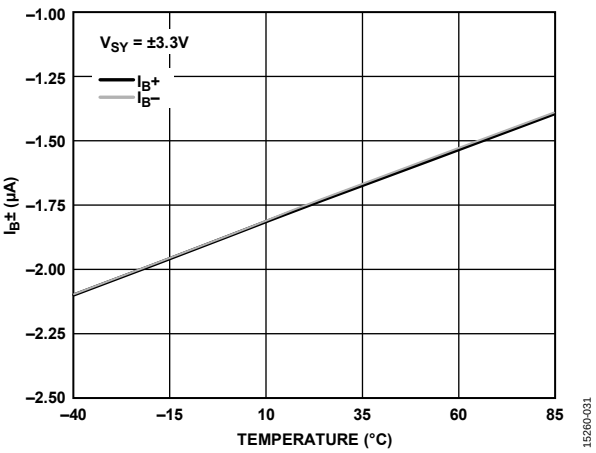


Figure 31. Input Bias Current (I_B±) vs. Temperature, V_{SY} = ±3.3 V

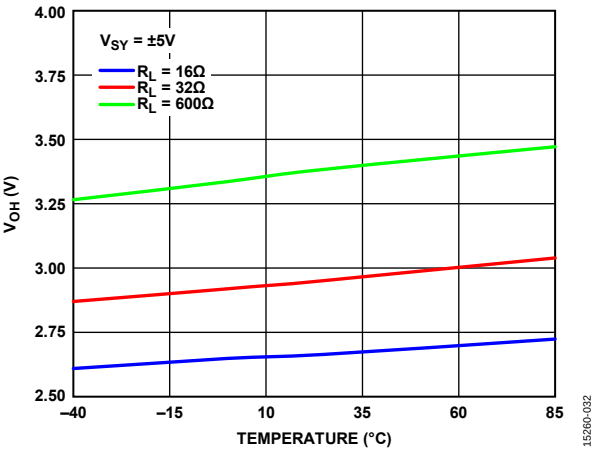


Figure 32. Output Voltage High (V_{OH}) vs. Temperature, V_{SY} = ±5 V

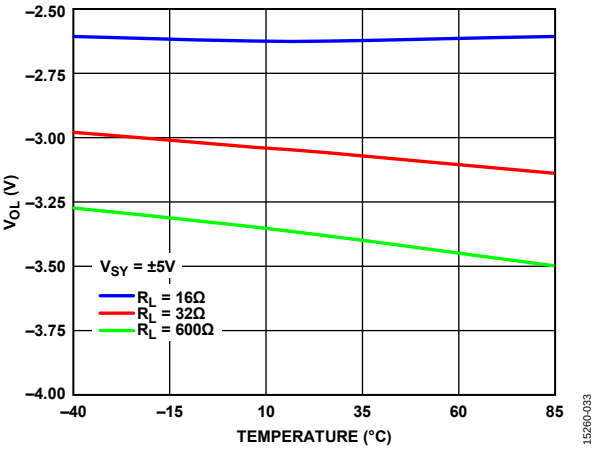


Figure 33. Output Voltage Low (V_{OL}) vs. Temperature, V_{SY} = ±5 V

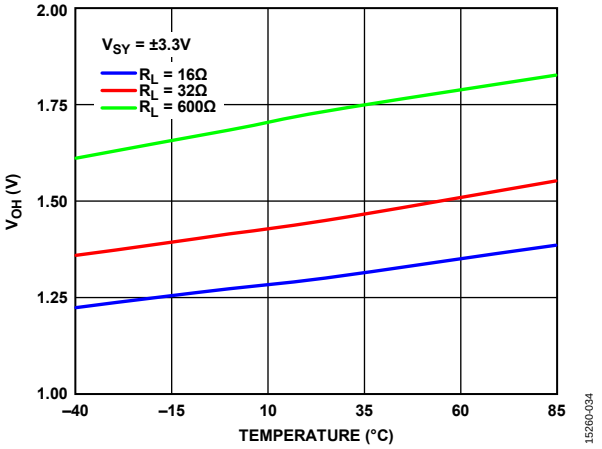


Figure 34. Output Voltage High (V_{OH}) vs. Temperature, V_{SY} = ±3.3 V

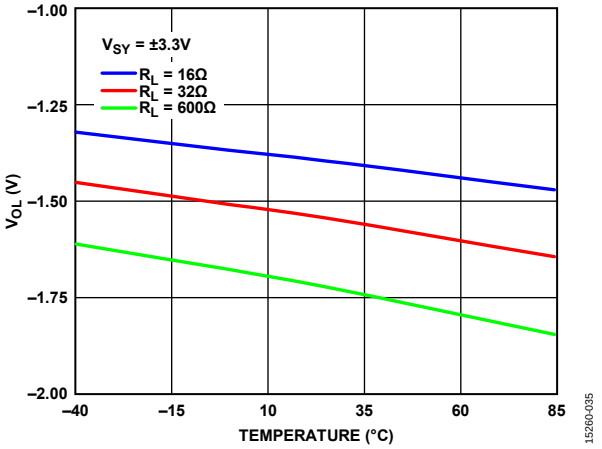


Figure 35. Output Voltage Low (V_{OL}) vs. Temperature, V_{SY} = ±3.3 V

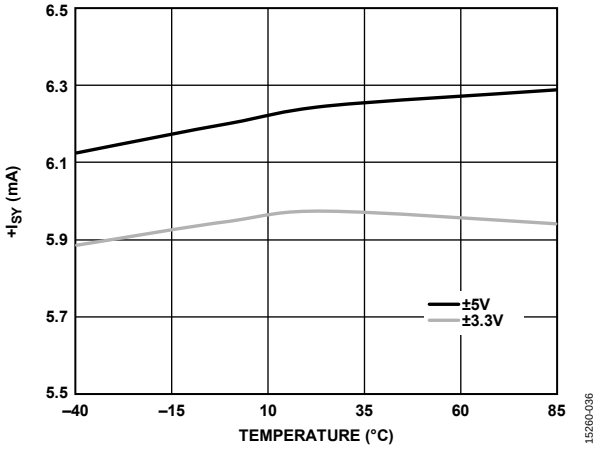


Figure 36. Supply Current ($+I_{SY}$) vs. Temperature

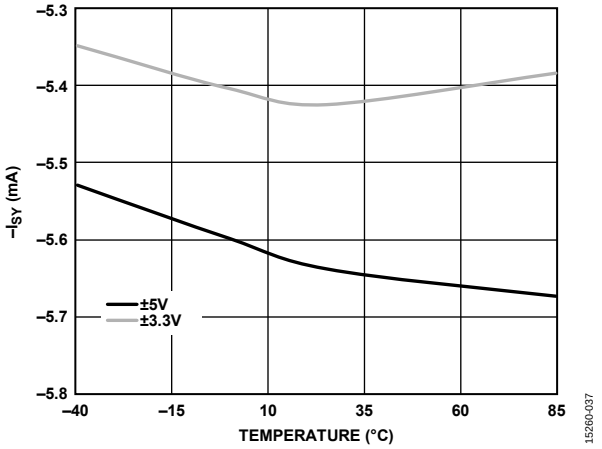


Figure 37. Supply Current ($-I_{SY}$) vs. Temperature

TEST CIRCUIT

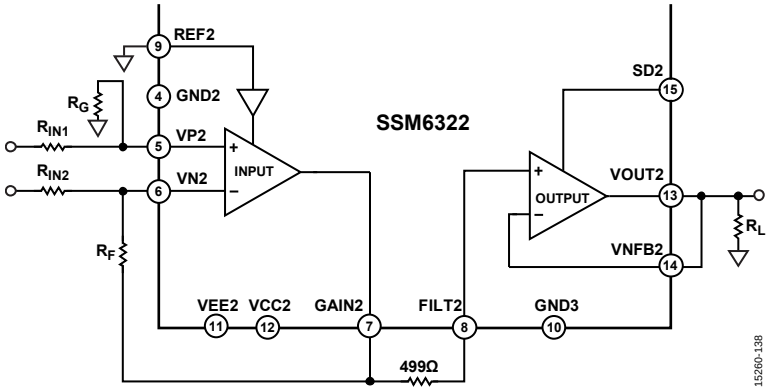


Figure 38. Test Circuit

THEORY OF OPERATION

The SSM6322 is designed using Analog Devices, Inc., proprietary extra fast complementary bipolar (XFCB) process. The device features exceptionally low 1/f noise, low power, and load drive capability. The device combines a classic difference amplifier configuration with a common-mode loop that maintains a fixed common-mode input level, regardless of the differential or common-mode currents going into the device. This combination results in the DAC operating in optimal conditions to reach the THD specifications. This configuration of a common-mode loop and a difference amplifier also has much lower noise and power consumption than other solutions by eliminating two additional amplifiers from the signal path.

The output driver has many features including heavy load drive, multiplexing, and pop click suppression. In both shutdown conditions, the output is high impedance in the audio band when the applied external signal is between the supply rails. An additional shutdown pin is included to power up the input difference amplifier so that it can settle before any unwanted signals are applied to the driver. The output driver is capable of delivering −120 dB THD with a 100 mA peak output current and a 2 V rms signal.

REF1 and REF2 Pin Voltage

REF1 and REF2 set the input common-mode signal. Internally, there is a 15 µA current source; by externally adding a resistor, 15 µA of current flows through the resistor to generate a common-mode voltage. For example, a 51 kΩ resistor and 15 µA current results in a common-mode voltage of 0.765 V.

Shutdown Control

The SSM6322 features two shutdown pins to control different sections of the device. When SD and SD2 are Logic 1, the entire device is enabled. When SD is Logic 0 and SD2 is Logic 1, the input stage is enabled, and the output buffer is disabled. When SD2 is Logic 0, the entire device is disabled with a quiescent current of only 15 µA (see Table 6).

Table 6. Disabled Mode and Enabled Mode

Logic Level of the Shutdown Pins	Device Status
SD and SD2 = 1	Entire device is enabled.
SD = 0 and SD2 = 1	Input stage is enabled, and the output buffer is disabled.
SD2 = 0	Entire device is disabled with a quiescent current of 15 µA.

APPLICATIONS INFORMATION

HEADPHONE DRIVERS IN MOBILE PHONES

In a headphone driver application, some high performance audio DACs can be configured as a voltage output or a current output. Typically, the current output configuration results in the best THD + N performance.

For a current output configuration, implement an current to voltage (I to V) circuit to convert the differential current signal from the R channel and the L channel to the differential voltage signal, followed by a difference amplifier circuit (see Figure 41).

For a voltage output configuration, the conditioning circuit is a difference amplifier circuit, which converts the differential signal from the R channel or L channel to a single-ended signal (see Figure 39).

Current output audio DACs are typically used to achieve the best THD + N performance (see Figure 41). Six amplifiers and many passive components are required to perform current mode signal conditioning, which consumes more PCB area and more power. Area consumption and power consumption are important considerations in mobile phone applications.

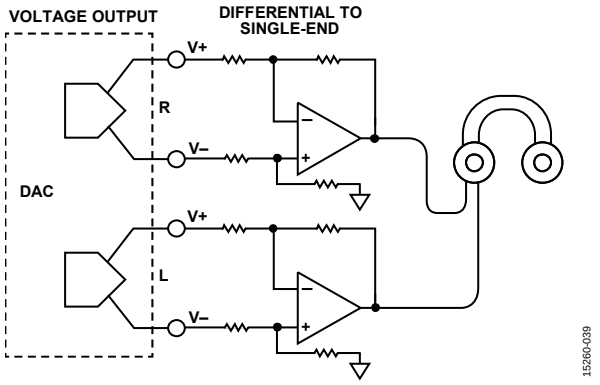


Figure 39. Voltage Output DAC Configuration

The SSM6322 is an integrated solution for mobile phone applications requiring low distortion and noise performance while directly driving a low impedance load. The device also saves more PCB area and power than the current discrete solution.

The SSM6322 contains an additional buffer to support high current drive capabilities. The buffer is also capable of being configured in true high-Z mode in the audio band, which is desirable in some portable applications for the multiplexing of other signals on the same output port.

COMMON-MODE CONTROL CIRCUIT

The differential output stage of the DAC can be modeled as two voltage sources, which both have the same amplitude and a 180° phase difference. R_S1 and R_S2 are the source resistors of the voltage source (see Figure 40).

In a typical current output DAC signal chain (see Figure 41), four amplifiers are configured as an I to V circuit. The non-inverting inputs are connected to a dc voltage that is the output common-mode level of the DAC, making the voltage at the I+/I– terminals a dc signal. This signal makes the voltage drop at two internal source resistors of the DAC (R_S1 and R_S2) the same, which makes the DAC achieve the best distortion performance.

In the SSM6322, the input difference amplifier performs the I to V conversion.

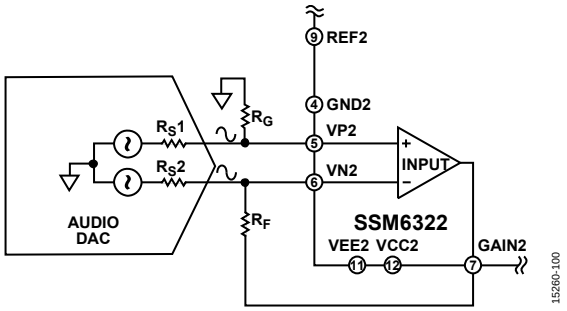


Figure 40. Common-Mode Circuit Without Common-Mode Control

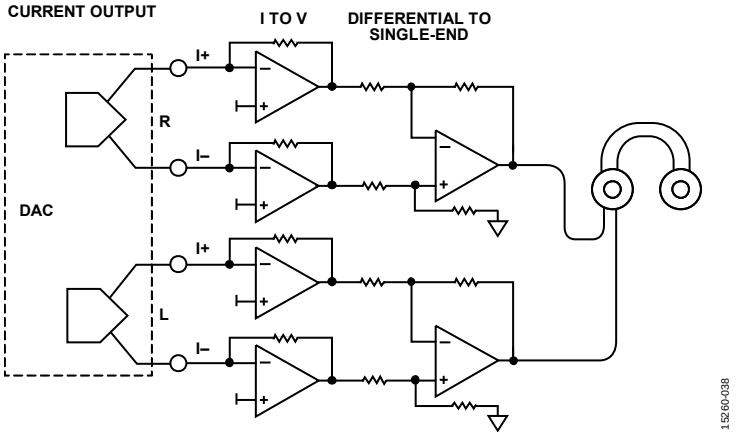


Figure 41. Current Output DAC Configuration

Assuming there is no common-mode control (see Figure 40), the signals at the input terminals (VP2/VN2) are ac signals that have the same amplitude and phase. In addition, the internal voltage source of the DAC is differential, which makes the voltage drop at R_S1 and R_S2 different values. This difference degrades the performance of the DAC. Simultaneously, from the amplifier, the ac common-mode signal at two input terminals (VP2 and VN2) generates additional error signal at the output by its limited ac common-mode rejection ratio (CMRR) performance.

After a common-mode control circuit (indicated by the dashed outline shown in Figure 42) is included, the signal at the input terminals (VP2 and VN2) is a dc signal set by the voltage at the REF2 pin (typically this voltage is the same as the dc common-mode voltage of the DAC). The voltage drop at R_S1 and R_S2 in the DAC is the same. Additionally, the high dc CMRR performance of the amplifier renders the CMRR error negligible. Both the DAC and the amplifier have the best performance in this configuration. The SSM6322 implements the circuit shown in Figure 42.

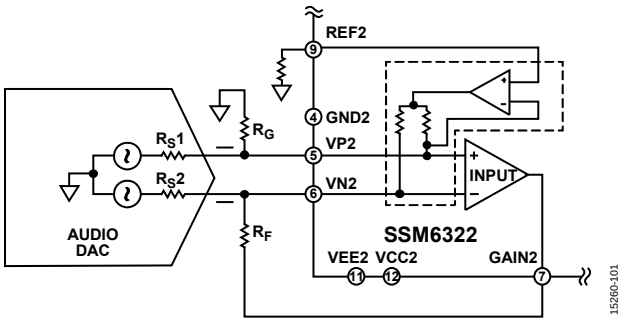


Figure 42. Common-Mode Circuit with Common-Mode Control

CAPACITIVE LOAD DRIVE

Figure 43 shows the schematic of the output stage for driving capacitive loads. Figure 44 and Figure 45 show the frequency response for a gain of 1 at the ±5 V and ±3.3 V power supply voltages, respectively. The peaking is high with a small capacitive load. With a 2.2 nF capacitive load (C_L), the frequency response is flat and without peaking.

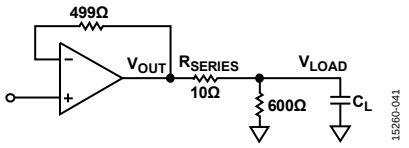


Figure 43. Schematic for Driving Capacitive Loads

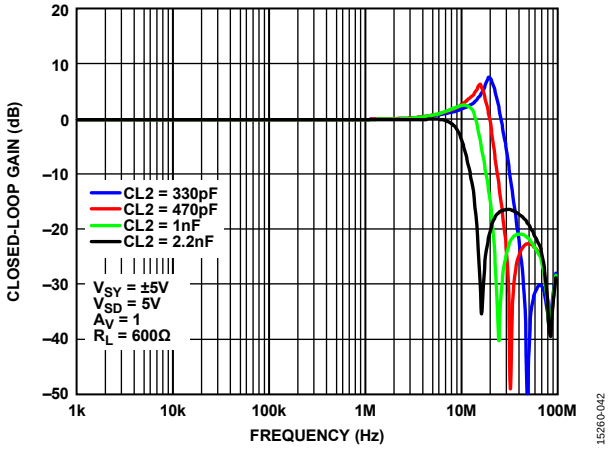


Figure 44. Frequency Response for Driving Capacitive Loads, V_{SY} = ±5 V

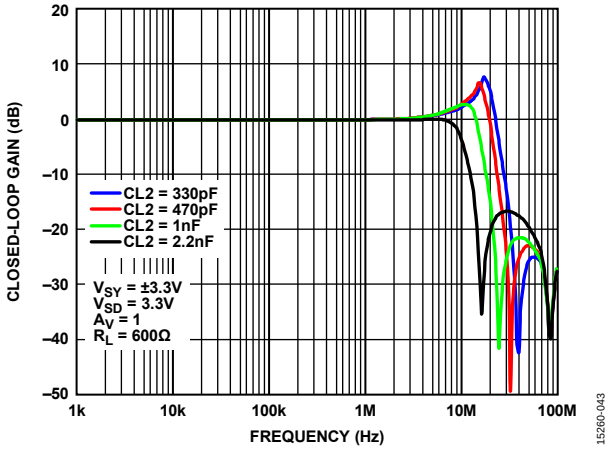


Figure 45. Frequency Response for Driving Capacitive Loads, V_{SY} = ±3.3 V

SSM6322 IN A HEADPHONE DRIVER APPLICATION

SSM6322 Circuit with Current Output DAC

For an audio DAC with a differential current output, two gain resistors convert the current to voltage (see Figure 46). The resistor value is determined by the DAC output full-scale current and the input stage output range (the output range is ±3 V at a ±5 V supply). Assuming that the DAC single-ended output current is ±1.5 mA, and that the differential current is ±3 mA, the output of the input stage is ±3 V when using two 1 kΩ gain resistors. The feedback capacitors, in parallel with the gain resistors, form a single-pole, low-pass filter. The SSM6322 can handle up to a 1 kΩ and 2.2 nF resistor capacitor combination.

Typically, audio DACs generate a dc offset current, which is converted to an input common-mode voltage at the input of the SSM6322. The REF1 and REF2 pins of the SSM6322 set the input common-mode voltage of each channel. The voltage at the REF1 and REF2 pins is achieved by an internal 15 µA current source and an external resistor; a 51 kΩ resistor is suggested to achieve a 0.765 V voltage. A 1 µF capacitor can be used in parallel with the resistor to remove noise.

A 499 Ω resistor and 1 nF capacitor can be added between the input stage and output stage for a second single-pole, low-pass filter, as shown in Figure 46.

For better gain matching and better distortion performance, all 1 kΩ and 499 Ω resistors must to be of 0.1% tolerance and a 25 ppm/°C temperature coefficient. The 1 nF capacitors must be NP0 capacitors. There are no specific requirements for the 51 kΩ resistor and the 1 µF capacitor at REF1 and REF2.

SSM6322 Circuit with Voltage Output DAC

For audio DACs that output a differential voltage, four gain resistors convert the differential voltage to single-ended voltage (see Figure 47). The feedback capacitors must be in parallel with the gain resistors to form the single-pole, low-pass filter. As shown in Figure 47, four 1 kΩ resistors and two 1 nF capacitors are used to achieve a gain of 1 and a first-order, 159 kHz cutoff frequency low-pass filter.

For REF1 and REF2, refer to the DAC data sheet for the common-mode voltage; then, calculate the resistor value at REF1 and REF2. As shown in Figure 47, a 51 kΩ resistor is suggested to obtain a 0.765 V voltage.

A 499 Ω resistor and 1 nF capacitor can be added between the input stage and output stage for a second single-pole, low-pass filter, as shown in Figure 47.

For better gain matching and better distortion performance, all 1 kΩ and 499 kΩ resistors must be of a 0.1% tolerance and 25ppm/°C temperature coefficent; the 1 nF capacitor must be NP0 capacitor.

There are no specific requirement for the 51 kΩ resistor and 1 µF capacitor at REF1 and REF2.

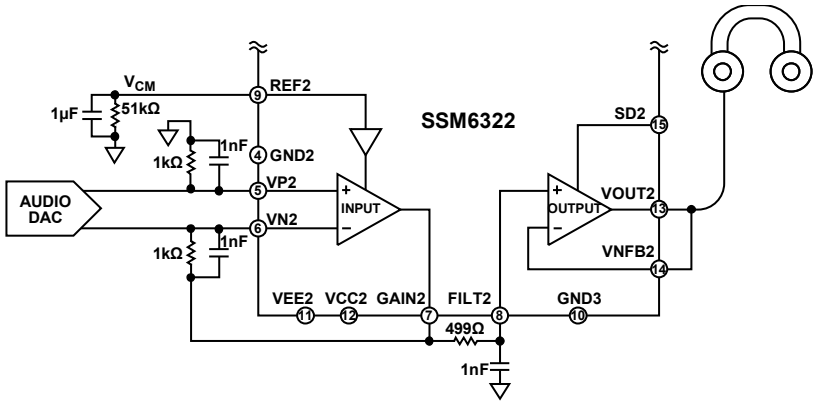


Figure 46. SSM6322 Circuit with Current Output DAC

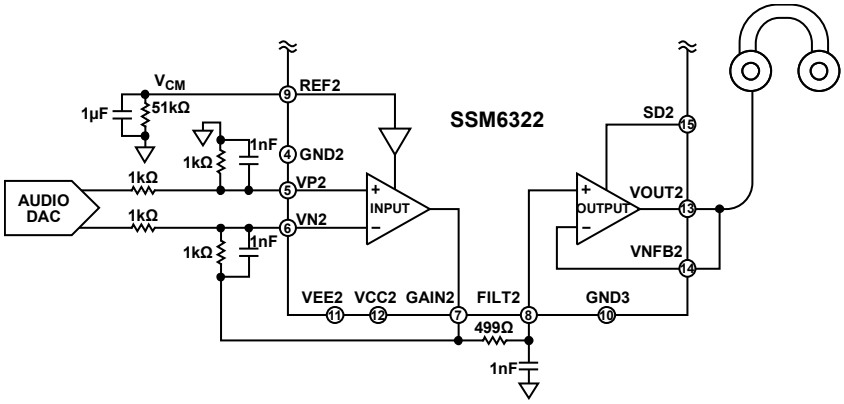


Figure 47. SSM6322 Circuit with Voltage Output DAC

DESIGN GUIDELINES

The performance of the SSM6322 is such that any minor external interference can destroy the circuit. When using this device, consider the following:

- The sensing ground of the input stage is sensitive to external interference. In the PCB layout, it is recommended to refer the sensing ground to the output interface ground (in high fidelity headphone driver applications, the output interface is the jack). As shown in Figure 48, the dashed outline enclosed ground is the input stage sensing ground, which must be routed directly to the ground of the jack. Note that Figure 48 only shows one channel; for the other channel, route the sensing ground to the jack ground separately.
- The SSM6322 circuit is different with a typical current output DAC signal chain (see Figure 41); there is only one op amp that performs the differential I to V conversion. The power across the noninverting grounded resistor is fixed, but the power across the feedback resistor varies with the output signal. This variability creates a mismatch between the two resistors, as well as distortion if the heat cannot be well dissipated. Low drift (25 ppm/°C) metal film or thin film resistors are suggested to avoid this situation (see Figure 46).
- If there is a resistor between the final output and the headphone, the resistor must be low drift (25 ppm/°C) and metal film or thin film to avoid distortion when driving heavy loads.
- Use a low dropout regulator (LDO) as the power supply. Place the decoupling capacitors (0.1 µF and 4.7 µF) near the amplifier power pins. If there is switching power on the board, keep the switching power circuit and return path far away from the SSM6322 circuit.
- For better heat dissipation, solder the exposed pad of the LFCSP package to the board pad and, using vias, connect the exposed pad to a large, solid copper plane at the opposite side of the board. The copper plane can be connected to the negative supply plane or ground plane.
- Shielding is important in mobile phone applications. To reach <−100 dB THD + N specifications, even small interferences can degrade THD + N performance, particularly when listening to music and browsing the internet simultaneously. Metal shielding helps prevent performance degradation.
- The maximum input filter capacitor values are 2.2 nF.

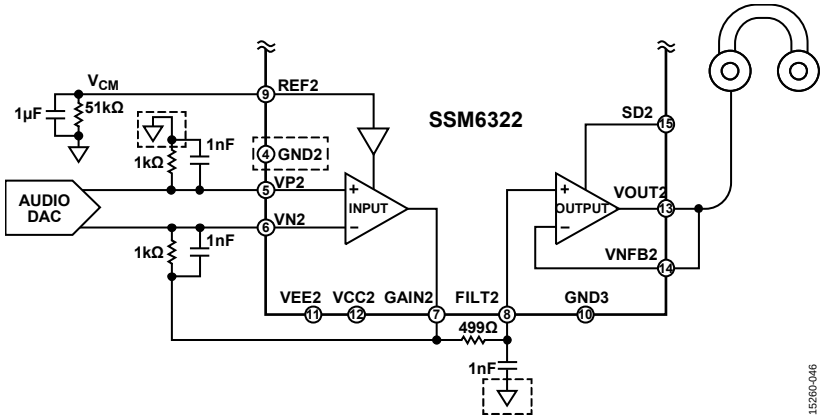
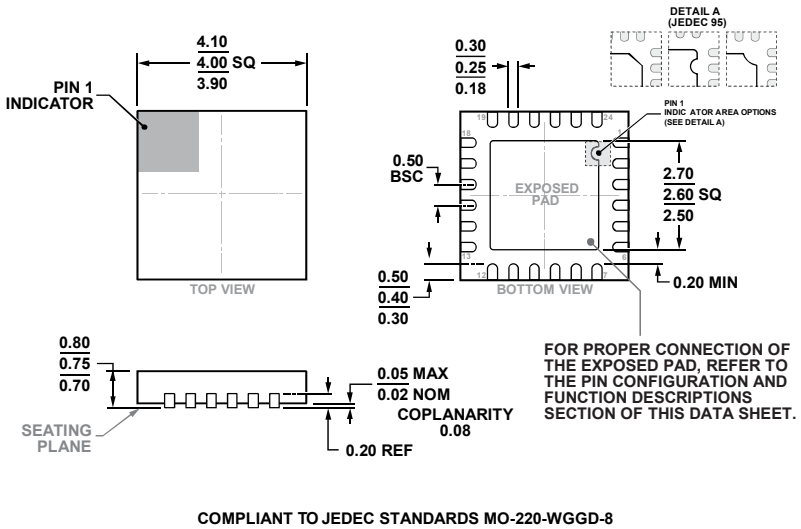


Figure 48. Sensing Ground of Input Stage

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8

Figure 49. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Package	Package Description	Package Option	Branding
SSM6322ACPZ-R2	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15	6322A
SSM6322ACPZ-R7	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15	6322A
SSM6322ACPZ-RL	−40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-15	6322A
SSM6322CP-EBZ		Evaluation Board		

[1] Z = RoHS Compliant Part.