- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 50 Ω or Greater**
- **Bus-Hold On Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) and Thin Shrink Small-Outline (DGG) Packages**

DGG OR DL PACKAGE
(TOP VIEW)

1$\overline{OE}$	1	48	2$\overline{OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V_{CC}	7	42	V_{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V_{CC}	18	31	V_{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
4$\overline{OE}$	24	25	3$\overline{OE}$

description

This 16-bit buffer/driver is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74ALVC16244 is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. It provides true outputs and symmetrical $\overline{OE}$ (active-low output-enable) inputs.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVC16244 is available in TI's shrink small-outline (DL) and thin shrink small-outline (DGG) packages, which provide twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The SN74ALVC16244 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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![Texas Instruments logo] **TEXAS INSTRUMENTS**

SN74ALVC16244
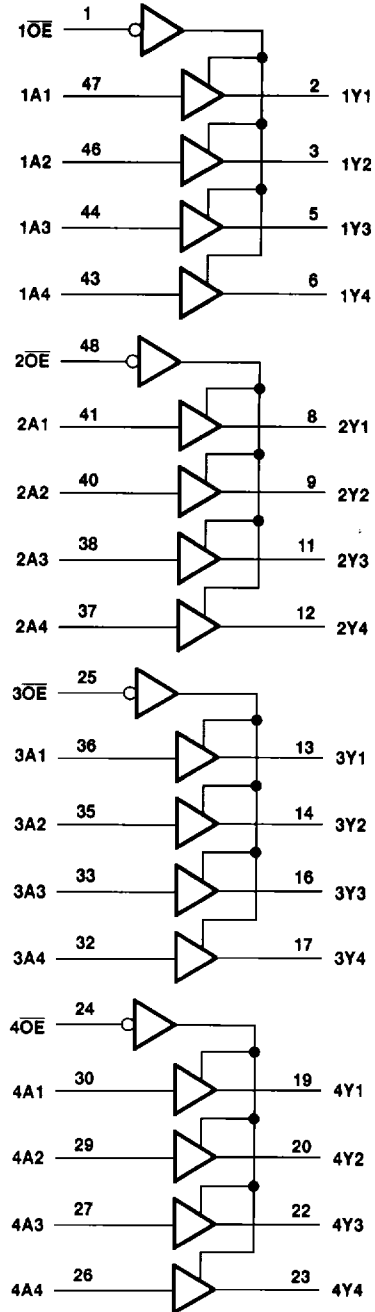## 16-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

SCAS250 – JANUARY 1993 – REVISED JANUARY 1994

logic symbol†
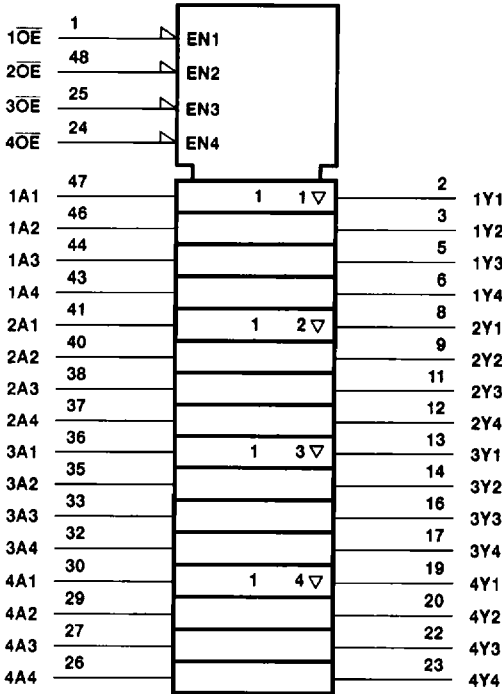
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

TEXAS INSTRUMENTS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 4.6 V
Output voltage range, V_O (see Notes 1 and 2) .... −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) .... ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±50 mA
Continuous current through V_{CC} or GND .... ±100 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DGG package .... 0.85 W
DL package .... 1.2 W
Storage temperature range .... −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

recommended operating conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			2.7	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V to 3.6 V		2		V
V_{IL}	Low-level input voltage	V_{CC} = 2.7 V to 3.6 V			0.8	V
V_I	Input voltage			0	V_{CC}	V
V_O	Output voltage			0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2.7 V			−12	mA
		V_{CC} = 3 V			−24	
I_{OL}	Low-level output current	V_{CC} = 2.7 V			12	mA
		V_{CC} = 3 V			24	
$\Delta t / \Delta v$	Input transition rise or fall rate			0	10	ns/V
T_A	Operating free-air temperature			−40	85	°C

PRODUCT PREVIEW

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}†	MIN	TYP	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$		MIN to MAX	$V_{CC}-0.2$			V
		$I_{OH} = -12\ mA$		2.7 V	2.2			
				3 V	2.4			
		$I_{OH} = -24\ mA$		3 V	2			
V_{OL}		$I_{OL} = 100\ \mu A$		MIN to MAX			0.2	V
		$I_{OL} = 12\ mA$		2.7 V			0.4	
		$I_{OL} = 24\ mA$		3 V			0.55	
I_I	Inputs	$V_I = V_{CC}$ or GND		3.6 V			±5	μA
$I_{I(hold)}$	Data pins	$V_I = 0.8\ V$		3 V	75			μA
		$V_I = 2\ V$			−75			
I_{OZ}		$V_O = V_{CC}$ or GND		3.6 V			±10	μA
I_{CC}		$V_I = V_{CC}$ or GND,	$I_O = 0$	3.6 V			40	μA
ΔI_{CC}		$V_{CC} = 3\ V$ to 3.6 V, Other inputs at V_{CC} or GND	One input at $V_{CC} - 0.6\ V$,				750	μA
C_i		$V_I = V_{CC}$ or GND		3.3 V		3.5		pF
C_o		$V_O = V_{CC}$ or GND		3.3 V				pF

† For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\ V \pm 0.3\ V$			$V_{CC} = 2.7\ V$		UNIT
			MIN	TYP	MAX	MIN	MAX	
t_{pd}	A	Y	1	2.2	3.6		4	ns
t_{en}	$\overline{OE}$	Y	1	2.7	5		6	ns
t_{dis}	$\overline{OE}$	Y	1	2.9	5		5.2	ns

NOTE 4: Load circuit and voltage waveforms are shown in Section 1.

operating characteristics, V_{CC} = 3.3 V, T_A = 25° C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per bit	Outputs enabled	$C_L = 50\ pF,\ f = 10\ MHz$	16	pF
	Outputs disabled		5	