

# Quad D flip-flop

54F175

## FEATURES

- Four edge-triggered D flip-flops
- Buffered common Clock
- Buffered, asynchronous Master Reset
- True and complementary output

## DESCRIPTION

The 54F175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and  $\bar{Q}$  outputs. The common buffered Clock (CP) and Master Reset ( $\bar{MR}$ ) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the  $\bar{MR}$  input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	54F175/BEA	GDIP1-T16
16-Pin Ceramic Flat Pack	54F175/BFA	GDFF2-F16
20-Pin Ceramic LLCC	54F175/B2A	CQCC2-N20

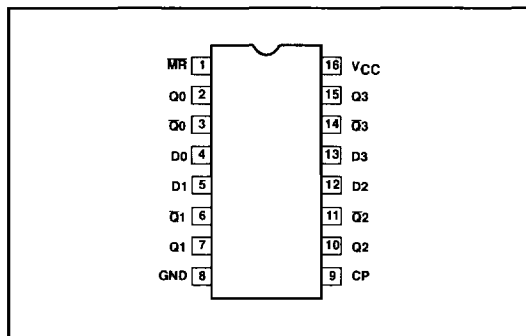
\* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

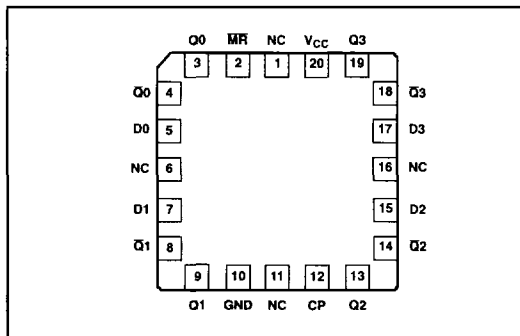
PINS	DESCRIPTION	54F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 - D3	Data inputs	1.0/1.0	20 $\mu$ A/0.6mA
CP	Clock pulse input (active rising edge)	1.0/1.0	20 $\mu$ A/0.6mA
$\bar{MR}$	Master Reset input (active Low)	1.0/1.0	20 $\mu$ A/0.6mA
Q0 - Q3	True outputs	50/33	1.0mA/20mA
$\bar{Q}0 - \bar{Q}3$	Complementary outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20 $\mu$ A in the High state and 0.6mA in the Low state.

## PIN CONFIGURATION



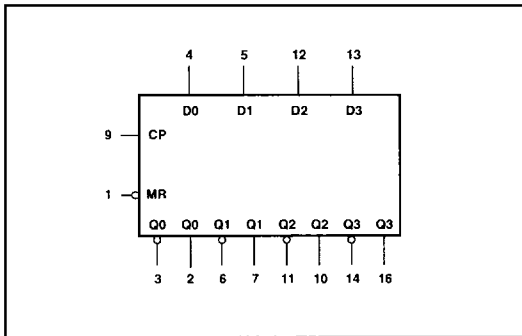
## LLCC LEAD CONFIGURATION



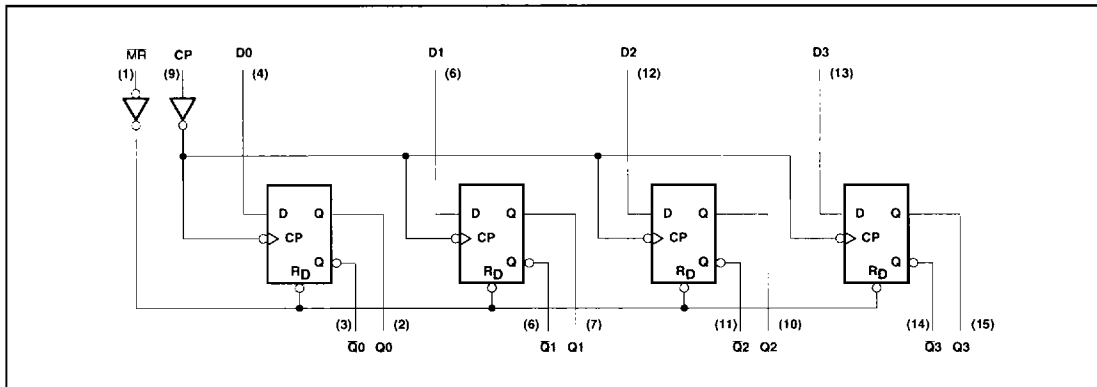
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## LOGIC SYMBOL



## LOGIC DIAGRAM



## FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	MR	CP	Dn	Qn	Qn
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = High voltage level steady state.  
 h = High voltage level one setup time prior to the Low-to-High Clock transition.  
 L = Low voltage level steady state.  
 l = Low voltage level one setup time prior to the Low-to-High Clock transition.  
 X = Don't Care.  
 ↑ = Low-to-High Clock transition.

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage range	-0.5 to +7.0	V
$V_I$	Input voltage range	-0.5 to +7.0	V
$I_I$	Input current range	-30 to +5.0	mA
$V_O$	Voltage applied to output in High output state range	-0.5 to $V_{CC}$	V
$I_O$	Current applied to output in Low output state	40	mA
$T_{STG}$	Storage temperature range	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
$V_{CC}$	Supply voltage	4.5	5.0	5.5	V
$V_{IH}$	High-level input voltage	2.0			V
$V_{IL}$	Low-level input voltage			0.8	V
$I_{IK}$	Input clamp current			-18	mA
$I_{OH}$	High-level output current			-1	mA
$I_{OL}$	Low-level output current			20	mA
$T_{amb}$	Operating free-air temperature range	-55		+125	°C

**DC ELECTRICAL CHARACTERISTICS**

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,4</sup>	LIMITS			UNIT
			MIN	TYP <sup>2</sup>	MAX	
$V_{OH}$	High-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OH} = \text{MAX}, V_{IH} = \text{MIN}$	2.5			V
$V_{OL}$	Low-level output voltage	$V_{CC} = \text{MIN}, V_{IL} = \text{MAX}, I_{OL} = \text{MAX}, V_{IH} = \text{MIN}$		0.35	0.50	V
$V_{IK}$	Input clamp voltage	$V_{CC} = \text{MIN}, I_I = I_{IK}$		-0.73	-1.2	V
$I_{IH2}$	Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	μA
$I_{IH1}$	High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$		1	20	μA
$I_{IL}$	Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$		-0.4	-0.6	mA
$I_{OS}$	Short-circuit output current <sup>3</sup>	$V_{CC} = \text{MAX}$	-60		-150	mA
$I_{CC}$	Supply current (total)	$V_{CC} = \text{MAX}, D_n = \text{MR} \geq 4.0\text{V}, CP = \uparrow$		25	34	mA

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f <sub>MAX</sub>	Maximum Clock frequency	Waveform 1	100	140		80 <sup>5</sup>		MHz
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay CP to Qn or Qn	Waveform 1	4.0 4.0	5.0 6.5	6.5 8.5	3.5 4.0	8.5 10.5	ns ns
t <sub>PHL</sub>	Propagation delay MR to Qn	Waveform 3	4.5	9.0	11.5	4.5	15	ns
t <sub>PLH</sub>	Propagation delay MR to Qn	Waveform 3	4.0	6.5	8.0	4.0	10	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			T <sub>amb</sub> = -55°C to +125°C V <sub>CC</sub> = +5.0V ± 10% C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Setup time, High or Low Dn to CP	Waveform 2	3.0 3.0			3.0 3.0		ns ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, High or Low Dn to CP	Waveform 2	1.0 1.0			1.0 1.0		ns ns
t <sub>w</sub> (H) <sup>6</sup> t <sub>w</sub> (L) <sup>6</sup>	CP pulse width, High or Low	Waveform 1	4.0 5.0			4.0 5.0		ns ns
t <sub>w</sub> (L) <sup>6</sup>	MR pulse width Low	Waveform 3	5.0			5.0		ns
t <sub>rec</sub>	Recovery time MR to CP	Waveform 3	5.0			5.0		ns

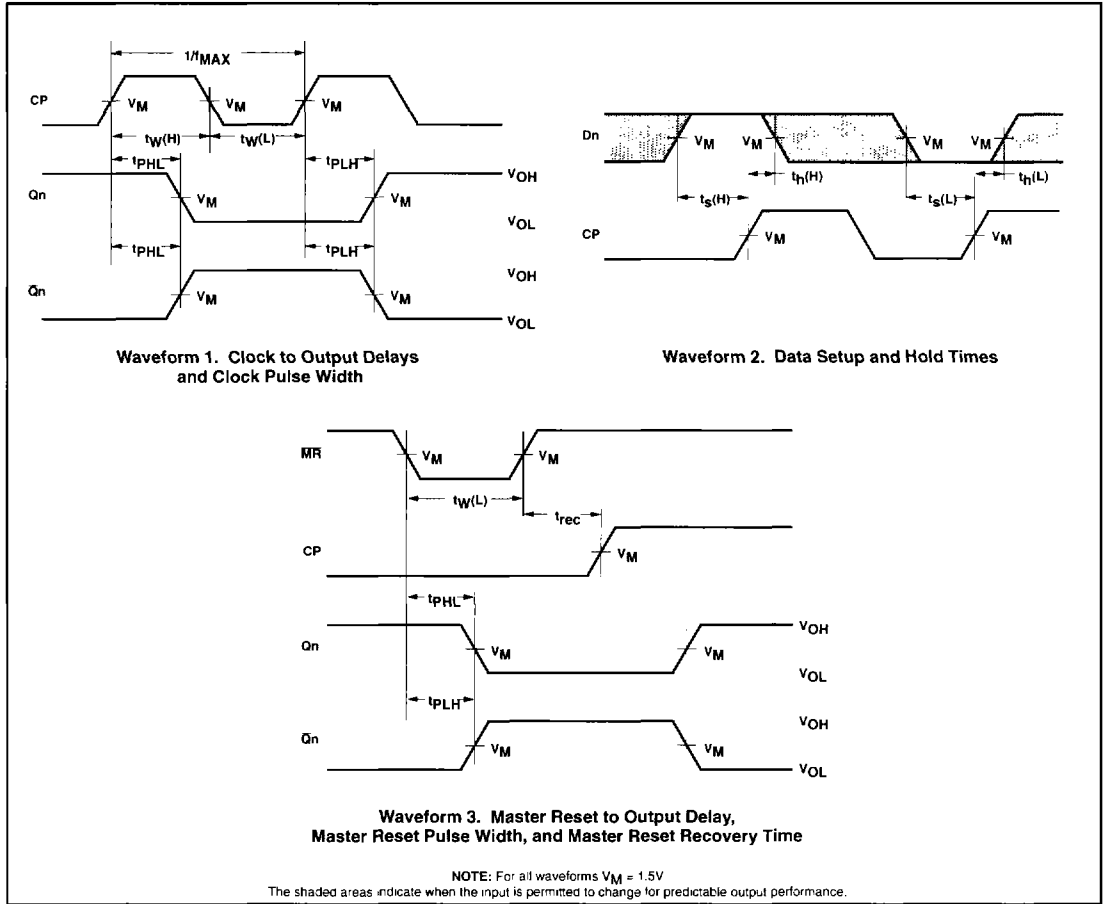
## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.
- When testing devices to the functional table specified refer to the "Recommended Operating Conditions Section" of Application Note 202, "Testing and Specifying FAST Logic".
- These parameters are guaranteed, but not tested.
- T<sub>w</sub> tested to 7.0ns but guaranteed as specified. This is due to tester limitations.

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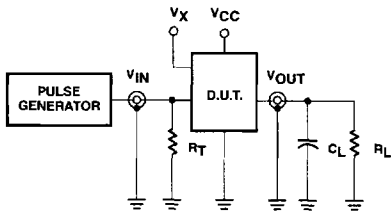
## AC WAVEFORMS



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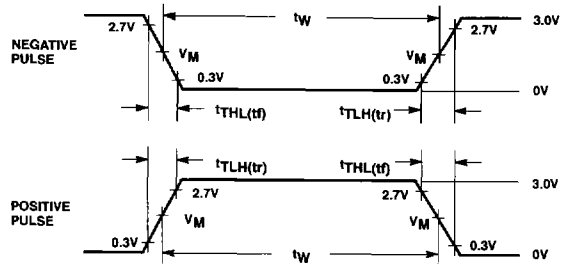
## TEST CIRCUIT AND WAVEFORM



Test Circuit for Totem-Pole Outputs

**DEFINITIONS:**

- $R_L$  = Load Resistor; see AC Characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.
- $V_X$  = Unclocked pins must be held at:  $\leq 0.8V$ ;  $\geq 2.7V$  or open per Function Table.



$V_M = 1.5V$

Input Pulse Definition

INPUT PULSE CHARACTERISTICS				
Family	Rep. Rate	Pulse Width	$t_{TLH}$	$t_{THL}$
54F	1MHz	500ns	$\leq 2.5ns$	$\leq 2.5ns$