

# HIGH LEVEL LOGIC DIODE-TRANSISTOR MICROLOGIC®

## INTEGRATED CIRCUITS COMPOSITE DATA SHEET

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

0°C TO 75°C TEMPERATURE RANGE

**GENERAL DESCRIPTION** — The Fairchild High Level Logic Diode-Transistor Micrologic® Integrated Circuit family (HLLDT $\mu$ L) consists of three high voltage, high threshold hex inverters which offer extremely good D.C. and A.C. Noise Immunity. These circuits are useful in applications involving a high noise environment or high voltage supply which prohibits the use of CCSL.

Interfacing from CCSL to HLLDT $\mu$ L is accomplished with the 9112, shifting from HLLDT $\mu$ L to CCSL is accomplished with the 9109. The 9112 can also be used to drive the  $\mu$ M3700 MOS Multiplexer.

The circuits are fabricated within a silicon monolithic substrate using standard Fairchild Planar\* and Epitaxial processes.

HLLDT $\mu$ L elements are available in the hermetically sealed ceramic Dual In-Line Package (DIP), designed for automated and low cost insertion techniques.

### FEATURES

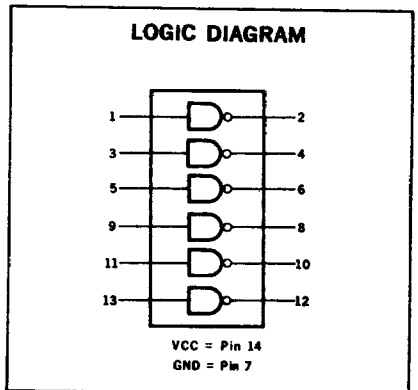
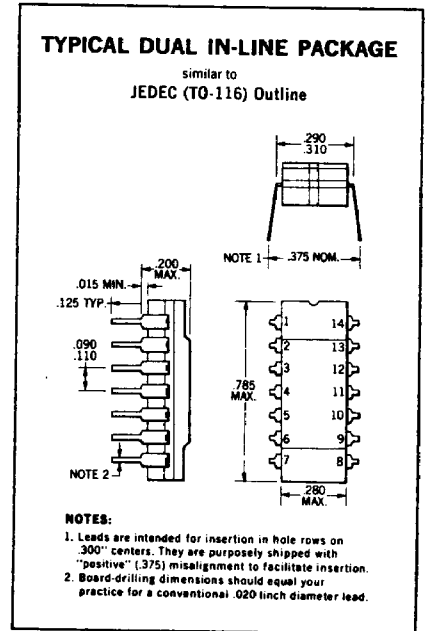
- High Voltage Operation . . .  $V_{CC}$  Range 12 to 20 V.
- Utilizes inexpensive external input diodes to facilitate a high density building block approach and very high Logic Fan-In where desired.
- High D.C. Noise Immunity . . . 6.5 V minimum
- High A.C. Noise Immunity . . . 10 V at 150 ns
- Interfaces with CCSL

### ABSOLUTE MAXIMUM RATINGS (above which the reliability of the device may be impaired)

Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +75°C
$V_{CC}$ Pin Potential to Gnd Pin	-0.5 V to +25 V
Output Current when output is low	40 mA
Input Current (9109, 9110)	10 mA
Output Voltage	25 V
Input Voltage (9112)	5.5 V

### ORDERING INFORMATION

To order HLLDT $\mu$ L elements specify U6AXXX59X, where XXXX is the four-digit number denoting the specific element desired.



\*Planar is a patented Fairchild process.

# FAIRCHILD HLLDT $\mu$ L INTEGRATED CIRCUITS

## ELECTRICAL CHARACTERISTICS

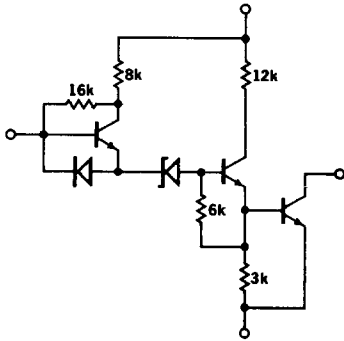
SYMBOL	CHARACTERISTIC	DEVICE	LIMITS						UNITS	CONDITIONS AND COMMENTS
			0°C		+25°C		+75°C			
			MIN.	MAX.	MIN.	TYP.	MAX.	MIN.		
$V_{OH}$	Output High Voltage	9110 9112	Note 2		Note 2		Note 2		Volts	$V_{CC} = 12\text{ V to }20\text{ V}$ $I_{OH} = -0.1\text{ mA}$ @ $V_{IL}$
$I_{CEX}$	Output Leakage Current	9109	75		1.0	75	75		$\mu\text{A}$	$V_{CC} = 20\text{ V}$ $V_{OH} = 20\text{ V}$ @ $V_{IL}$
$V_{OL1}$	Output Low Voltage	9109 9110 9112	0.5		0.25	0.5	0.5		Volts	$V_{CC} = 12\text{ V}$ $I_{OL} = 10\text{ mA}$ @ $V_{IH}$
$V_{OL2}$	Output Low Voltage	9109 9110 9112	1.0		0.5	1.0	1.0		Volts	$V_{CC} = 20\text{ V}$ $I_{OL} = 20\text{ mA}$ @ $V_{IH}$
$V_{IL}$	Input Low Voltage	9109	7.05		7.0		6.8		Volts	Input Low Threshold @ $V_{OH}$
		9110								
		9112	1.05		1.0		0.8			
$V_{IH}$	Input High Voltage	9109	8.6		8.5		8.4		Volts	Input High Threshold @ $V_{OL}$
		9110								
		9112	2.1		2.0		1.9			
$I_F$	Input Load Current	9109 9110 9112	-1.20		-0.80	-1.12	-1.12		mA	$V_{CC} = 20\text{ V}$ , $V_F = 0.5\text{ V}$
$I_{SC}$	Output Short Circuit Current	9110	-17		-9.0	-16.3	-15.6		mA	$V_{CC} = 20\text{ V}$ , $V_{IN} = 0\text{ V}$ $V_{OUT} = 0\text{ V}$
		9112	-2.4		-1.65	-2.3	-2.3			
$I_{CEX}$	Output Leakage Current	9110 9112	75		1.0	75	75		$\mu\text{A}$	$V_{CC} = 20\text{ V}$ , $V_{OUT} = 20\text{ V}$ $V_{IN} = 0\text{ V}$
$I_{PDH}$	Input High Supply Current	9109			19	28			mA	$V_{CC} = 20\text{ V}$ , Input Open
		9110								
		9112			22	34				
$I_R$	Input Leakage Current	9112			5.0		10		$\mu\text{A}$	$V_{CC} = 20\text{ V}$ , $V_R = 4.0\text{ V}$
$I_{max}$	Ground Current	9109							mA	$V_{CC} = V_{OUT} = 25\text{ V}$ , Inputs @ GND
		9110			15					
		9112								
$t_{pd+}$	Turn Off Delay	9109							ns	See Fig. 4
		9110			145	300				
		9112								
$t_{pd-}$	Turn On Delay	9109							ns	See Fig. 4
		9110			95	200				
		9112			30	125				
$V_{TN}$	"0" Level A.C. Noise Immunity	9110			7.0				Volts	See Fig. 5
$V_{TP}$	"1" Level A.C. Noise Immunity	9110			8.5				Volts	See Fig. 5

### NOTES:

- (1) Tests on 9109, 9110 are performed with FDH6 input diodes.
- (2) MIN =  $V_{CC} - 2.0\text{ V}$  for all temperature  
TYP =  $V_{CC} - 1.5\text{ V}$  for 25°C

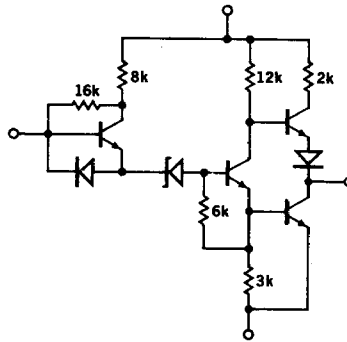
# FAIRCHILD HLLDT $\mu$ L INTEGRATED CIRCUITS

**Fig. 1a**



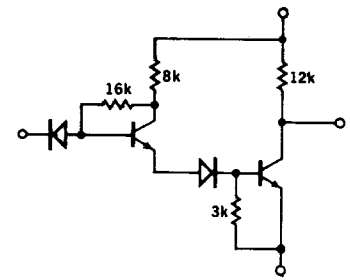
**1/6 HLLDTL 9109**  
HLL → CCSL

**Fig. 1b**



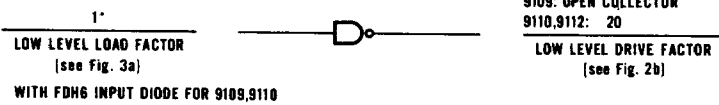
**1/6 HLLDTL 9110**  
HLL → HLL

**Fig. 1c**

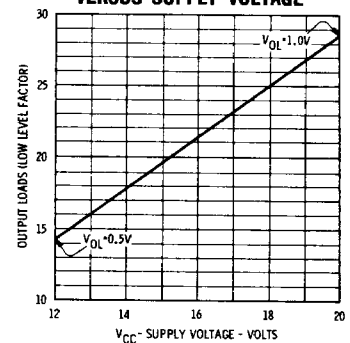


**1/6 HLLDTL 9112**  
CCSL → HLL

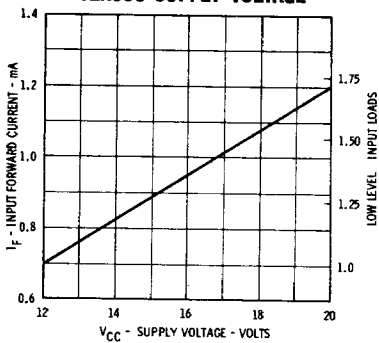
**Fig. 2a**



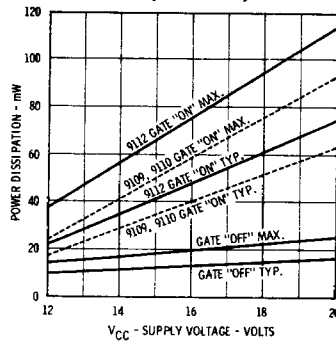
**Fig. 2b**  
**OUTPUT LOADS**  
**(LOW LEVEL DRIVE FACTOR)**  
**VERSUS SUPPLY VOLTAGE**



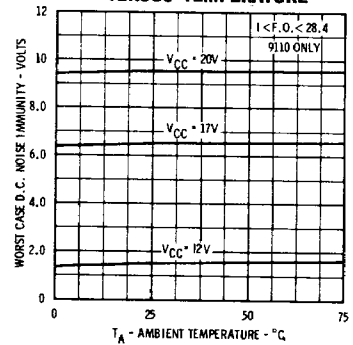
**Fig. 3a**  
**WORST CASE INPUT FORWARD**  
**CURRENT AND INPUT LOADS**  
**VERSUS SUPPLY VOLTAGE**



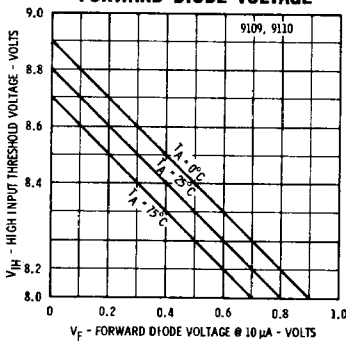
**Fig. 3b**  
**WORST CASE POWER DISSIPATION**  
**VERSUS SUPPLY VOLTAGE**  
**(PER GATE)**



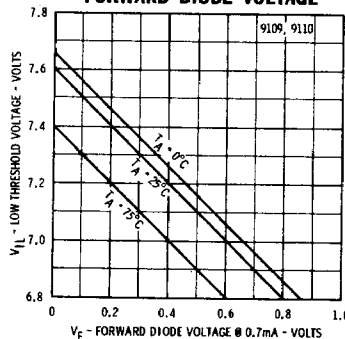
**Fig. 3c**  
**WORST CASE HIGH LEVEL**  
**D.C. NOISE IMMUNITY**  
**VERSUS TEMPERATURE**



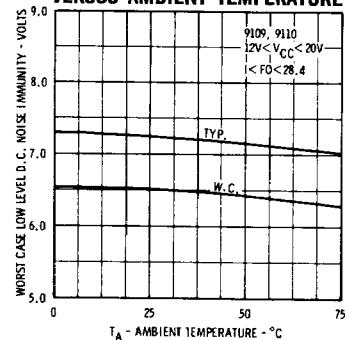
**Fig. 3d**  
**WORST CASE HIGH INPUT**  
**THRESHOLD VOLTAGE VERSUS**  
**FORWARD DIODE VOLTAGE**



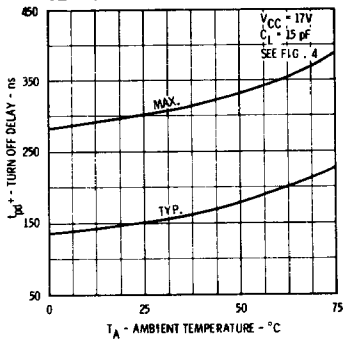
**Fig. 3e**  
**WORST CASE LOW THRESHOLD**  
**VOLTAGE VERSUS**  
**FORWARD DIODE VOLTAGE**



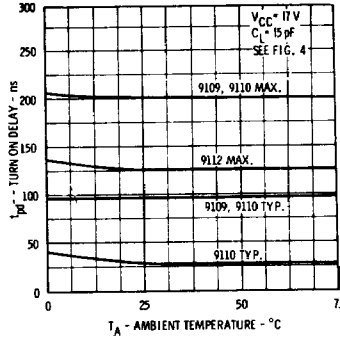
**Fig. 3f**  
**WORST CASE LOW LEVEL**  
**D.C. NOISE IMMUNITY**  
**VERSUS AMBIENT TEMPERATURE**



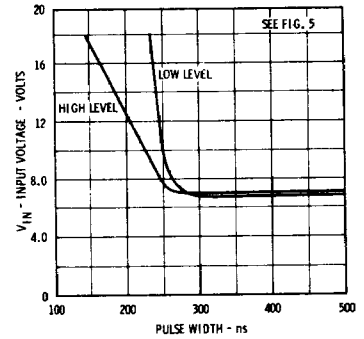
**Fig. 3g**  
**TURN OFF DELAY**  
**VERSUS AMBIENT TEMPERATURE**



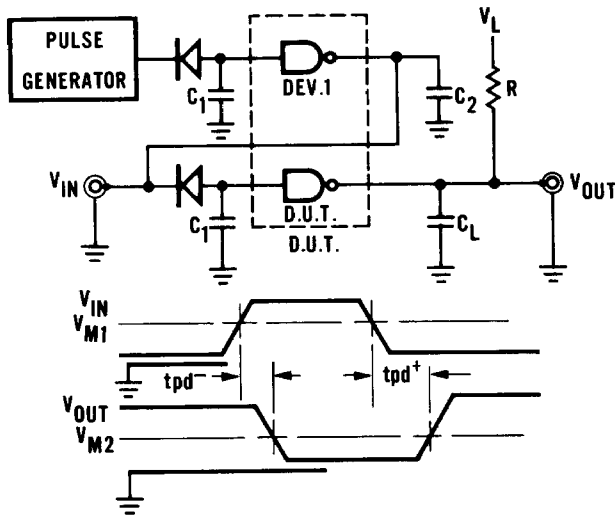
**Fig. 3h**  
**TURN ON DELAY**  
**VERSUS AMBIENT TEMPERATURE**



**Fig. 3i**  
**TYPICAL A.C. NOISE IMMUNITY**  
**INPUT VOLTAGE VERSUS**  
**PULSE WIDTH**



**Fig. 4**  
**SWITCHING TIME TEST CIRCUIT**  
**AND WAVEFORMS**



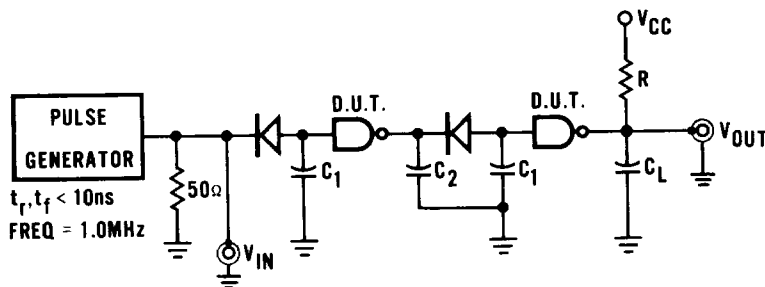
$C_1 = 5.0 \text{ pF}$  Includes all probe  
 $C_2 = 10 \text{ pF}$  and jig capacitance  
 $C_L = 15 \text{ pF}$

FDHG Input Diodes are used on 9109, 9110

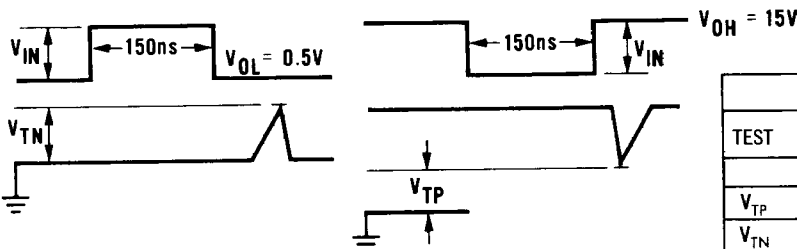
**TEST CONDITIONS**

D.U.T.	DEV. 1	$V_{m1}$ (V)	$V_{m2}$ (V)	$V_L$ (V)	$R_{tpd-}$	$R_{tpd+}$
9109	9110	7.5	1.5	5.0	510 $\Omega$	3.6 k
9110	9110	7.5	7.5	17.0	2.4 k	24 k
9112	932	1.5	7.5	17.0	2.4 k	24 k

**Fig. 5**  
**A.C. NOISE IMMUNITY TEST CIRCUIT**



Unused inputs grounded  
diodes are FDHG  
 $C_1 = 5.0 \text{ pF}$  Includes jig and  
 $C_2 = 10 \text{ pF}$  all probe capacitance  
 $C_L = 15 \text{ pF}$



**TEST CONDITIONS AND LIMITS**

TEST	LIMIT		$V_{CC}$ (Volts)	R (k $\Omega$ )	$T_A$ ( $^{\circ}$ C)	$V_{IN}$ (Volts)
	MIN.	MAX.				
$V_{TP}$	8.5 V		17	24	25	10
$V_{TN}$		7.0 V	17	2.4	25	10

APPLICATIONS:

Fig. 6—CCSL INTERFACING

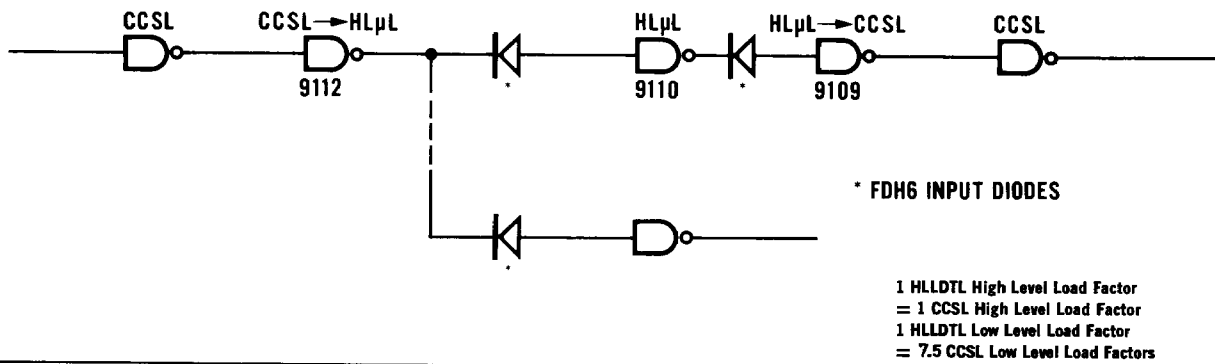


Fig. 7—LAMP DRIVER

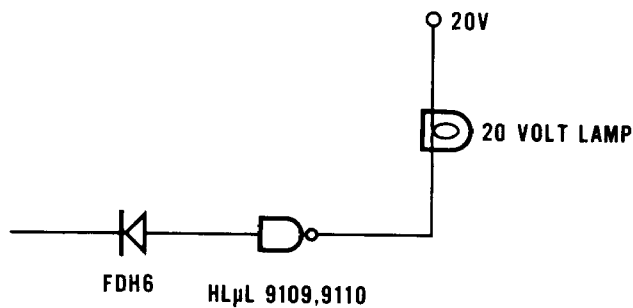
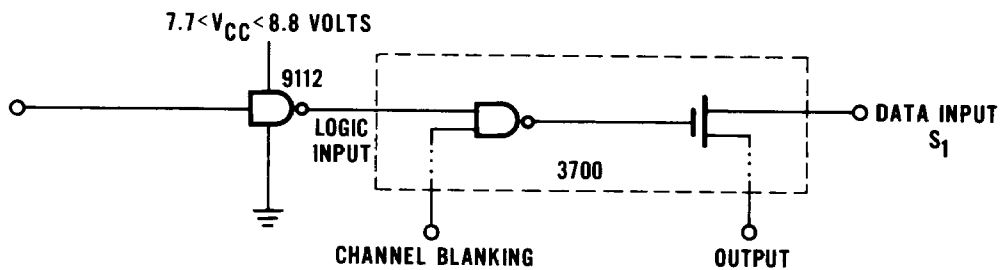
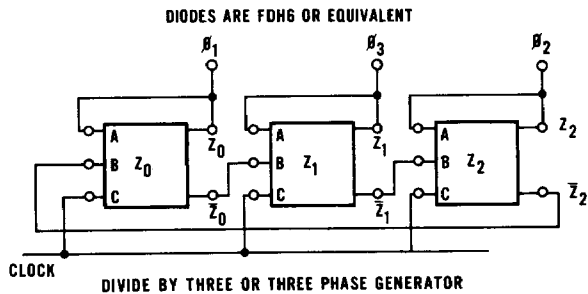


FIG. 8—DRIVING MOS3700 MULTIPLEXER OR EQUIVALENT



Output Levels : min "1" level =  $V_{CC} - 1.5 V$   
 : max "0" level = 0.2 V

Fig. 9—SEQUENTIAL COUNTER



$\phi_1$	$\phi_3$	$\phi_2$	Clock
1	0	0	0
1	0	1	1
0	0	1	0
0	1	1	1
0	1	0	0
1	1	0	1

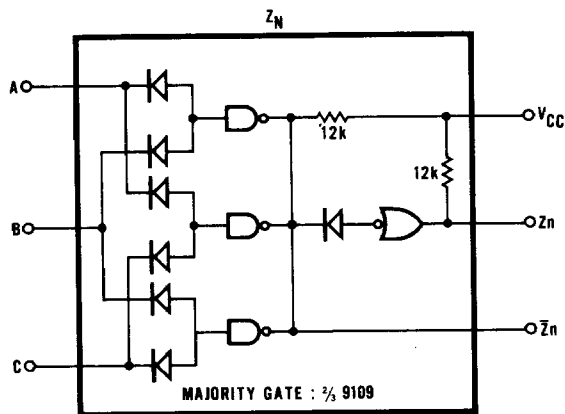
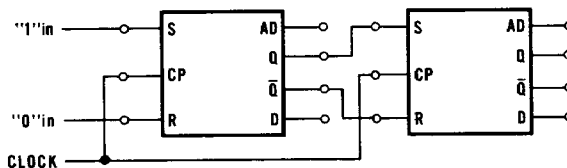
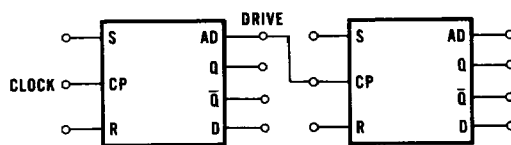
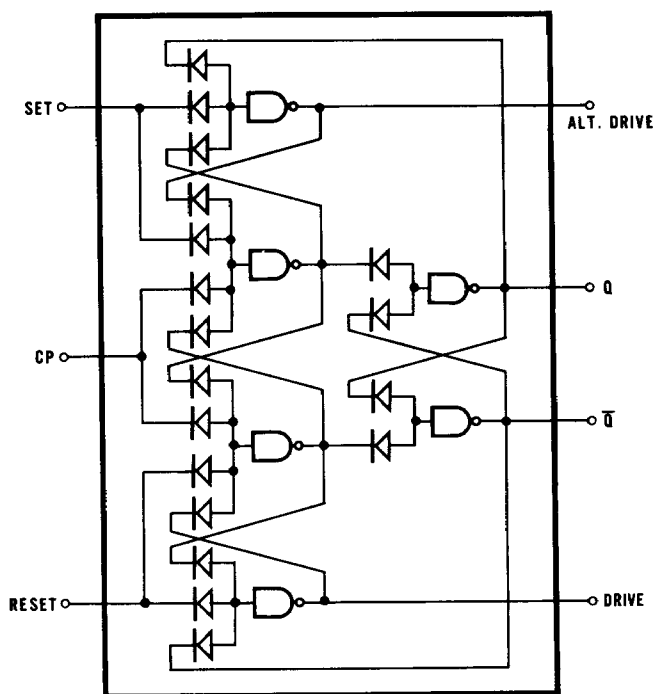


Fig. 10—JK FLIP FLOP



DIODES ARE FDH6 OR EQUIVALENT

J	K	$Q_{n+1}$
L	H	L
L	L	$Q_n$
H	H	$\bar{Q}_n$
H	L	H