

# 74HC112; 74HCT112

Dual JK flip-flop with set and reset; negative-edge trigger

Rev. 4 — 11 January 2021

Product data sheet

## 1. General description

The 74HC112; 74HCT112 is a dual negative-edge triggered JK flip-flop. It features individual J and K inputs, clock ( $\overline{CP}$ ) set ( $\overline{SD}$ ) and reset ( $\overline{RD}$ ) inputs. It also has complementary  $nQ$  and  $n\overline{Q}$  outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The J and K inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the HIGH-to-LOW clock transition for predictable operation. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

## 2. Features and benefits

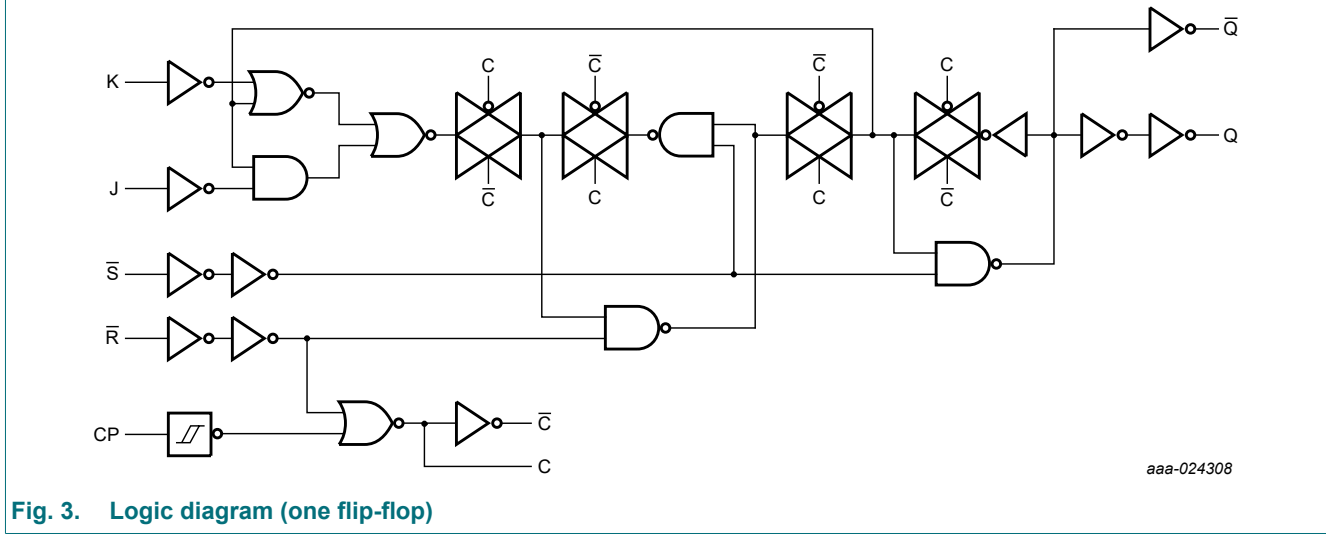
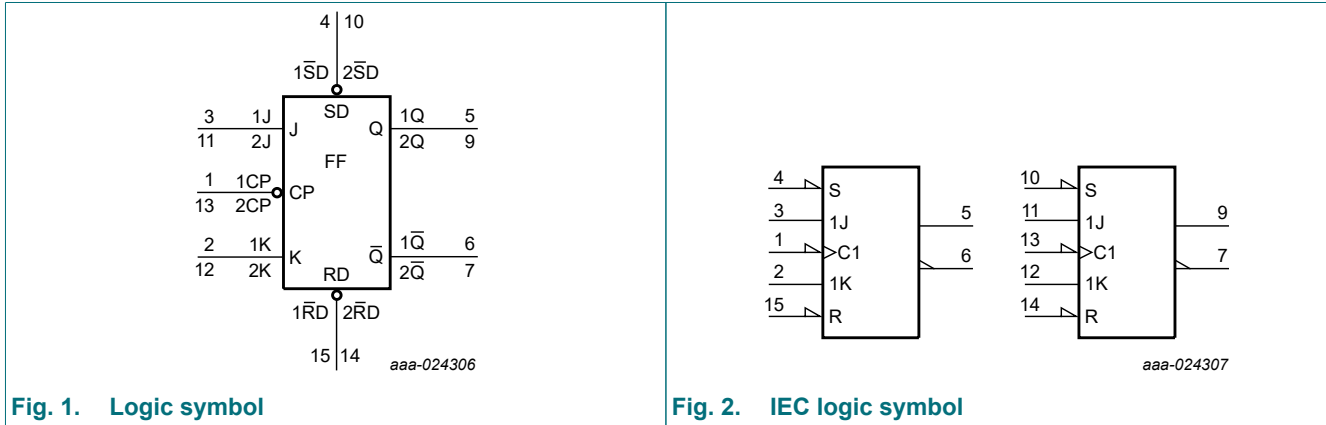
- Input levels:
  - For 74HC112: CMOS level
  - For 74HCT112: TTL level
- Asynchronous set and reset
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

## 3. Ordering information

Table 1. Ordering information

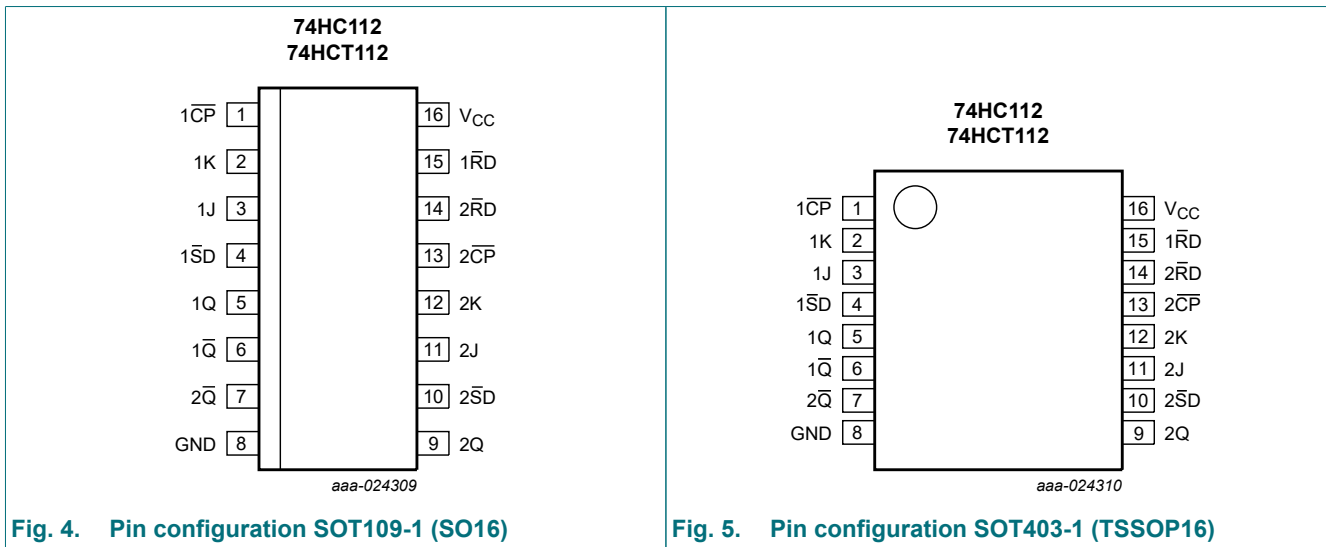
Type number	Package			
	Temperature range	Name	Description	Version
74HC112D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT112D				
74HC112PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT112PW				

### 4. Functional diagram



### 5. Pinning information

#### 5.1. Pinning



## 5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1CP, 2CP	1, 13	clock input (HIGH-to-LOW; edge-triggered)
1K, 2K	2, 12	data input
1J, 2J	3, 11	data input
1SD, 2SD	4, 10	set input (active LOW)
1Q, 2Q	5, 9	true flip-flop output
1Q̄, 2Q̄	6, 7	complement flip-flop output
GND	8	ground (0 V)
1RD, 2RD	15, 14	reset input (active LOW)
V <sub>CC</sub>	16	supply voltage

## 6. Functional description

Table 3. Function selection

If  $n\overline{SD}$  and  $n\overline{RD}$  simultaneously go from LOW-to-HIGH, the output states are unpredictable.

H = HIGH voltage level; h = HIGH voltage level one set-up time before the HIGH-to-LOW clock transition;

L = LOW voltage level; l = LOW voltage level one set-up time before the HIGH-to-LOW clock transition;

q = lowercase letters indicate the state of the referenced output one set-up time before the HIGH-to-LOW clock transition;

X = don't care; ↓ = HIGH-to-LOW clock transition.

Operating modes	Input					Output	
	nSD	nRD	nCP	nJ	nK	nQ	nQ̄
Asynchronous set	L	H	X	X	X	H	L
Asynchronous reset	H	L	X	X	X	L	H
Undetermined	L	L	X	X	X	H	L
Toggle	H	H	↓	h	h	q̄	q
Load 0 (reset)	H	H	↓	l	h	L	H
Load 1 (set)	H	H	↓	h	l	H	L
Hold no change	H	H	↓	l	l	q	q̄

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+7	V
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$	-	$\pm 20$	mA
$I_O$	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	$\pm 25$	mA
$I_{CC}$	supply current		-	+50	mA
$I_{GND}$	ground current		-50	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	[1]	-	500	mW

- [1] For SOT109-1 (SO16) package:  $P_{tot}$  derates linearly with 12.4 mW/K above 110 °C.  
For SOT403-1 (TSSOP16) package:  $P_{tot}$  derates linearly with 8.5 mW/K above 91 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC112			74HCT112			Unit
			Min	Typ	Max	Min	Typ	Max	
$V_{CC}$	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
$V_I$	input voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0\text{ V}$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5\text{ V}$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0\text{ V}$	-	-	83	-	-	-	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
<b>74HC112</b>										
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	1.2	-	1.5	-	1.5	-	V
		$V_{CC} = 4.5\text{ V}$	3.15	2.4	-	3.15	-	3.15	-	V
		$V_{CC} = 6.0\text{ V}$	4.2	3.2	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.8	0.5	-	0.5	-	0.5	V
		$V_{CC} = 4.5\text{ V}$	-	2.1	1.35	-	1.35	-	1.35	V
		$V_{CC} = 6.0\text{ V}$	-	2.8	1.8	-	1.8	-	1.8	V

## Dual JK flip-flop with set and reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -20 µA; V <sub>CC</sub> = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I <sub>O</sub> = -4.0 mA; V <sub>CC</sub> = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I <sub>O</sub> = -5.2 mA; V <sub>CC</sub> = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I <sub>O</sub> = 5.2 mA; V <sub>CC</sub> = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 6.0 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	4.0	-	40	-	80	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF
<b>74HCT112</b>										
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I <sub>O</sub> = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 4.5 V								
		I <sub>O</sub> = 20 µA; V <sub>CC</sub> = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I <sub>O</sub> = 4.0 mA; V <sub>CC</sub> = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	4.0	-	40	-	80	µA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 4.5 V to 5.5 V								
		n $\overline{S}$ D inputs	-	50	180	-	225	-	245	µA
		nK inputs	-	60	216	-	270	-	294	µA
		n $\overline{R}$ D inputs	-	65	236	-	293	-	319	µA
		nJ, and n $\overline{C}$ P inputs	-	100	360	-	450	-	490	µA
C <sub>I</sub>	input capacitance		-	3.5	-	-	-	-	-	pF

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V);  $C_L = 50$  pF unless otherwise specified; for test circuit, see Fig. 8.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
<b>74HC112</b>										
$t_{pd}$	propagation delay	$n\overline{CP}$ to $nQ$ ; see Fig. 6 [2]								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		$n\overline{CP}$ to $n\overline{Q}$ ; see Fig. 6								
		$V_{CC} = 2.0$ V	-	55	175	-	220	-	265	ns
		$V_{CC} = 4.5$ V	-	20	35	-	44	-	53	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	17	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	16	30	-	37	-	45	ns
		$n\overline{RD}$ to $nQ$ , $n\overline{Q}$ ; see Fig. 7								
		$V_{CC} = 2.0$ V	-	58	180	-	225	-	270	ns
		$V_{CC} = 4.5$ V	-	21	36	-	45	-	54	ns
		$V_{CC} = 5$ V; $C_L = 15$ pF	-	18	-	-	-	-	-	ns
		$V_{CC} = 6.0$ V	-	17	31	-	38	-	46	ns
		$n\overline{SD}$ to $nQ$ , $n\overline{Q}$ ; see Fig. 7								
$V_{CC} = 2.0$ V	-	50	155	-	295	-	235	ns		
$V_{CC} = 4.5$ V	-	18	31	-	39	-	47	ns		
$V_{CC} = 5$ V; $C_L = 15$ pF	-	15	-	-	-	-	-	ns		
$V_{CC} = 6.0$ V	-	14	26	-	33	-	40	ns		
$t_t$	transition time	$nQ$ , $n\overline{Q}$ ; see Fig. 6 [3]								
		$V_{CC} = 2.0$ V	-	19	75	-	95	-	110	ns
		$V_{CC} = 4.5$ V	-	7	15	-	19	-	22	ns
		$V_{CC} = 6.0$ V	-	6	13	-	16	-	19	ns
$t_w$	pulse width	$n\overline{CP}$ HIGH or LOW; see Fig. 6								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
		$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns
		$n\overline{SD}$ , $n\overline{RD}$ LOW; see Fig. 7								
		$V_{CC} = 2.0$ V	80	22	-	100	-	120	-	ns
		$V_{CC} = 4.5$ V	16	8	-	20	-	24	-	ns
$V_{CC} = 6.0$ V	14	6	-	17	-	20	-	ns		

## Dual JK flip-flop with set and reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>rec</sub>	recovery time	nRD to nCP; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	80	22	-	125	-	150	-	ns
		V <sub>CC</sub> = 4.5 V	16	8	-	25	-	30	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	21	-	26	-	ns
		nSD to nCP; see Fig. 7								
		V <sub>CC</sub> = 2.0 V	80	-19	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	-7	-	20	-	24	-	ns
V <sub>CC</sub> = 6.0 V	14	-6	-	17	-	20	-	ns		
t <sub>su</sub>	set-up time	nJ and nK to nCP; see Fig. 6								
		V <sub>CC</sub> = 2.0 V	80	19	-	100	-	120	-	ns
		V <sub>CC</sub> = 4.5 V	16	7	-	20	-	24	-	ns
		V <sub>CC</sub> = 6.0 V	14	6	-	17	-	20	-	ns
t <sub>h</sub>	hold time	nJ and nK to nCP; see Fig. 6								
		V <sub>CC</sub> = 2.0 V	0	-11	-	0	-	0	-	ns
		V <sub>CC</sub> = 4.5 V	0	-4	-	0	-	0	-	ns
		V <sub>CC</sub> = 6.0 V	0	-3	-	0	-	0	-	ns
f <sub>max</sub>	maximum frequency	nCP; see Fig. 6								
		V <sub>CC</sub> = 2.0 V	6	20	-	4.8	-	4.0	-	MHz
		V <sub>CC</sub> = 4.5 V	30	60	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	66	-	-	-	-	-	MHz
		V <sub>CC</sub> = 6.0 V	35	71	-	28	-	24	-	MHz
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	[4]	-	27	-	-	-	-	pF
<b>74HCT112</b>										
t <sub>pd</sub>	propagation delay	nCP to nQ; see Fig. 6 [2]								
		V <sub>CC</sub> = 4.5 V	-	21	35	-	44	-	53	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	19	-	-	-	-	-	ns
		nCP to nQ; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	-	23	40	-	50	-	60	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	19	-	-	-	-	-	ns
		nRD to nQ, nQ; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	-	22	37	-	46	-	56	ns
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	19	-	-	-	-	-	ns
		nSD to nQ, nQ; see Fig. 7								
V <sub>CC</sub> = 4.5 V	-	18	32	-	40	-	48	ns		
V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	15	-	-	-	-	-	ns		
t <sub>t</sub>	transition time	nQ, nQ; see Fig. 6 [3]								
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
t <sub>w</sub>	pulse width	nCP HIGH or LOW; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	16	8	-	20	-	24	-	ns
		nSD, nRD LOW; see Fig. 7								
V <sub>CC</sub> = 4.5 V	18	10	-	23	-	27	-	ns		

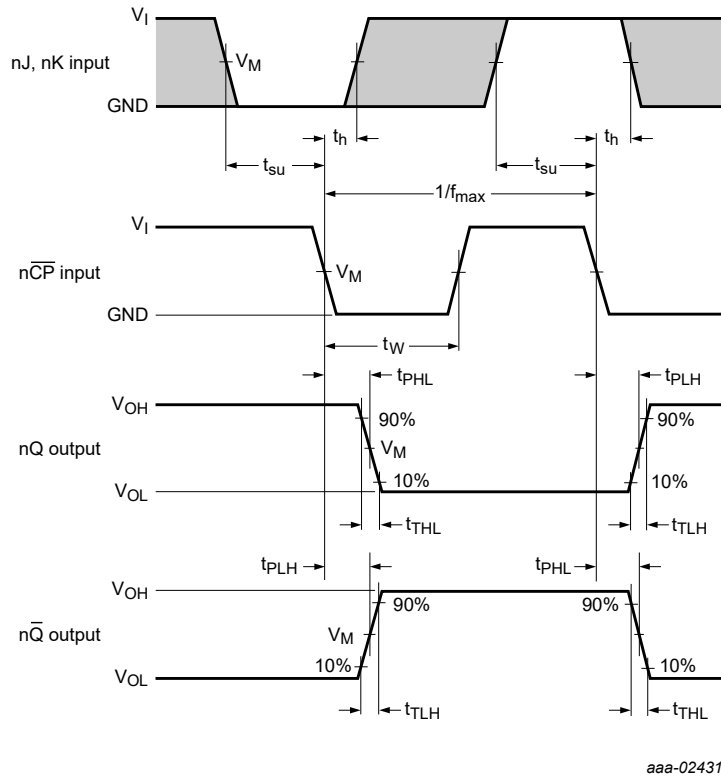
## Dual JK flip-flop with set and reset; negative-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t <sub>rec</sub>	recovery time	nRD to nCP; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	20	11	-	25	-	30	-	ns
		nSD to nCP; see Fig. 7								
		V <sub>CC</sub> = 4.5 V	20	-8	-	25	-	30	-	ns
t <sub>su</sub>	set-up time	nJ and nK to nCP; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	16	7	-	20	-	24	-	ns
t <sub>h</sub>	hold time	nJ and nK to nCP; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	0	-7	-	0	-	0	-	ns
f <sub>max</sub>	maximum frequency	nCP; see Fig. 6								
		V <sub>CC</sub> = 4.5 V	30	64	-	24	-	20	-	MHz
		V <sub>CC</sub> = 5 V; C <sub>L</sub> = 15 pF	-	70	-	-	-	-	-	MHz
C <sub>PD</sub>	power dissipation capacitance	C <sub>L</sub> = 50 pF; f = 1 MHz; V <sub>I</sub> = GND to V <sub>CC</sub>	[4]	-	30	-	-	-	-	pF

- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.  
 [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 [3] t<sub>i</sub> is the same as t<sub>THL</sub> and t<sub>TLH</sub>.  
 [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz;  
 f<sub>o</sub> = output frequency in MHz;  
 C<sub>L</sub> = output load capacitance in pF;  
 V<sub>CC</sub> = supply voltage in V;  
 N = number of inputs switching;  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs.



10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical voltage output levels that occur with the output load.

**Fig. 6. Clock propagation delays, output transition time, pulse width, set-up, hold times, and maximum frequency**

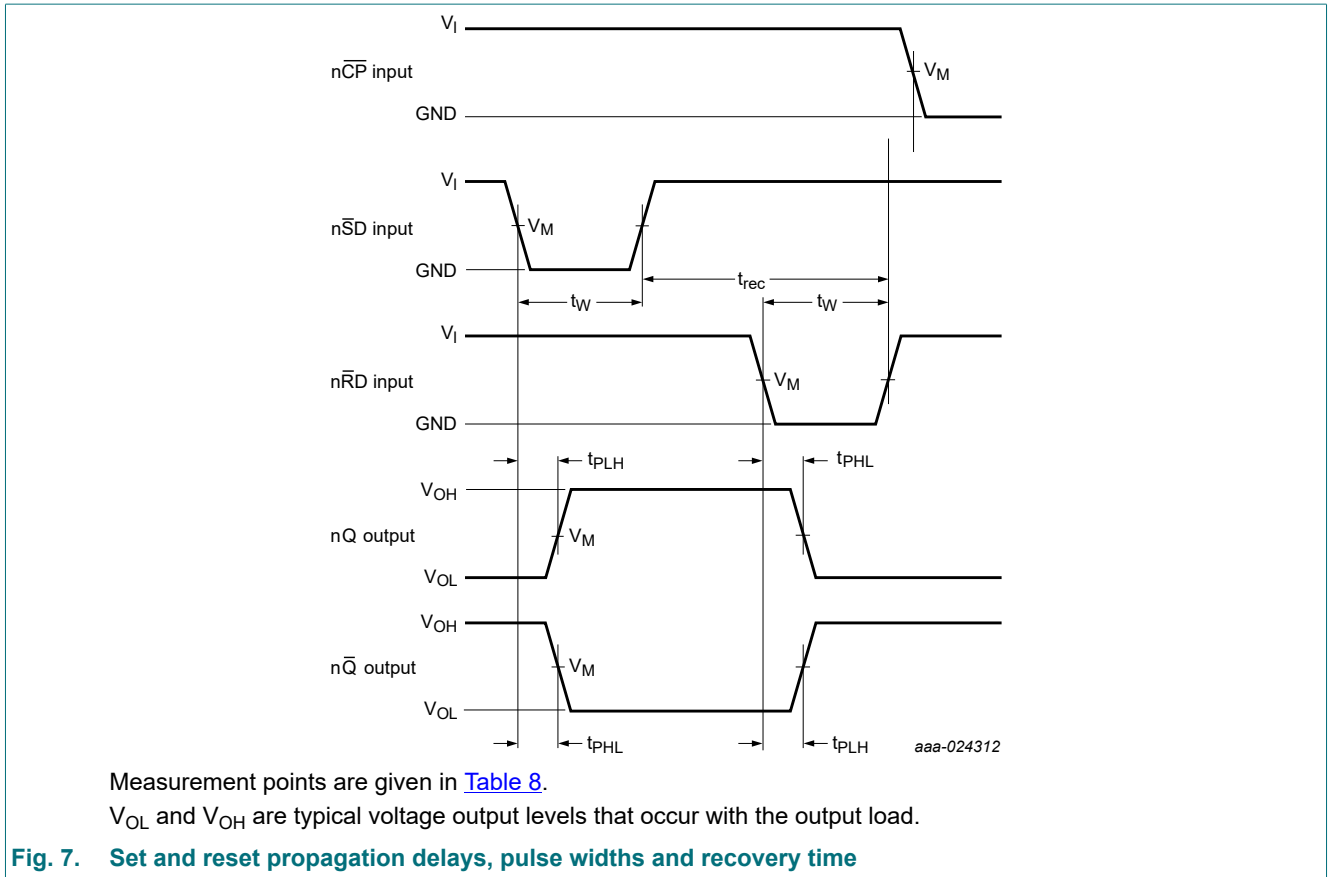


Table 8. Measurement points

Type	Input	Output
	$V_M$	$V_M$
74HC112	$0.5V_{CC}$	$0.5V_{CC}$
74HCT112	1.3 V	1.3 V

Dual JK flip-flop with set and reset; negative-edge trigger

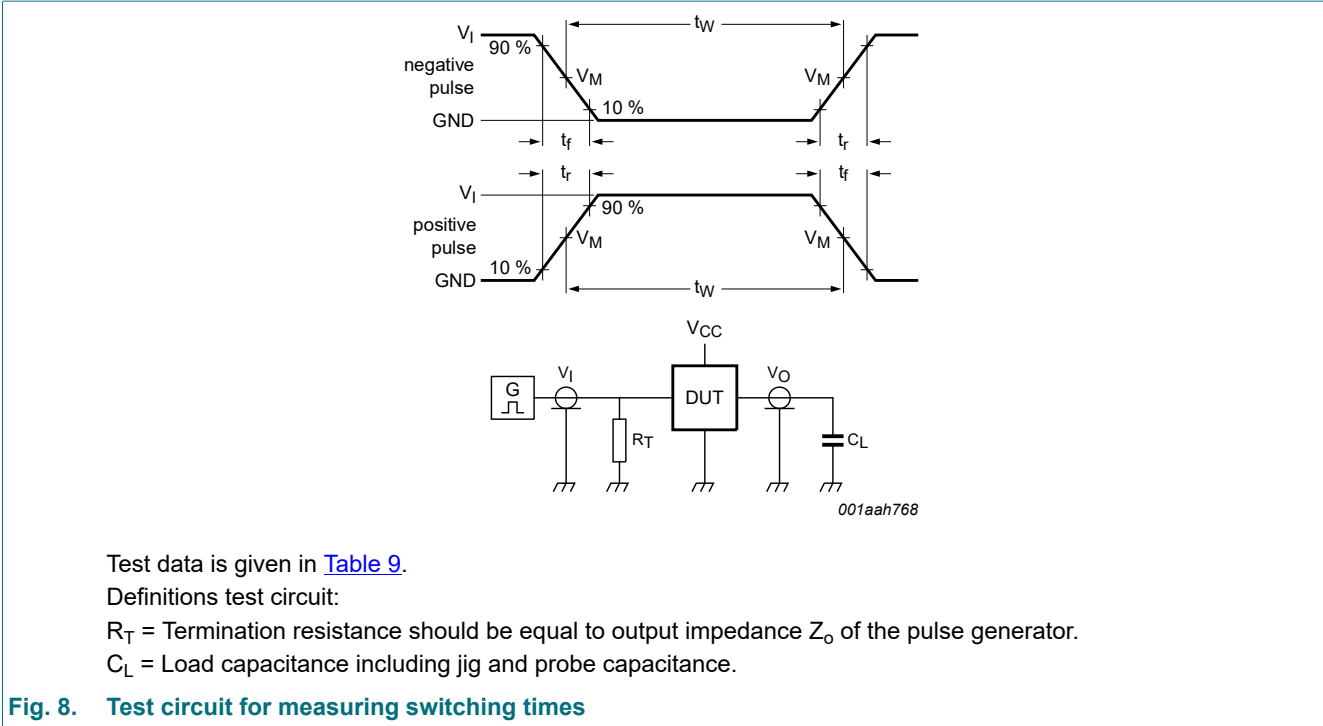


Fig. 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	$V_I$	$t_r, t_f$	$C_L$	
74HC112	$V_{CC}$	6 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$
74HCT112	3 V	6 ns	15 pF, 50 pF	$t_{PLH}, t_{PHL}$

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



Fig. 9. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

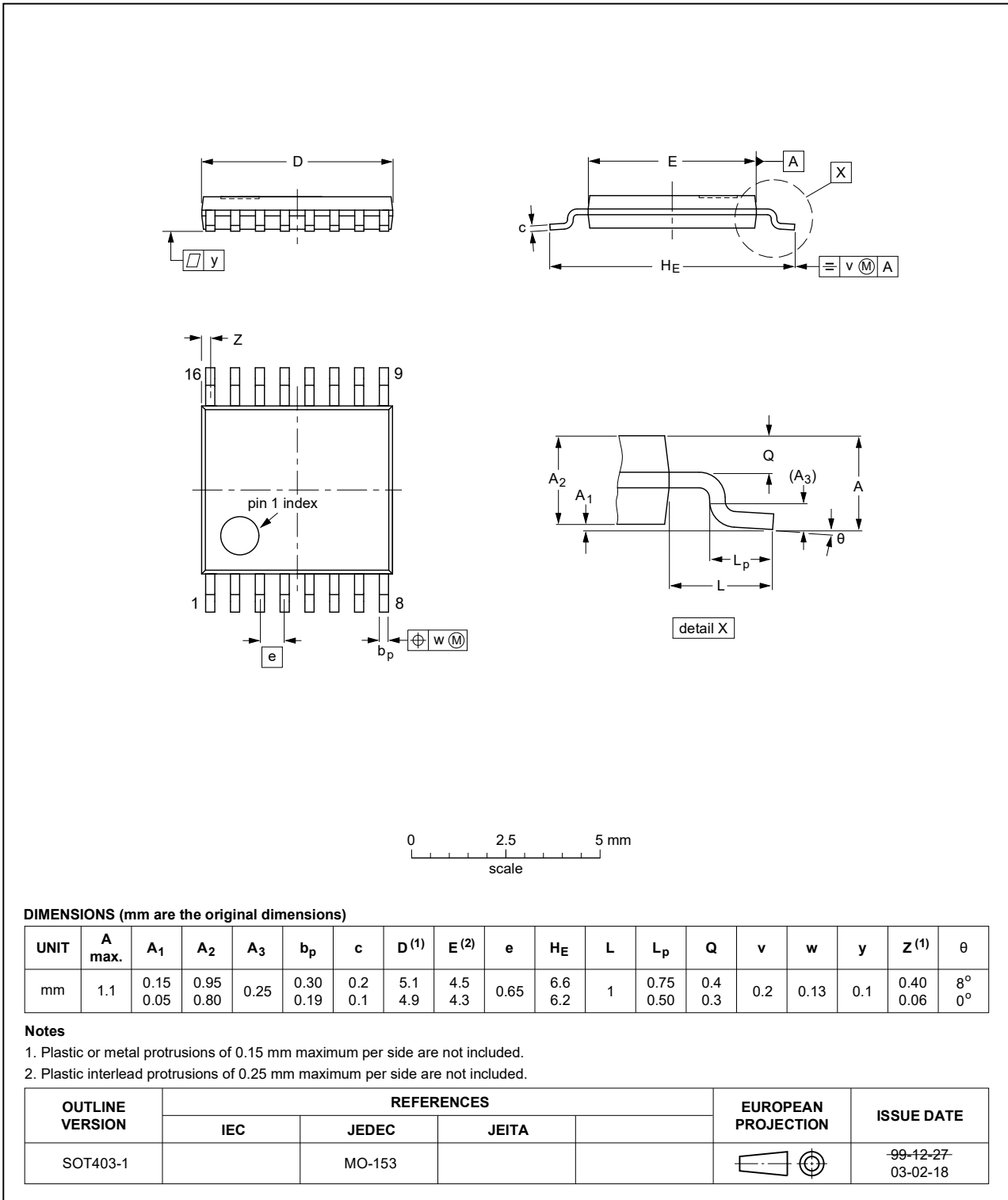


Fig. 10. Package outline SOT403-1 (TSSOP16)

## 12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT112 v.4	20210111	Product data sheet	-	74HC_HCT112 v.3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC112DB and 74HCT112DB (SOT338-1 / SSOP16) removed.</li> <li><a href="#">Section 7</a>: Derating values for <math>P_{tot}</math> total power dissipation have been updated.</li> </ul>			
74HC_HCT112 v.3	20160809	Product data sheet	-	74HC_HCT112_CNV v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Type numbers 74HC112N and 74HCT112N removed.</li> </ul>			
74HC_HCT112_CNV v.2	19980610	Product specification	-	-

## 14. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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