

54AC377 • 54ACT377 Octal D Flip-Flop with Clock Enable

General Description

The 'AC/'ACT377 has eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) input loads all flip-flops simultaneously, when the Clock Enable (\overline{CE}) is LOW.

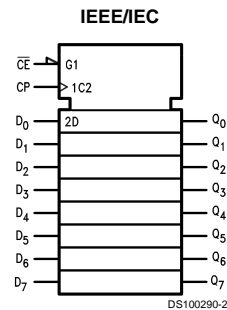
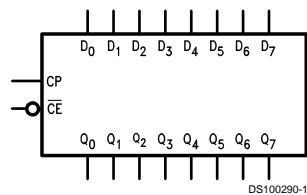
The register is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The \overline{CE} input must be stable only one setup time prior to the LOW-to-HIGH clock transition for predictable operation.

Features

- I_{CC} reduced by 50%

- Ideal for addressable register applications
- Clock enable for address and data synchronization applications
- Eight edge-triggered D flip-flops
- Buffered common clock
- Outputs source/sink 24 mA
- See '273 for master reset version
- See '373 for transparent latch version
- See '374 for TRI-STATE® version
- 'ACT377 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
 - 'AC377: 5962-88702
 - 'ACT377: 5962-87697

Logic Symbols

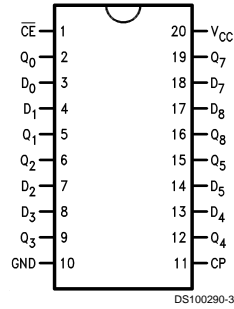


Pin Names	Description
D_0 – D_7	Data Inputs
\overline{CE}	Clock Enable (Active LOW)
Q_0 – Q_7	Data Outputs
CP	Clock Pulse Input

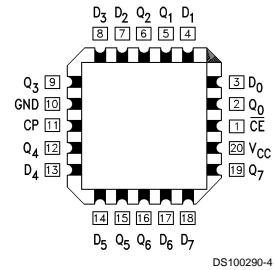
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Connection Diagrams

Pin Assignment
for DIP and Flatpak



Pin Assignment
for LCC

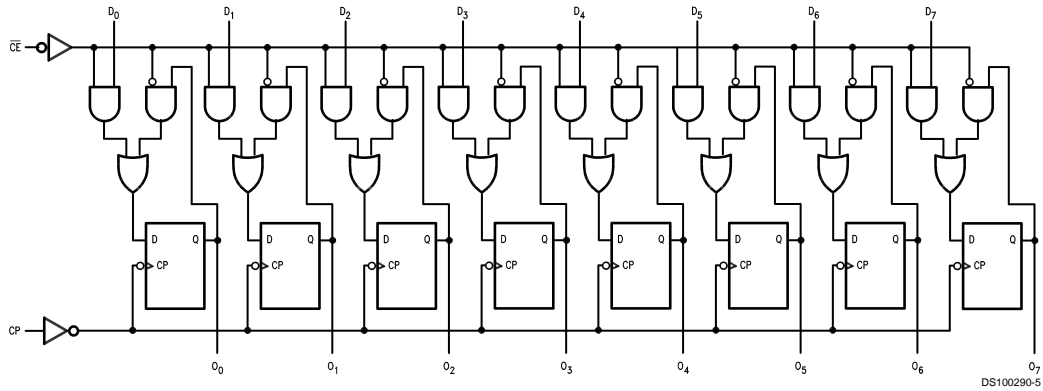


Mode Select-Function Table

Operating Mode	Inputs			Outputs
	CP	CĒ	D _n	Q _n
Load '1'	↗	L	H	H
Load '0'	↗	L	L	L
Hold (Do Nothing)	↗	H	X	No Change
	X	H	X	No Change

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'AC	2.0V to 6.0V
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54AC/ACT	-55°C to +125°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: See individual datasheets for those devices which differ from the typical input rise and fall times noted here.

DC Characteristics for 'AC Family Devices

Symbol	Parameter	V_{CC} (V)	54AC	Units	Conditions	
			$T_A =$ -55°C to +125°C			
			Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	3.15			
		5.5	3.85			
V_{IL}	Maximum Low Level Input Voltage	3.0	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$	
		4.5	1.35			
		5.5	1.65			
V_{OH}	Minimum High Level Output Voltage	3.0	2.9	V	$I_{OUT} = -50 \mu A$	
		4.5	4.4			
		5.5	5.4			
			3.0	2.4	V	(Note 3) $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12 \text{ mA}$ $I_{OH} = -24 \text{ mA}$ $I_{OH} = -24 \text{ mA}$
			4.5	3.7		
			5.5	4.7		
V_{OL}	Maximum Low Level Output Voltage	3.0	0.1	V	$I_{OUT} = 50 \mu A$	
		4.5	0.1			
		5.5	0.1			
			3.0	0.50	V	(Note 3) $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12 \text{ mA}$ $I_{OL} = 24 \text{ mA}$ $I_{OL} = 24 \text{ mA}$
			4.5	0.50		
			5.5	0.50		
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}, GND$	

DC Characteristics for 'AC Family Devices (Continued)

Symbol	Parameter	V _{CC} (V)	54AC	Units	Conditions
			T _A = -55°C to +125°C		
			Guaranteed Limits		
I _{OLD}	(Note 4) Minimum Dynamic Output Current	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	-50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC}.

I_{CC} for 54AC @ 25°C is identical to 74AC @ 25°C.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V _{CC} (V)	54ACT	Units	Conditions
			T _A = -55°C to +125°C		
			Guaranteed Limits		
V _{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	2.0		
V _{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	0.8		
V _{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I _{OUT} = -50 μA
		5.5	5.4		
		4.5	3.70	V	(Note 6) V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA
		5.5	4.70		
V _{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I _{OUT} = 50 μA
		5.5	0.1		
		4.5	0.50	V	(Note 6) V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA
		5.5	0.50		
I _{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	1.6	mA	V _I = V _{CC} - 2.1V
I _{OLD}	(Note 7) Minimum Dynamic Output Current	5.5	50	mA	V _{OLD} = 1.65V Max
I _{OHD}		5.5	-50	mA	V _{OHD} = 3.85V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	80.0	μA	V _{IN} = V _{CC} or GND

Note 6: *All outputs loaded; thresholds on input associated with output under test.

Note 7: †Maximum test duration 2.0 ms, one output loaded at a time.

Note 8: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 9)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
f _{max}	Maximum Clock Frequency	3.3 5.0	75 95		MHz	
t _{PLH}	Propagation Delay CP to Q _n	3.3 5.0	1.0 1.5	14.0 10.0	ns	
t _{PHL}	Propagation Delay CP to Q _n	3.3 5.0	1.0 1.5	15.0 11.0	ns	

Note 9: Voltage Range 3.3 is 3.3V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V _{CC} (V) (Note 10)	54AC		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Guaranteed Minimum			
t _s	Setup Time, HIGH or LOW D _n to CP	3.3 5.0	7.5 6.0		ns	
t _h	Hold Time, HIGH or LOW D _n to CP	3.3 5.0	1.5 2.5		ns	
t _s	Setup Time, HIGH or LOW \overline{CE} to CP	3.3 5.0	9.5 6.0		ns	
t _h	Hold Time, HIGH or LOW \overline{CE} to CP	3.3 5.0	1.0 2.0		ns	
t _w	CP Pulse Width HIGH or LOW	3.3 5.0	6.5 5.0		ns	

Note 10: Voltage Range 3.3 is 3.0V ±0.3V
Voltage Range 5.0 is 5.0V ±0.5V

AC Electrical Characteristics

Symbol	Parameter	V _{CC} (V) (Note 11)	54ACT		Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF			
			Min	Max		
f _{max}	Maximum Clock Frequency	5.0	85		MHz	
t _{PLH}	Propagation Delay CP to Q _n	5.0	1.5	11.0	ns	
t _{PHL}	Propagation Delay CP to Q _n	5.0	1.5	12.0	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

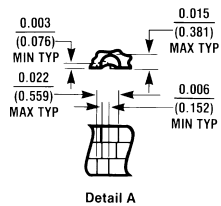
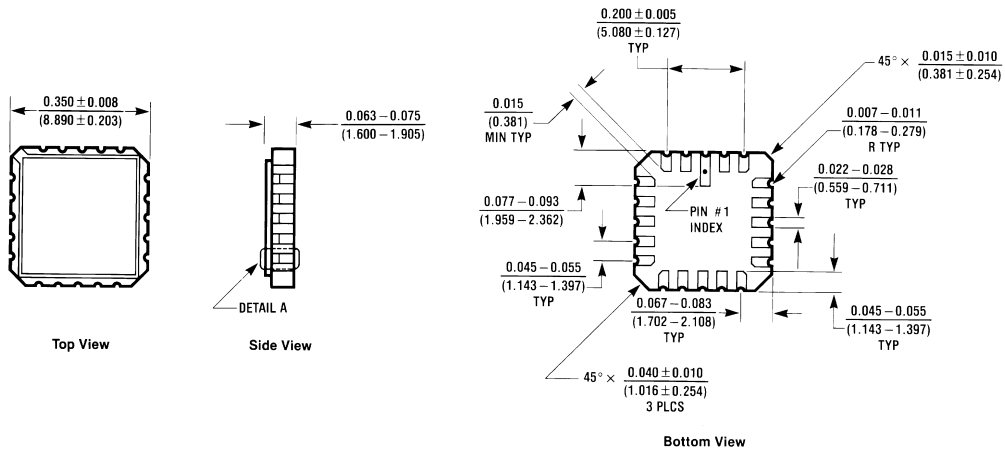
Symbol	Parameter	V _{CC} (V) (Note 12)	54ACT	Units	Fig. No.
			T _A = -55°C to +125°C C _L = 50 pF		
			Guaranteed Minimum		
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	7.0	ns	
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	1.0	ns	
t _s	Setup Time, HIGH or LOW CE to CP	5.0	7.0	ns	
t _h	Hold Time, HIGH or LOW CE to CP	5.0	1.0	ns	
t _w	CP Pulse Width HIGH or LOW	5.0	5.5	ns	

Note 12: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

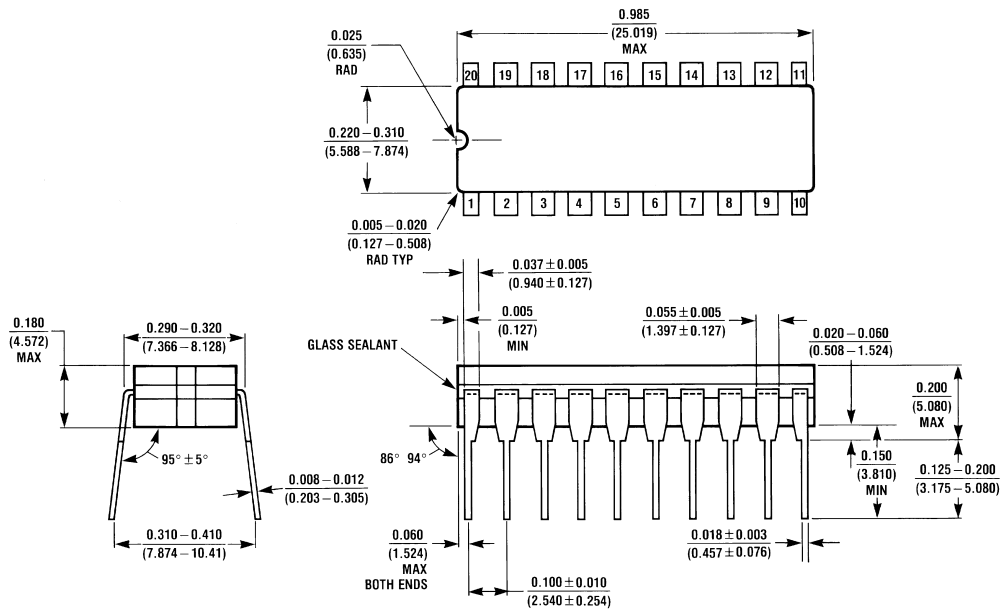
Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	90.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

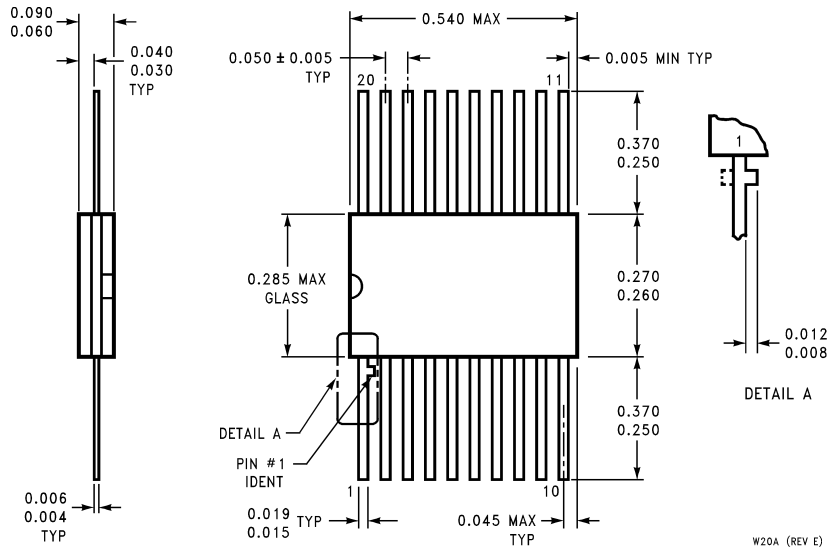
E20A (REV D)



20 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

J20A (REV M)

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**20 Lead Ceramic Flatpak (F)
NS Package Number W20A**

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Datasheet

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54AC377 54ACT377 Octal D Flip-Flop with Clock Enable	177 Kbytes	2-Feb-99	View Online	Download	Receive via Email
54AC377 Mil-Aero Datasheet MN54AC377-X	15 Kbytes		View Online	Download	Receive via Email

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Part Number	Package			Status	Models		Samples & Electronic Orders	Budgetary Pricing		Std Pack Size	Package Marking
	Type	Pins	MSL		SPICE	IBIS		Qty	\$US each		
5962-88702012A (54AC377LMQB)	LCC	20	MSL	Full production	N/A	N/A	Buy Now	50+	\$11.0000	rail of 50	[logo]cZcSc4cA54AC377LMQB/QcMSE5962-88702012A
5962-8870201RA (54AC377DMQB)	CERDIP	20	MSL	Full production	N/A	N/A	Buy Now	50+	\$8.6000	rail of 20	[logo]cZcSc4cA54AC377DMQB/QcM5962-8870201RA
5962-8870201SA (54AC377FMQB)	CERPACK	20	MSL	Full production	N/A	N/A		50+	\$11.0000	rail of 19	[logo]cZcSc4cA54AC377FMQBQcM5962-8870201SA
JM54AC377B2A-RH	LCC	20	MSL	Full production	N/A	N/A				rail of N/A	[logo]JM38510R75603B2A27014QScZcSc4cA54
JM38510/75603B2	LCC	20	MSL	Full production	N/A	N/A		50+	\$13.6000	rail of 50	[logo]JM38510/75603B2A27014QScZcSc4cA54
JM54AC377BRA-RH	CERDIP	20	MSL	Full production	N/A	N/A				rail of N/A	[logo]cZcSc4cA54JM38510R75603BRA27014QS

JM38510/75603BS	CERPACK	20	MSL	Full production	N/A	N/A		50+	\$13.6000	rail of 19	[logo]cZcSc4cASE JM38510/75603BSA 27014 QS
R75603BSA	CERPACK	20	MSL	Full production	N/A	N/A		50+	\$73.0000	rail of 19	[logo]cZcSc4cASE JM38510R 75603BSA 27014 QS
JM54AC377S2A-RH	LCC	20	MSL	Full production	N/A	N/A				rail of N/A	[logo]cZcSc4cA 27014 QSE JM38510R 75603S2A
JM54AC377SRA-RH	CERDIP	20	MSL	Full production	N/A	N/A				rail of N/A	[logo]cZcSc4cASE JM38510R75603SRA 27014 Q
RM54AC377SSA	CERPACK	20	MSL	Preliminary	N/A	N/A				rail of N/A	[logo]cZcSc4cASE RM54AC377 SSA WAFER # cR
JM38510/75603SS	CERPACK	20	MSL	Full production	N/A	N/A		50+	\$138.0000	rail of 19	[logo]cZcSc4cASE 27014 JM38510/75603SSA Q
JM38510R75603SS	CERPACK	20	MSL	Full production	N/A	N/A		50+	\$138.0000	rail of 19	[logo]cZcSc4cASE 27014 JM38510R 75603SSA Q

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