

74F109

Dual JK Positive Edge-Triggered Flip-Flop

General Description

The F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D-type flip-flop (refer to F74 data sheet) by connecting the J and \bar{K} inputs.

Asynchronous Inputs:

LOW input to \bar{S}_D sets Q to HIGH level

LOW input to \bar{C}_D sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on \bar{C}_D and \bar{S}_D makes

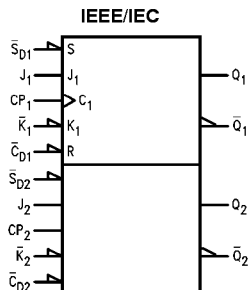
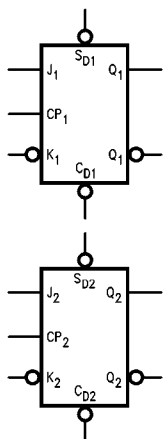
both Q and \bar{Q} HIGH

Ordering Code:

Order Number	Package Number	Package Description
74F109SC	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body
74F109SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE 11, 5.3mm Wide
74F109PC	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

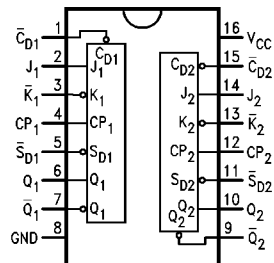
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram

Pin Assignment for DIP and SOIC



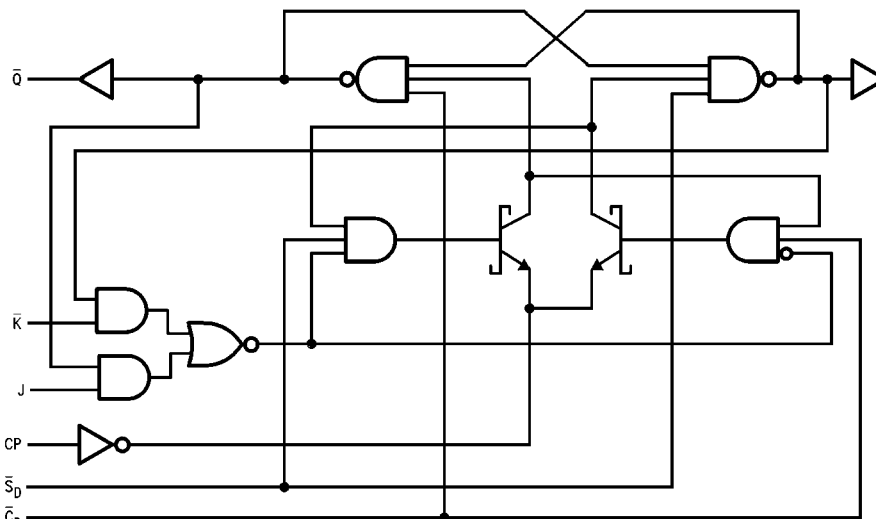
Truth Table

Inputs					Outputs	
\bar{S}_D	\bar{C}_D	CP	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H	H
H	H	↗	l	l	L	H
H	H	↗	h	l	Toggle	
H	H	↗	l	h	Q	Q
H	H	↗	h	h	H	L
H	H	L	X	X	Q	Q

H (h) = HIGH Voltage Level
 L (l) = LOW Voltage Level
 ↗ = LOW-to-HIGH Transition
 X = Immaterial
 Q_0 (\bar{Q}_0) = Before LOW-to-HIGH Transition of Clock
 Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram

(One Half Shown)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Unit Loading/Fan Out

Pin Names	Description	U.L.	Input I_{IH}/I_{IL}
		HIGH/LOW	Output I_{OH}/I_{OL}
$J_1, J_2, \bar{K}_1, \bar{K}_2$	Data Inputs	1.0/1.0	20 μA / -0.6 mA
CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)	1.0/1.0	20 μA / -0.6 mA
$\bar{C}_{D1}, \bar{C}_{D2}$	Direct Clear Inputs (Active LOW)	1.0/3.0	20 μA / -1.8 mA
$\bar{S}_{D1}, \bar{S}_{D2}$	Direct Set Inputs (Active LOW)	1.0/3.0	20 μA / -1.8 mA
$Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$	Outputs	50/33.3	-1 mA / 20 mA

Absolute Maximum Ratings (Note 1)	3-STATE Output	-0.5V to +5.5V
Storage Temperature	Current Applied to Output	
Ambient Temperature under Bias	in LOW State (Max)	twice the rated I_{OL} (mA)
Junction Temperature under Bias		
V_{CC} Pin Potential to Ground Pin		
Input Voltage (Note 2)		
Input Current (Note 2)		
Voltage Applied to Output in HIGH State (with $V_{CC} = 0V$)		
Standard Output		

Recommended Operating Conditions		
Free Air Ambient Temperature	0°C to +70°C	
Supply Voltage	+4.5V to +5.5V	

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			-1.2	V	Min	$I_{IN} = -18$ mA
V_{OH}	Output HIGH Voltage	10% V_{CC} 5% V_{CC}	2.5 2.7		V	Min	$I_{OH} = -1$ mA $I_{OH} = -1$ mA
V_{OL}	Output LOW Voltage	10% V_{CC}		0.5	V	Min	$I_{OL} = 20$ mA
I_{IH}	Input HIGH Current			5.0	μ A	Max	$V_{IN} = 2.7V$
I_{BVI}	Input HIGH Current Breakdown Test			7.0	μ A	Max	$V_{IN} = 7.0V$
I_{CEX}	Output HIGH Leakage Current			50	μ A	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	4.75			V	0.0	$I_{ID} = 1.9$ μ A All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current			3.75	μ A	0.0	$V_{IOD} = 150$ mV All Other Pins Grounded
I_{IL}	Input LOW Current			-0.6 -1.8	mA	Max	$V_{IN} = 0.5V$ (J_n, \bar{K}_n) $V_{IN} = 0.5V$ ($\bar{C}_{Dn}, \bar{S}_{Dn}$)
I_{OS}	Output Short-Circuit Current	-60		-150	mA	Max	$V_{OUT} = 0V$
I_{CC}	Power Supply Current		11.7	17.0	mA	Max	CP = 0V

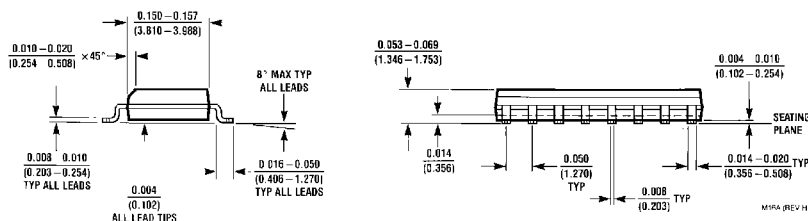
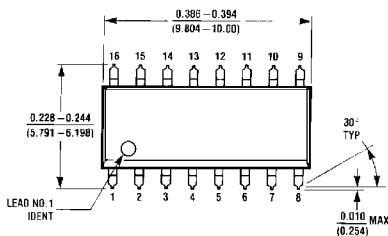
AC Electrical Characteristics

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	
f_{max}	Maximum Clock Frequency	100	125		90		MHz
t_{PLH}	Propagation Delay	3.8	5.3	7.0	3.8	8.0	ns
t_{PHL}	CP_n to Q_n or \bar{Q}_n	4.4	6.2	8.0	4.4	9.2	ns
t_{PLH}	Propagation Delay	3.2	5.2	7.0	3.2	8.0	ns
t_{PHL}	\bar{C}_{Dn} or \bar{S}_{Dn} to Q_n or \bar{Q}_n	3.5	7.0	9.0	3.5	10.5	ns

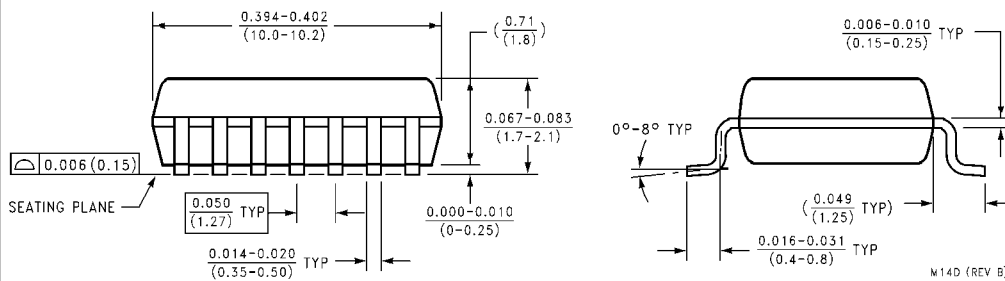
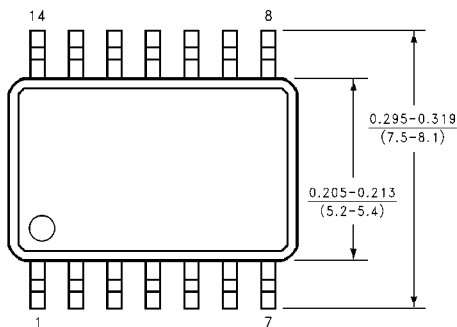
AC Operating Requirements

Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$		Units
		Min	Max	Min	Max	
$t_{\text{S(H)}}$	Setup Time, HIGH or LOW	3.0		3.0		ns
$t_{\text{S(L)}}$	J_n or \bar{K}_n to CP_n	3.0		3.0		
$t_{\text{H(H)}}$	Hold Time, HIGH or LOW	1.0		1.0		ns
$t_{\text{H(L)}}$	J_n or \bar{K}_n to CP_n	1.0		1.0		
$t_{\text{W(H)}}$	CP_n Pulse Width	4.0		4.0		ns
$t_{\text{W(L)}}$	HIGH or LOW	5.0		5.0		ns
$t_{\text{W(L)}}$	\bar{C}_{Dn} or \bar{S}_{Dn} Pulse Width LOW	4.0		4.0		ns
t_{rec}	Recovery Time \bar{C}_{Dn} or \bar{S}_{Dn} to CP	2.0		2.0		ns

Physical Dimensions inches (millimeters) unless otherwise noted

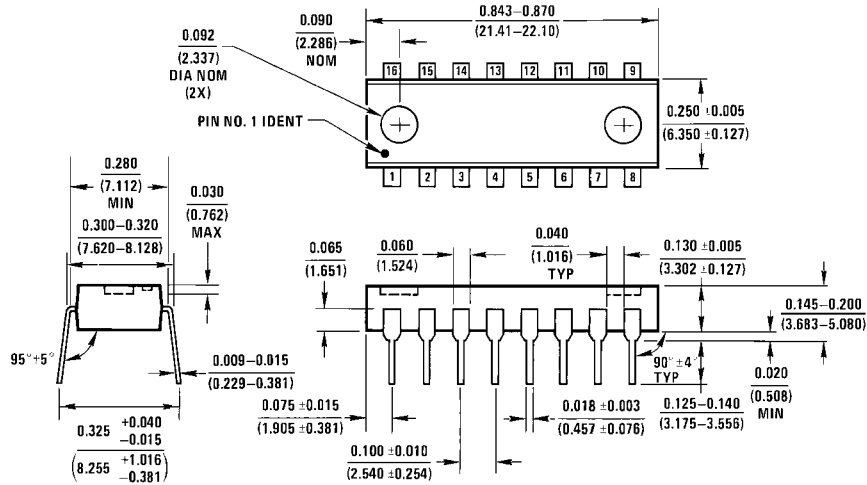


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Body Package Number M16A



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N16A (REV E)

16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com