

SN74ALB16244 16-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS

SCBS647D – AUGUST 1995 – REVISED JANUARY 2001

- Member of Texas Instruments' Widebus™ Family
- State-of-the-Art Advanced Low-Voltage BiCMOS (ALB) Technology Design for 3.3-V Operation
- Schottky Diodes on All Inputs to Eliminate Overshoot and Undershoot
- Industry Standard '16244 Pinout
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout

description

The SN74ALB16244 16-bit buffer and line driver is designed for high-speed, low-voltage (3.3-V) V_{CC} operation. This device is intended to replace the conventional driver in any speed-critical path. The small propagation delay is achieved using a unity-gain amplifier on the input and feedback resistors from input to output, which allows the output to track the input with a small offset voltage.

The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. This device provides true outputs and symmetrical active-low output-enable (\overline{OE}) inputs.

DGG, DGV, OR DL PACKAGE (TOP VIEW)

$\overline{1OE}$	1	48	$\overline{2OE}$
1Y1	2	47	1A1
1Y2	3	46	1A2
GND	4	45	GND
1Y3	5	44	1A3
1Y4	6	43	1A4
V _{CC}	7	42	V _{CC}
2Y1	8	41	2A1
2Y2	9	40	2A2
GND	10	39	GND
2Y3	11	38	2A3
2Y4	12	37	2A4
3Y1	13	36	3A1
3Y2	14	35	3A2
GND	15	34	GND
3Y3	16	33	3A3
3Y4	17	32	3A4
V _{CC}	18	31	V _{CC}
4Y1	19	30	4A1
4Y2	20	29	4A2
GND	21	28	GND
4Y3	22	27	4A3
4Y4	23	26	4A4
$\overline{4OE}$	24	25	$\overline{3OE}$

ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74ALB16244DL	ALB16244
		Tape and reel	SN74ALB16244DLR	
	TSSOP – DGG	Tape and reel	SN74ALB16244DGGR	ALB16244
	TVSOP – DGV	Tape and reel	SN74ALB16244DGVR	AV244

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z



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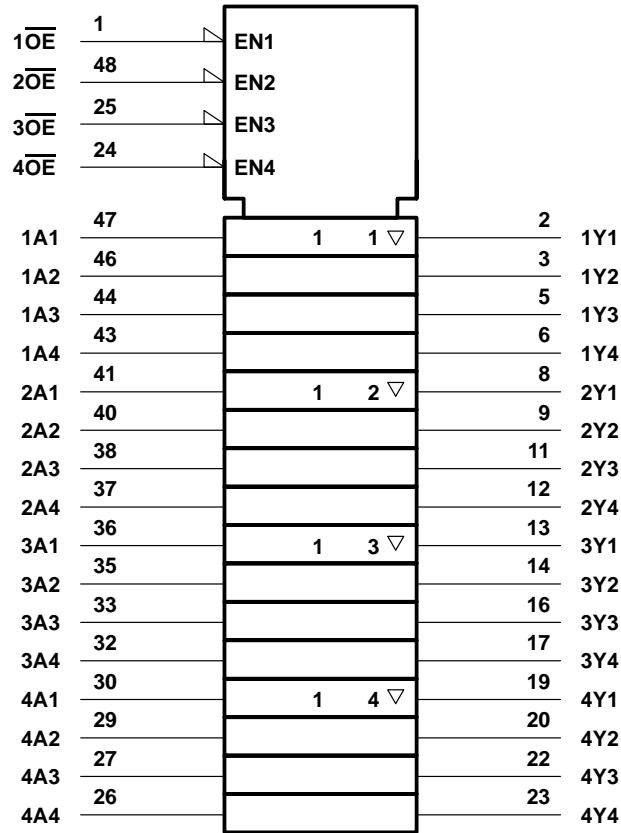
SN74ALB16244

16-BIT BUFFER/DRIVER

WITH 3-STATE OUTPUTS

SCBS647D – AUGUST 1995 – REVISED JANUARY 2001

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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16-BIT BUFFER/DRIVER

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recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	3.6	V
I_{OH}^{\dagger}	High-level output current		-25	mA
I_{OL}^{\dagger}	Low-level output current		25	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		5	ns/V
T_A	Operating free-air temperature	-40	85	°C

[†] See Figures 1 and 2 for typical I/O ranges.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [‡]	MAX	UNIT
V_{IK}	Data inputs	$V_{CC} = 3\text{ V}$	$I_I = 18\text{ mA}$	3.6	$V_{CC}-1.2$		V
			$I_I = -18\text{ mA}$	-0.9	-1.2		
I_I	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			±10	μA
	Data inputs	$V_{CC} = 3.6\text{ V}$	$V_I = V_{CC}$	\overline{OE} low	0.4	0.6	mA
				\overline{OE} high		25	μA
			$V_I = 0$	\overline{OE} low	-0.8	-1	mA
				\overline{OE} high		-60	μA
I_{OZH}	$V_{CC} = 3.6\text{ V}$,	$V_O = 3\text{ V}$	0.6	20	μA		
I_{OZL}	$V_{CC} = 3.6\text{ V}$,	$V_O = 0.5\text{ V}$	-0.1	-50	μA		
I_{CC}/buffer	$V_{CC} = 3.6\text{ V}$,	$I_O = 0$,	$V_I = V_{CC}$ or GND	3.7	5.6	mA	
I_{CCZ}	$V_{CC} = 3.6\text{ V}$,	Control inputs = V_{CC} or GND			0.8	mA	
ΔI_{CC}^{\S}	$V_{CC} = 3\text{ V}$ to 3.6 V , One input at $V_{CC} - 0.6\text{ V}$, Other inputs at V_{CC} or GND				600	μA	
C_i	$V_I = 3\text{ V}$ or 0			4.5		pF	
C_o	$V_O = 3\text{ V}$ or 0			5.5		pF	

[‡] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

switching characteristics over recommended operating free-air temperature range, $C_L = 50\text{ pF}$ (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			UNIT
			MIN	TYP [‡]	MAX	
t_{pd}	A	Y	0.6	1.3	2	ns
t_{en}	\overline{OE}	Y	1.3	2.5	4.7	ns
t_{dis}	\overline{OE}	Y	1.8	2.8	4.2	ns

[‡] All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^{\circ}\text{C}$.



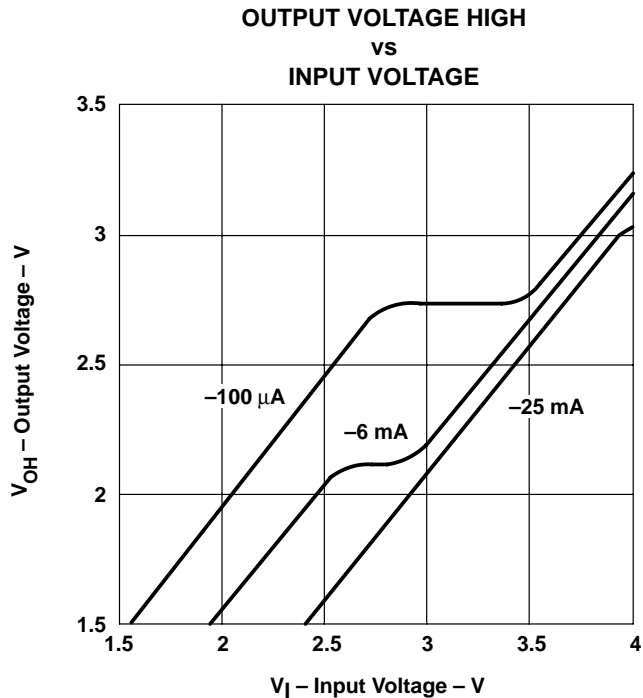


Figure 1. V_{OH} Over Recommended Free-Air Temperature Range

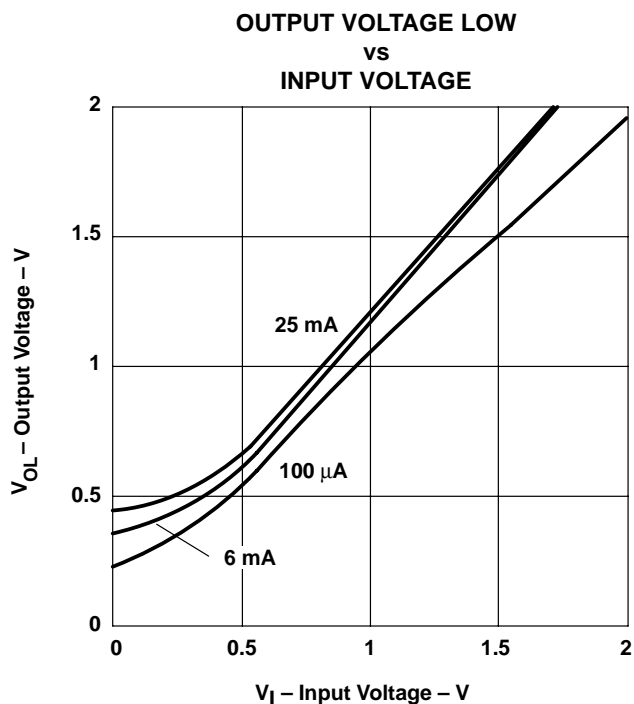
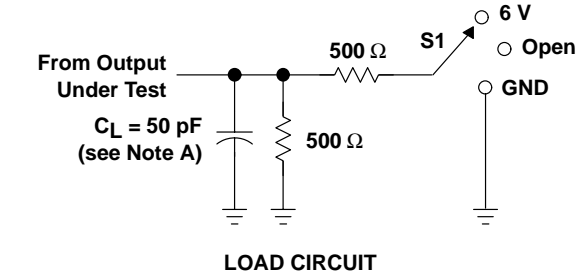


Figure 2. V_{OL} Over Recommended Free-Air Temperature Range

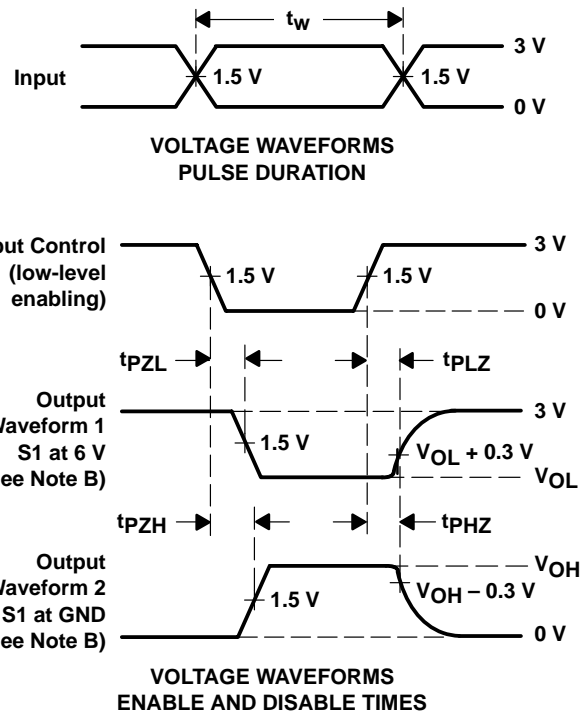
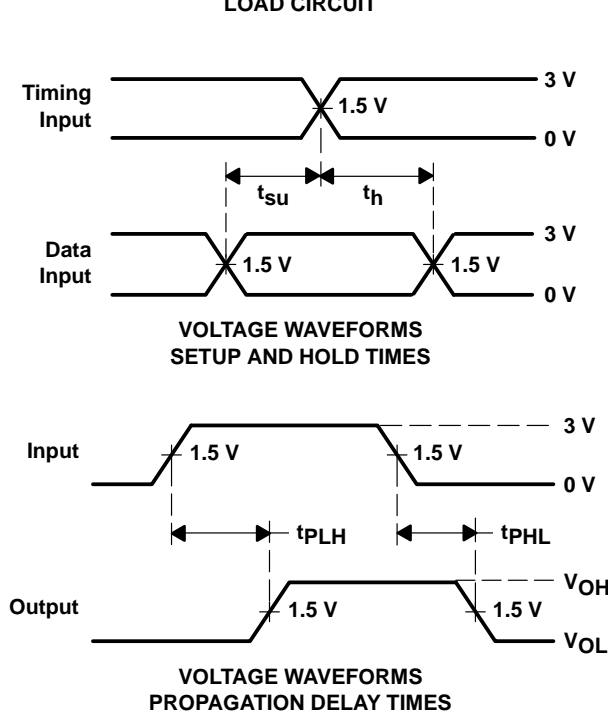
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PARAMETER MEASUREMENT INFORMATION



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ALB16244DGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALB16244	Samples
SN74ALB16244DL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALB16244	Samples
SN74ALB16244DLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ALB16244	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALB16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74ALB16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALB16244DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74ALB16244DLR	SSOP	DL	48	1000	367.0	367.0	55.0

TUBE

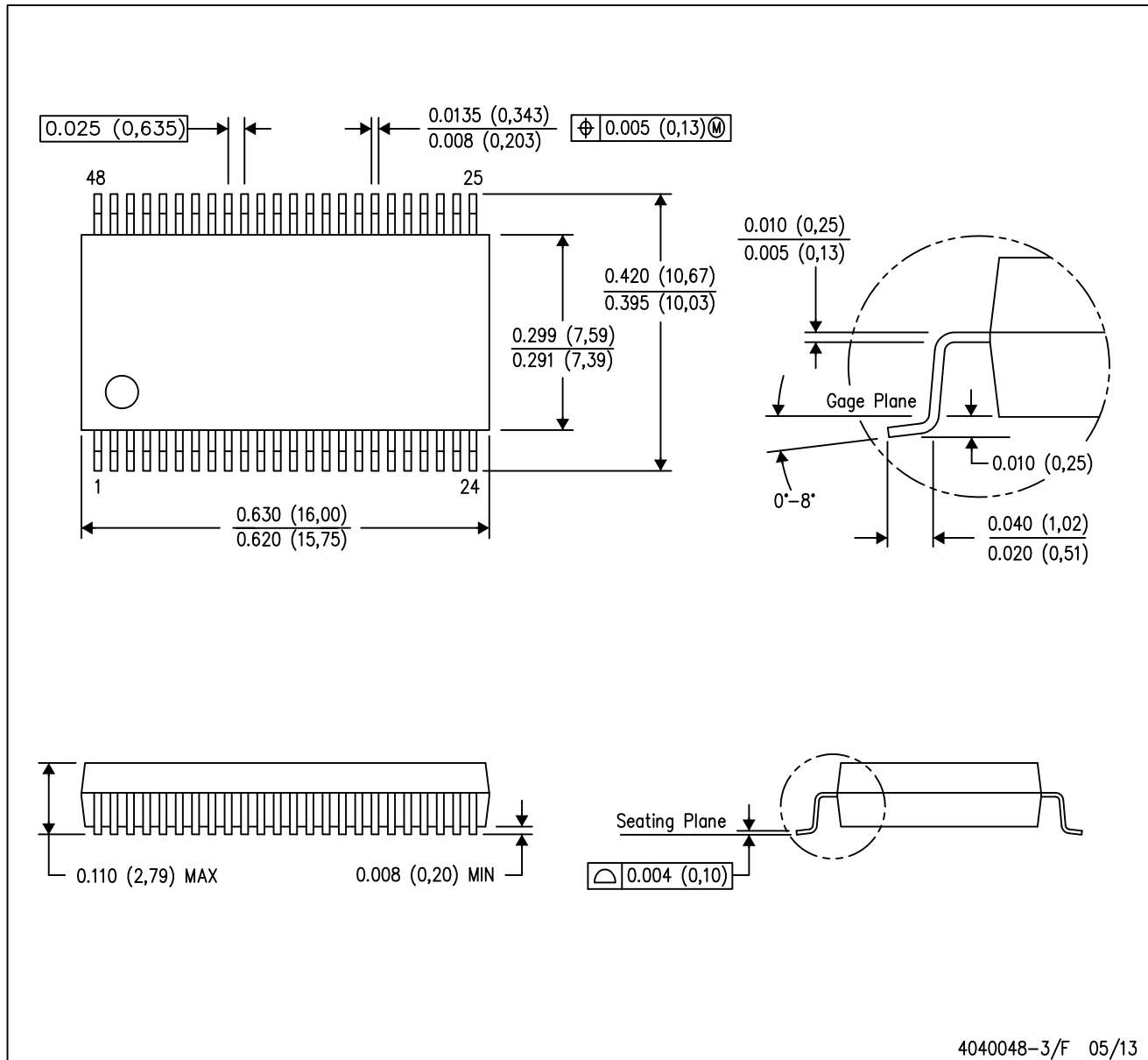

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALB16244DL	DL	SSOP	48	25	473.7	14.24	5110	7.87

MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118

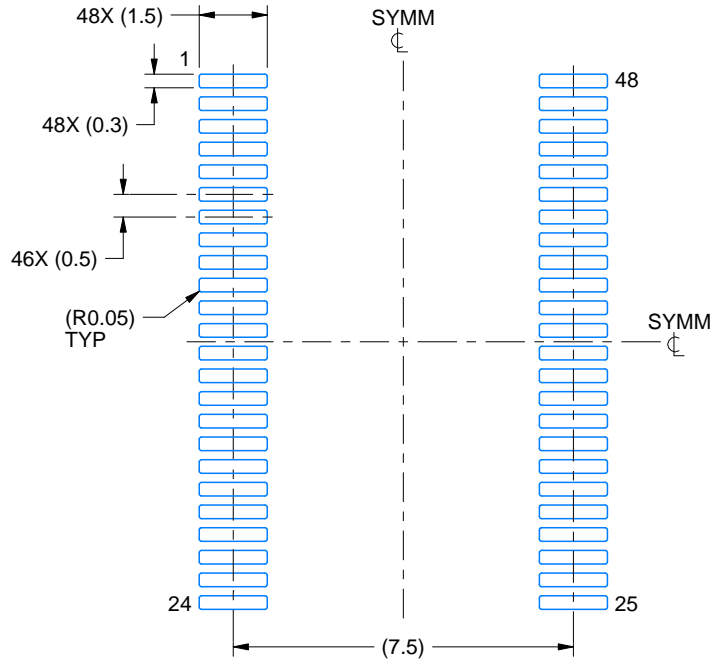
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EXAMPLE BOARD LAYOUT

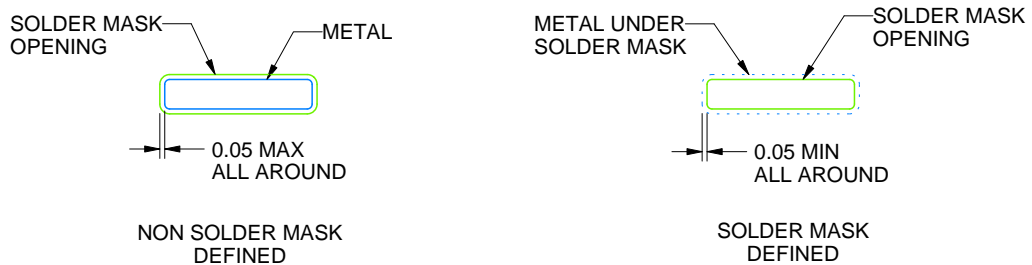
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

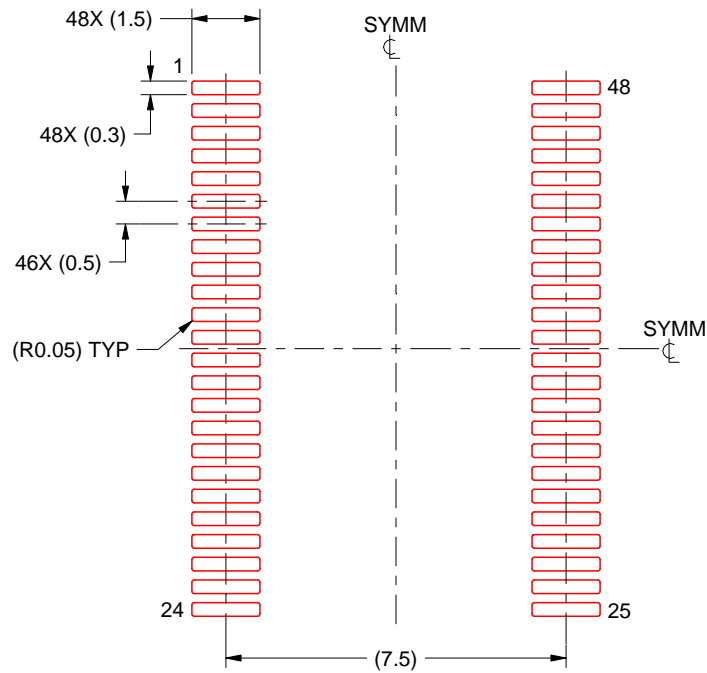
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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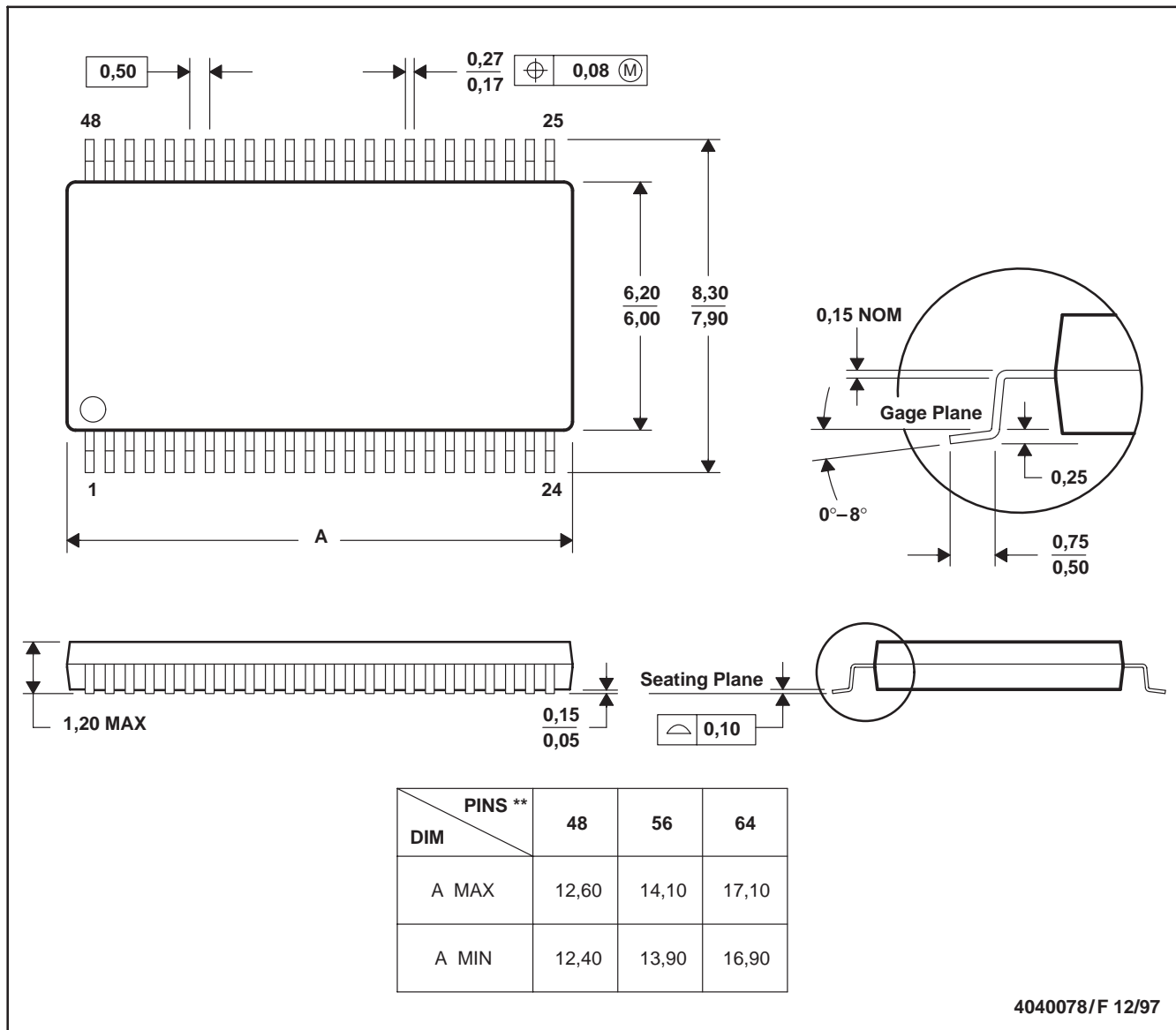
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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