National Semiconductor

DM74ALS174/DM74ALS175 Hex/Quad D Flip-Flop with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

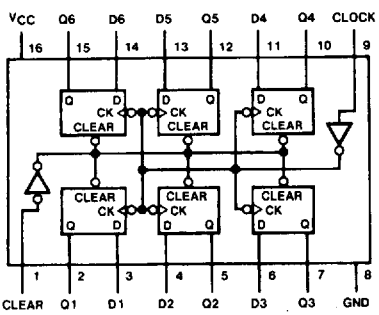
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- Advanced oxide-isolated ion-implanted Schottky TTL process
- Pin and functional compatible with LS family counterpart
- Typical clock frequency maximum is 80 MHz
- Switching performance guaranteed over full temperature and V_{CC} supply range

Connection Diagrams

Dual-In-Line Package



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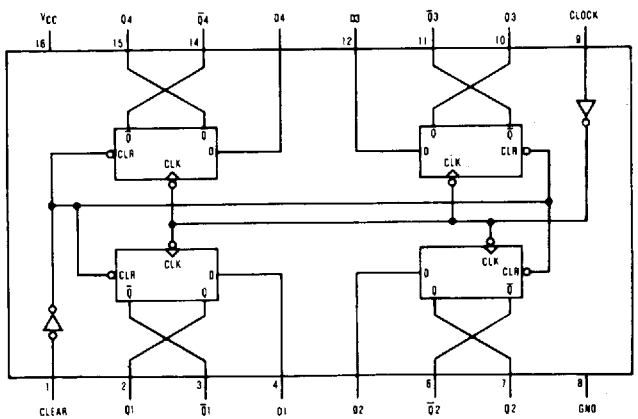
Order Number DM74ALS174M, DM74ALS174N or DM74ALS174SJ
See NS Package Number M16A, M16D or N16A

Dual-In-Line Package



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Function Table

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$***
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from Low to High Level
Q_0 = the level of Q before the indicated steady-state input conditions were established
*applies to 74ALS175 only

Order Number DM74ALS175M, DM74ALS175N or DM74ALS175SJ
See NS Package Number M16A, M16D or N16A

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM74ALS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Typical θ_{JA}	
N Package	77.9°C/W
M Package	107.3°C/W

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM74ALS174,175			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	V
V_{IH}	High Level Input Voltage		2			V
V_{IL}	Low Level Input Voltage				0.8	V
I_{OH}	High Level Output Current				−0.4	mA
I_{OL}	Low Level Output Current				8	mA
t_W	Pulse Width	Clock High or Low	10			ns
		$\overline{\text{Clear}}$ Low	10			
t_{SETUP}	Setup Time (Note 1)	Data Input	10↑			ns
		$\overline{\text{Clear}}$ Inactive State	6↑			
t_{HOLD}	Data Hold Time (Note 1)		0↑			ns
f_{CLOCK}	Clock Frequency		0		50	MHz
T_A	Free Air Operating Temperature		0		70	°C

Note 1: The symbol ↑ indicates that the rising edge of the clock is used as reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at V_{CC} = 5V, T_A = 25°C.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −400 μA, V_{CC} = 4.5V to 5.5V		V_{CC} − 2	V_{CC} − 1.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V	DM74 I_{OL} = 8 mA		0.35	0.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.1	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−112	mA
I_{CC}	Supply Current	V_{CC} = 5.5V, Clock = 4.5V, Clear = GND, D Input = GND	ALS174		11	19	mA
			ALS175		8	14	

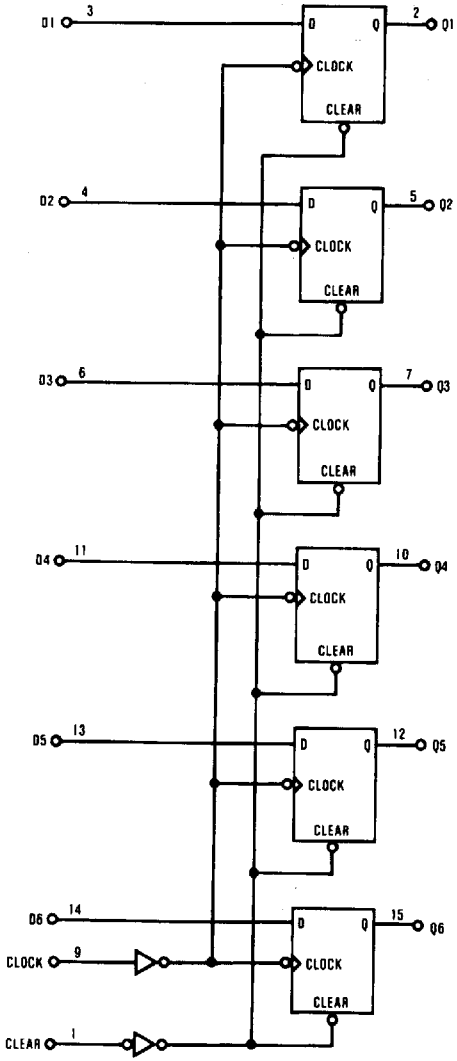
Switching Characteristics over recommended operating free air temperature range (Note 1)

Symbol	Parameter	Conditions	DM74ALS174, 175		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	$R_L = 500\Omega$ $C_L = 50$ pF $V_{CC} = 4.5V$ to $5.5V$	50		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output From Clear (175 Only)		5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output From Clear		8	23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output From Clock		3	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output From Clock		5	17	ns

Note 1: See Section 5 for test waveforms and output load.

Logic Diagrams

ALS174



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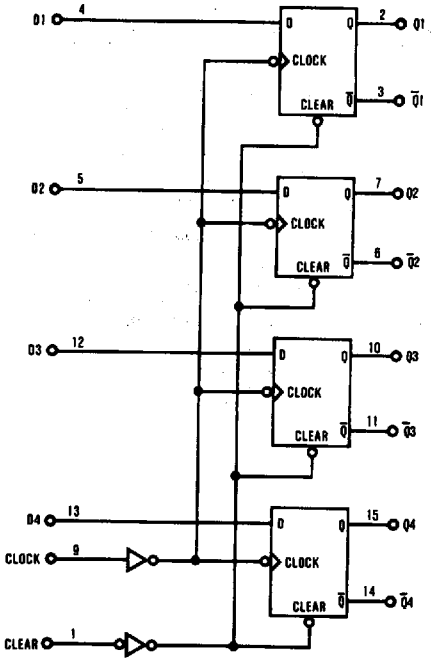
ALS175



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