11.3-GBPS DIFFERENTIAL VCSEL DRIVER

FEATURES

- **Up to 11.3-Gbps Operation**
- **Two-Wire Digital Interface**
- **Digitally Selectable Modulation Current up to 40 mA**
- **Digitally Selectable Bias Current up to 20 mA**
- **Automatic Power Control (APC) Loop**
- **Supports Transceiver Management System (TMS)**
- **Programmable Input Equalizer**
- **Includes Laser Safety Features**
- **Analog Temperature Sensor Output**
- **Single 3.3-V Supply**
- **Operating Temperature –40°C to 85°C**
- **Surface-Mount, Small-Footprint, 4-mm × 4-mm, 20-Pin QFN Package**

APPLICATIONS

- **10-Gigabit Ethernet Optical Transmitters**
- **8× and 10× Fibre Channel Optical Transmitters**
- **SONET OC-192/SDH STM-64 Optical Transmitters**
- **XFP and SFP+ Transceiver Modules**
- **XENPAK, XPAK, X2, and 300-Pin MSA Transponder Modules**

DESCRIPTION

The ONET1191V is a high-speed, 3.3-V laser driver designed to directly modulate VCSELs at data rates up to 11.3 Gbps.

The device provides a two-wire serial interface which allows digital control of the modulation and bias currents, eliminating the need for external components. An optional input equalizer can be used for equalization of up to 300 mm (12 inches) of microstrip or stripline transmission line on FR4 printed-circuit boards.

The ONET1191V includes an integrated automatic power control (APC) loop as well as circuitry to support laser safety and transceiver management systems.

The VCSEL driver is characterized for operation from –40°C to 85°C ambient temperatures and is available in a small-footprint, 4-mm × 4-mm, 20-pin QFN package.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

A simplified block diagram of the ONET1191V is shown in Figure 1.

The VCSEL driver consists of an equalizer, a high-speed current modulator, a modulation current generator, power-on reset circuitry, a two-wire interface and control logic block, a bias current generator and automatic power control loop, and an analog reference block.

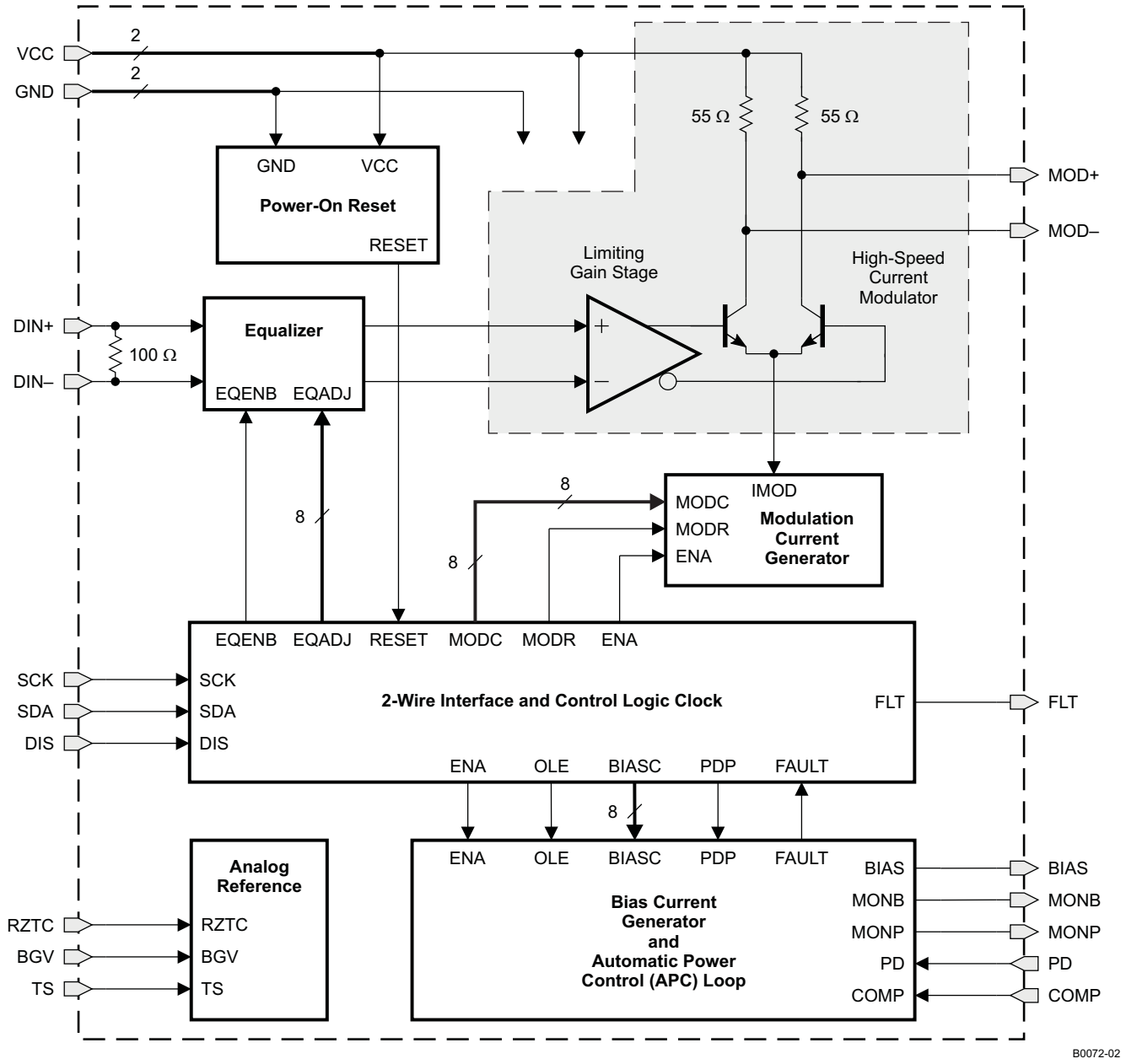

Figure 1. Simplified Block Diagram of the ONET1191V

EQUALIZER

The data signal can be applied to an input equalizer by means of the input signal pins DIN+/DIN–, which provide on-chip differential 100-Ω line termination. The equalizer is enabled by setting EQENB = 0 (bit 1 of register 0). Equalization of up to 300 mm (12 inches) of microstrip or stripline transmission line on FR4 printed circuit boards can be achieved. The amount of equalization is digitally controlled by the two-wire interface and control logic block and depends on the register settings EQADJ[0..7] (register 3). The equalizer can also be turned off and bypassed by setting EQENB = 1. For details about the equalizer settings, see Table 6.

HIGH-SPEED CURRENT MODULATOR

The output of the equalizer is applied to the high-speed current modulator. The limiting gain stage ensures sufficient drive amplitude and edge speed for driving the current modulator differential pair.

The modulation current is sunk from the common-emitter node of the named differential pair by means of a modulation current generator, which is digitally controlled by the two-wire interface and control logic block.

The collector nodes of the differential pair are connected to the output pins MOD+/MOD–, which include on-chip 2 × 55-Ω back-termination to VCC. The 55-Ω back-termination helps to suppress signal distortion caused by double reflections for VCSEL diodes with impedances from 50 Ω through 75 Ω.

MODULATION CURRENT GENERATOR

The modulation current generator provides the current for the current modulator described previously. The circuit is digitally controlled by the two-wire interface and control logic block.

An 8-bit-wide control bus, MODC, is used to set the desired modulation current. Furthermore, two modulation current ranges are selected by means of the MODR signal. The ENA signal enables or disables the modulation current generator.

The modulation current can be disabled by setting the DIS input pin to a high level. The modulation current is also disabled in a fault condition if the fault detection enable register flag FLTEN is set.

For more information about the register functionality, see the register mapping description in Table 6.

TWO-WIRE INTERFACE AND CONTROL LOGIC

The ONET1191V uses a two-wire serial interface for digital control. A simplified block diagram of this interface is shown in Figure 2. The two circuit inputs, SDA and SCK, are driven, respectively, by the serial data and serial clock from a microcontroller, for example. Both inputs include 100-kΩ pullup resistors to VCC. For driving these inputs, an open-drain output is recommended.

A write cycle consists of a START command, three address bits with MSB first, 8 data bits with MSB first, and a STOP command. In idle mode, both the SDA and SCK lines are at a high level.

A START command is initiated by the falling edge of SDA with SCK at a high level, transitioning to a low level.

Bits are clocked into an 11-bit-wide shift register during the high level of the serial clock, SCK.

A STOP command is detected on the rising edge of SDA after SCK has changed from a low to a high level.

At the time of detection of a STOP command, the eight data bits from the shift register are copied to a selected 8-bit register. Register selection occurs according to the three address bits in the shift register, which are decoded to eight independent select signals using an 3-to-8 decoder block.

In the ONET1191V, addresses 0 (000b) through 3 (011b) are used.

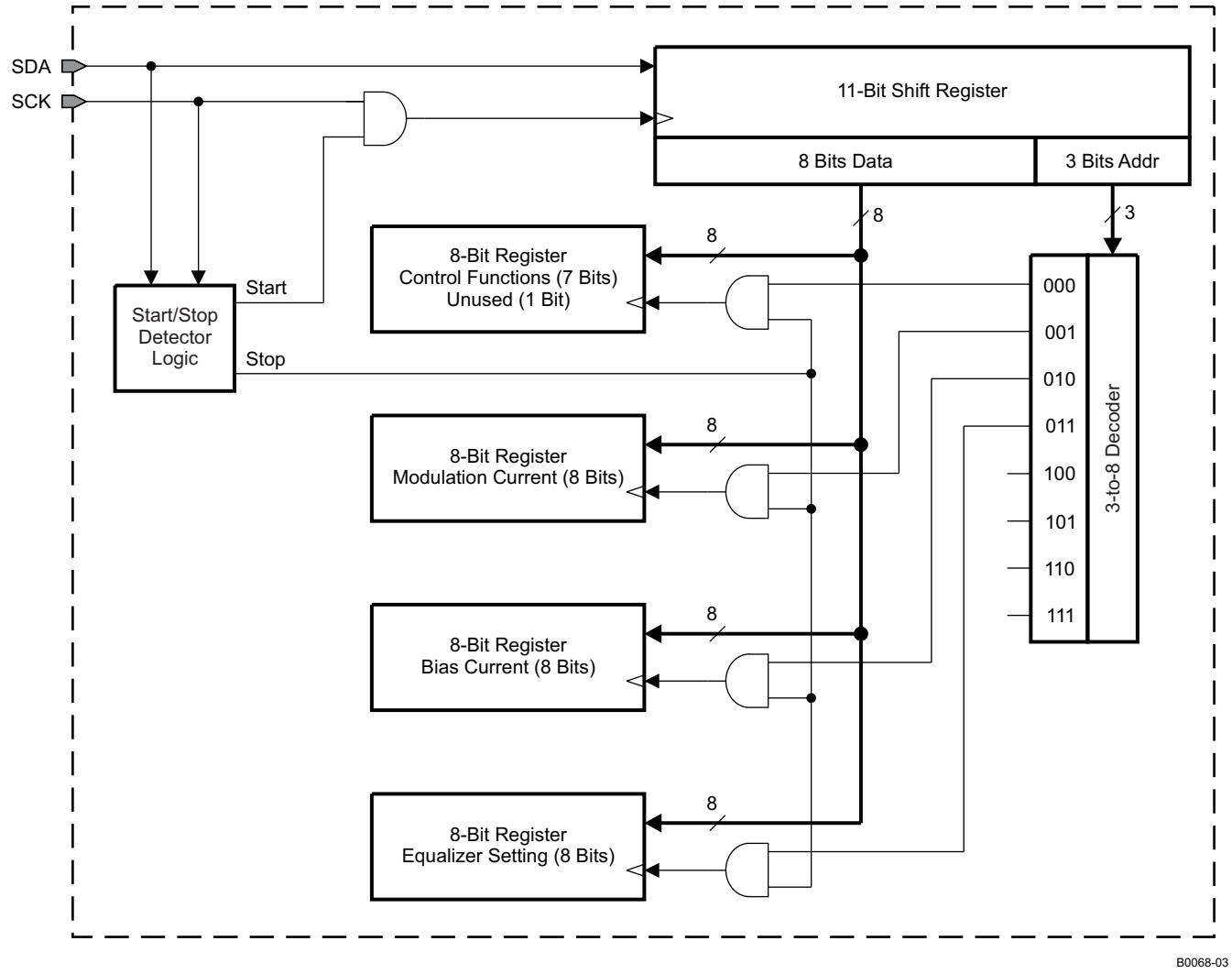

Figure 2. Simplified Two-Wire Interface Block Diagram

The timing definition for the serial data signal SDA and the serial clock signal SCK is shown in Figure 3. The corresponding timing requirements are listed in Table 1.

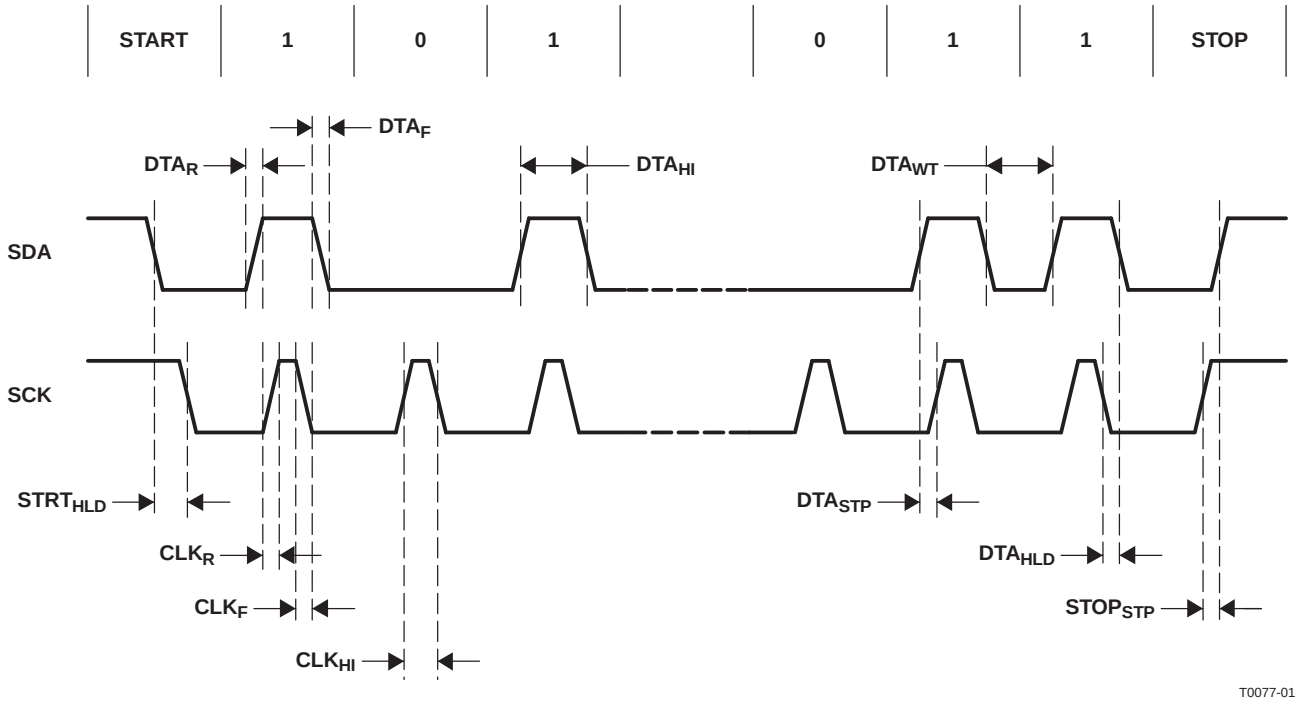

Figure 3. Two-Wire Interface Timing Diagram

Table 1. Two-Wire Interface Timing

PARAMETER		DESCRIPTION	MIN	MAX	UNIT
$STRT_{HLD}$	START hold time	Time required from data falling edge to clock falling edge at START	10		ns
CLK_R, DTA_R	Clock and data rise time	Clock and data rise time		10	ns
CLK_F, DTA_F	Clock and data fall time	Clock and data fall time		10	ns
CLK_{HI}	Clock high time	Minimum clock high period	50		ns
DTA_{HI}	Data high time	Minimum data high period	100		ns
DTA_{STP}	Data setup time	Minimum time from data rising edge to clock rising edge	10		ns
DTA_{WT}	Data wait time	Minimum time from data falling edge to data rising edge	50		ns
DTA_{HLD}	Data hold time	Minimum time from clock falling edge to data falling edge	10		ns
$STOP_{STP}$	STOP setup time	Minimum time from clock rising edge to data rising edge at STOP	10		ns

REGISTER MAPPING

The register mapping for the register addresses 0 (000b) through 3 (011b) are shown in Table 2 through Table 5. Table 6 describes the circuit functionality based on the register settings.

Table 2. Register 0 (000b) Mapping

address 0 (000b)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
ENA	PDP	PDR	OLE	FLTEN	MODR	EQENB	–

Table 3. Register 1 (001b) Mapping

address 1 (001b)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
MODC7	MODC6	MODC5	MODC4	MODC3	MODC2	MODC1	MODC0

Table 4. Register 2 (010b) Mapping

address 2 (010b)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
BIASC7	BIASC6	BIASC5	BIASC4	BIASC3	BIASC2	BIASC1	BIASC0

Table 5. Register 3 (011b) Mapping

address 3 (011b)							
bit 7	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
EQADJ7	EQADJ6	EQADJ5	EQADJ4	EQADJ3	EQADJ2	EQADJ1	EQADJ0

Table 6. Register Functionality

SYMBOL	REGISTER	FUNCTION
ENA	Enable	Enables chip when set to 1. Can be toggled low to reset a fault condition.
PDP	Photodiode polarity	Photodiode polarity bit: 1 = photodiode cathode connected to V_{CC} 0 = photodiode anode connected to GND
PDR	Photodiode current range	Photodiode current range bit: With coupling ratio CR between VCSEL bias current and photodiode current = 30 1 = 12 µA–640 µA with 2.5 µA resolution 0 = 2.5 µA–12 8µA with 0.5µA resolution
OLE	Open loop enable	Open-loop enable bit: 1 = open-loop bias current control 0 = closed-loop bias current control
FLTEN	Fault detection enable	Fault detection enable bit: 1 = fault detection on 0 = fault detection off
MODR	Modulation tail current range	Laser modulation tail current range: 1 = 0 mA–40 mA 0 = 0 mA–20 mA
EQENB	Equalizer enable	Equalizer enable bit 1 = equalizer disabled 0 = equalizer enabled
MODC7	Modulation current bit 7 (MSB)	Modulation current setting:
MODC6	Modulation current bit 6	
MODC5	Modulation current bit 5	MODR = 1:
MODC4	Modulation current bit 4	Modulation current up to 40 mA in 156-µA steps
MODC3	Modulation current bit 3	
MODC2	Modulation current bit 2	MODR = 0:
MODC1	Modulation current bit 1	Modulation current up to 20 mA in 78-µA steps
MODC0	Modulation current bit 0 (LSB)	
BIASC7	Bias current bit 7 (MSB)	**Closed loop (APC):**
BIASC6	Bias current bit 6	Coupling ratio CR = $I_{BIAS-VCSEL}/I_{PD}$
BIASC5	Bias current bit 5	PDR = 0, BIASC = 0..255, $I_{BIAS-VCSEL} \leq 20$ mA:
BIASC4	Bias current bit 4	$I_{BIAS-VCSEL} = 0.5\ \mu A \times CR \times BIASC$
BIASC3	Bias current bit 3	PDR = 1, BIASC = 0..255, $I_{BIAS-VCSEL} \leq 20$ mA:
BIASC2	Bias current bit 2	$I_{BIAS-VCSEL} = 2.5\ \mu A \times CR \times BIASC$
BIASC1	Bias current bit 1	
BIASC0	Bias current bit 0 (LSB)	**Open loop:** $I_{BIAS-VCSEL} = 75\ \mu A \times BIASC$
EQADJ7	Equalizer adjustment bit 7 (MSB)	**Equalizer adjustment setting**
EQADJ6	Equalizer adjustment bit 6	
EQADJ5	Equalizer adjustment bit 5	EQENB = 1
EQADJ4	Equalizer adjustment bit 4	Equalizer is turned off and bypassed
EQADJ3	Equalizer adjustment bit 3	

Table 6. Register Functionality (continued)

SYMBOL	REGISTER	FUNCTION
EQADJ2	Equalizer adjustment bit 2	EQENB = 0
EQADJ1	Equalizer adjustment bit 1	Maximum equalization for 0000 0000
EQADJ0	Equalizer adjustment bit 0 (LSB)	Minimum equalization for 1111 1111

BIAS CURRENT GENERATION AND APC LOOP

The bias current generation and APC loop are controlled by means of the two-wire interface. In open-loop operation, selected by setting OLE = 1 (bit 4 of register 0), the bias current is set directly by the 8-bit-wide control word BIASC[0..7] (register 2). In automatic power control mode, selected by setting OLE = 0, the bias current depends on the register settings BIASC[0..7] and the coupling ratio (CR) between the VCSEL bias current and the photodiode current. CR = $I_{BIAS-VCSEL}/I_{PD}$.

Two photodiode current ranges can be selected by means of the PDR register (bit 5 of register 0). The photodiode range should be chosen to keep the laser bias control DAC close to the center of its range. This keeps the laser bias current setpoint resolution high and the loop settling time constant within specification.

For details regarding the bias current setting in open- as well as in closed-loop mode, see Table 6.

In closed-loop mode, the photodiode polarity bit, PDP, must be set for common-anode or common-cathode configuration to ensure proper operation. In open-loop mode, if a photodiode is present, the photodiode polarity bit must be set to the opposite setting.

ANALOG REFERENCE

The ONET1191V VCSEL driver is supplied by a single 3.3-V ±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

On-chip bandgap voltage circuitry generates a reference voltage, independent of the supply voltage, from which all other internally required voltages and bias currents are derived.

An external zero-temperature-coefficient resistor must be connected from the RZTC pin of the device to ground (GND). This resistor is used to generate a precise, zero-TC current, which is required as a reference current for the on-chip DACs.

In order to minimize the module component count, the ONET1191V provides an on-chip temperature sensor. The output voltage of the temperature sensor is available at the TS pin.

The voltage is V_{TS} = (8.2 mV/°C × TEMP) + 1140 mV, with TEMP given in °C.

Note that the voltage at TS is not buffered. As a result, TS can only drive capacitive loads.

POWER-ON RESET AND REGISTER LOADING SEQUENCE

The ONET1191V has power-on-reset circuitry, which ensures that all registers are reset to zero during startup. After the power-on to initialize time (t_{INIT1}), the internal registers are ready to be loaded. It is important that the registers are loaded in the following order:

1. Bias current register (register 2, 010b)
2. Modulation current register (register 1, 001b)
3. Control register (register 0, 000b)
4. Loading of equalizer register (register 3, 011b) is not required.

The part is ready to transmit data after the initialize to transmit time t_{INIT2}, assuming that the control register enable bit ENA is set to 1 and the disable pin DIS is low.

The ONET1191V can be disabled using either the ENA control register bit or the disable pin DIS. In both cases, the internal registers are not reset. After the disable pin DIS is set low and/or the enable bit ENA is set back to 1, the part returns to its prior output settings.

LASER SAFETY FEATURES AND FAULT RECOVERY PROCEDURE

The ONET1191V provides built-in laser safety features. The following fault conditions are detected:

- Voltage at MONB exceeds the voltage at RZTC (1.15V).
- Photodiode current exceeds 150% of its set value.
- Bias control DAC drops in value by more than 50% in one step.

If one or more fault conditions occur and the fault enable bit FLTEN is set to 1, the ONET1191V responds by:

- Setting the VCSEL bias current to zero
- Setting the modulation current to zero
- Asserting and latching the FLT pin

Fault recovery is performed by the following procedure:

1. The disable pin DIS and/or the enable control bit ENA are toggled for at least the fault latch reset time t_{RESET}.
2. The FLT pin deasserts while the disable pin DIS is asserted or the enable bit ENA is deasserted.
3. If the fault condition is no longer present, the part returns to normal operation with its prior output settings after the disable negate time t_{ON}.
4. If the fault condition is still present, FLT reasserts once DIS is set to a low level, and the part does not return to normal operation.

PACKAGE

The ONET1191V is packaged in a small-footprint, 4-mm × 4-mm, 20-pin QFN package with a lead pitch of 0,5 mm. The pinout is shown in Figure 4.

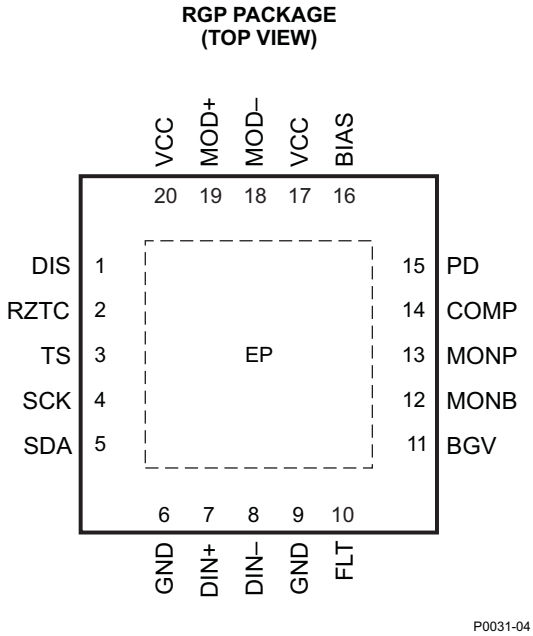

Figure 4. Pinout of ONET1191V in a 4-mm × 4-mm, 20-Pin QFN Package

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
BGV	11	Anolog-out	Buffered bandgap voltage with open emitter output. This is a replica of the bandgap voltage at RZTC. For best matching, use the same 28.7-kΩ resistor to GND as used at RZTC.
BIAS	16	Analog	Sinks average bias current for VCSEL in both APC and open-loop modes. Connect to laser cathode through an inductor. BLM15HG102SN1D recommended.
COMP	14	Analog	Compensation pin used to control the bandwidth of the APC loop. Connect a 0.01-µF capacitor to ground.
DIN+	7	Analog-in	Noninverted data input. On-chip differentially 100-Ω terminated to DIN–. Must be ac-coupled.
DIN–	8	Analog-in	Inverted data input. On-chip differentially 100-Ω terminated to DIN+. Must be ac-coupled.
DIS	1	Digital-in	Disables both bias and modulation currents when set to high state. Toggle to reset a fault condition.
FLT	10	Digital-out	Fault detection flag.
GND	6, 9, EP	Supply	Circuit ground. Exposed die pad (EP) must be grounded.
MOD+	19	CML-out	Noninverted modulation current output. On-chip, 55-Ω back-terminated to VCC.
MOD–	18	CML-out	Inverted modulation current output. On-chip, 55-Ω back-terminated to VCC.
MONB	12	Analog-out	Bias current monitor. Sources a 3.3% replica of the bias current. Connect an external resistor to ground (GND). If the voltage at this pin exceeds 1.15 V, a fault is triggered. Typically, choose a resistor to give MONB voltage of 0.8 V at the maximum desired bias current.
MONP	13	Analog-out	Photodiode current monitor. Sources a 50% replica of the photodiode current when PDR = 1 and a 250% replica when PDR = 0. Connect an external resistor (5 kΩ typical) to ground (GND).
PD	15	Analog	Photodiode input. Pin can source or sink current dependent on PDP register setting. PDP = 0: source; PDP = 1: sink. Pin supplies >1.5-V reverse bias.
RZTC	2	Analog	Connect external zero-TC, 28.7-kΩ resistor to ground (GND). Used to generate a defined zero-TC reference current for internal DACs.
SCK	4	Digital-in	Two-wire interface serial clock. Includes a 100-kΩ pullup resistor to VCC.
SDA	5	Digital-in	Two-wire interface serial data input. Includes a 100-kΩ pullup resistor to VCC.
TS	3	Analog-out	Temperature sensor output. Not buffered, capacitive load only.
VCC	17, 20	Supply	3.3-V ±10% supply voltage

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC}	Supply voltage(2)	–0.3 to 4	V
V_{DIS}, V_{RZTC}, V_{TS}, V_{SCK}, V_{SDA}, V_{DIN+}, $V_{DIN–}$, V_{FLT}, V_{BGV}, V_{MONB}, V_{MONP}, V_{CAPC}, V_{PD}, V_{BIAS}, V_{MOD+}, $V_{MOD–}$	Voltage at DIS, RZTC, TS, SCK, SDA, DIN+, DIN–, FLT, BGV, MONB, MONP, CAPC, PD, BIAS, MOD+, MOD–(2)	–0.3 to 4	V
ESD	ESD rating at all pins	2	kV (HBM)
$T_{J,max}$	Maximum junction temperature	125	°C
T_{stg}	Storage temperature range	–65 to 85	°C
T_A	Characterized free-air operating temperature range	–40 to 85	°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		2.9	3.3	3.6	V
V_{IH}	Digital input high voltage	DIS, SCK, SDA	2			V
V_{IL}	Digital input low voltage	DIS, SCK, SDA			0.8	V
	Bias output headroom voltage	V_{BIAS} – GND	300			mV
	Photodiode current range	Control bit PDR = 1, step size = 2.5 µA	12		640	µA
		Control bit PDR = 0 step size = 0.5 µA	2.5		128	
R_{RZTC}	Zero-TC resistor value(1)	1.15-V bandgap bias across resistor	28.4	28.7	29	kΩ
V_{IN}	Differential input voltage swing	Control bit EQENA = 1	200		1200	mVp-p
		Control bit EQENA = 0	500		1200	
t_{R-IN}	Input rise time	20%–80%		30	55	ps
t_{F-IN}	Input fall time	20%–80%		30	55	ps
T_A	Operating free-air temperature		–40		85	° C

(1) Changing the value alters the DAC ranges.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions; all values are for open-loop operation, I_{MODC} = 12 mA, I_{BIASC} = 6 mA, and R_{RZTC} = 28.7 kΩ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.9	3.3	3.6	V
I_{VCC}	Supply current	I_{MODC} = 24mA, I_{BIASC} = 6 mA, including I_{MODC} and I_{BIASC}, EQENB = 1		62	71	mA
		I_{MODC} = 24mA, I_{BIASC} = 6mA, including I_{MODC} and I_{BIASC}, EQENB = 0		70		
		Disabled, DIS = high and/or control bit ENA = low, EQENB = 1		35	42	
R_{IN}	Data input resistance	Differential between DIN+/DIN–	85	100	125	Ω
R_{OUT}	Data output resistance	Single-ended to V_{CC}	45	55	65	Ω
	Digital input current	SCK, SDA, 100-kΩ pullup to V_{CC} (1)	–50		10	µA
		DIS (1)	–10		10	µA
V_{OH}	Digital output high voltage	FLT, I_{SOURCE} = 500 µA	2.4			V
V_{OL}	Digital output low voltage	FLT, I_{SINK} = 500 µA			0.4	V
$I_{BIAS-DIS}$	Bias current during disable				100	µA
$I_{BIAS-MIN}$	Minimum bias current	See (2)			0.2	mA
$I_{BIAS-MAX}$	Maximum bias current	DAC set to maximum, open- and closed-loop	14	20		mA
V_{PD}	Photodiode reverse bias voltage	APC active, I_{PD} = max	1.5	2.3		V
	Photodiode fault current level, percent of target I_{PD} (1)			150%		
V_{TS}	Temperature sensor voltage range	–40°C to 120°C junction temperature, capacitive load only, with midscale calibration. (1)	0.5		2.5	V
	Temperature sensor accuracy	With midscale calibration (1)		±3		°C
I_{TS}	Temperature sensor drive current	Source or sink (1)	–1		1	µA
	Photodiode current monitor ratio	I_{MONP}/I_{PD} with control bit PDR = 1	40%	50%	60%	
		I_{MONP}/I_{PD} with control bit PDR = 0	200%	265%	300%	
	Bias current monitor ratio	I_{MONB}/I_{BIAS} (nominal 1/30 = 3.3%). 1.2-kΩ sense resistor	2.7%	3.3%	4%	
V_{CC-RST}	V_{CC} reset threshold voltage	V_{CC} voltage level which triggers power-on reset (1)	2.4	2.5	2.8	V
$V_{CC-RSTHYS}$	V_{CC} reset threshold voltage hysteresis			100 (1)		mV
$V_{MONB-FLT}$	Fault voltage at MONB	Fault occurs if voltage at MONB exceeds value	1.05	1.15	1.25	V

(1) Assured by simulation over process, supply, and temperature variation
(2) The bias current can be set below the specified minimum according to the corresponding register setting described in the register mapping section. However, in closed-loop operation, settings below the specified value may trigger a fault.

AC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions with 50-Ω output load, open-loop operation, I_{MODC} = 12 mA, I_{BIASC} = 6 mA, and R_{RZTC} = 28.7 kΩ, unless otherwise noted. Typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{r\text{-}OUT}$	Output rise time	20%–80%, $t_{r\text{-}IN}$ < 40 ps, 50-Ω load		20	30	ps
$t_{f\text{-}OUT}$	Output fall time	20%–80%, $t_{f\text{-}IN}$ < 40 ps, 50-Ω load		25	30	ps
$I_{MOD\text{-}MAX}$	Maximum modulation current	Control bit MODR = 1, 50-Ω load	36	45		mA
		Control bit MODR = 0, 50-Ω load	18	27		
$I_{MOD\text{-}STEP}$	Modulation current step size	Control bit MODR = 1, 50-Ω load		175		µA
		Control bit MODR = 0, 50-Ω load		100		
DJ	Deterministic output jitter	Control bit EQENB = 1, K28.5 pattern at 11.3 Gbps		4	12	$ps_{p\text{-}p}$
		Control bit EQENB = 0, K28.5 pattern at 11.3 Gbps, maximum equalization with 300-mm FR4 trace		10	20	
RJ	Random output jitter	50-Ω load		0.5	0.8	ps_{RMS}
τ_{APC}	APC time constant	C_{APC} = 0.01 µF, I_{PD} = 100 µA, PD coupling ratio CR = 40 (1)		200		µs
t_{OFF}	Transmitter disable time	Rising edge of DIS to $I_{BIAS} \le 0.1 \times I_{BIAS\text{-}NOMINAL}$ (1)		1	5	µs
t_{ON}	Disable negate time	Falling edge of DIS to $I_{BIAS} \ge 0.9 \times I_{BIAS\text{-}NOMINAL}$ (1)			1	ms
t_{INIT1}	Power-on to initialize	Power-on to registers ready to be loaded		1	10	ms
t_{INIT2}	Initialize to transmit	Register load STOP command to part ready to transmit valid data (1)			2	ms
t_{RESET}	DIS pulse duration	Time DIS must held high to reset part (1)	100			ns
t_{FAULT}	Fault assert time	Time from fault condition to FLT high (1)			50	µs

(1) Assured by simulation over process, supply, and temperature variation

TYPICAL CHARACTERISTICS

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, MODR = 0 (unless otherwise noted).

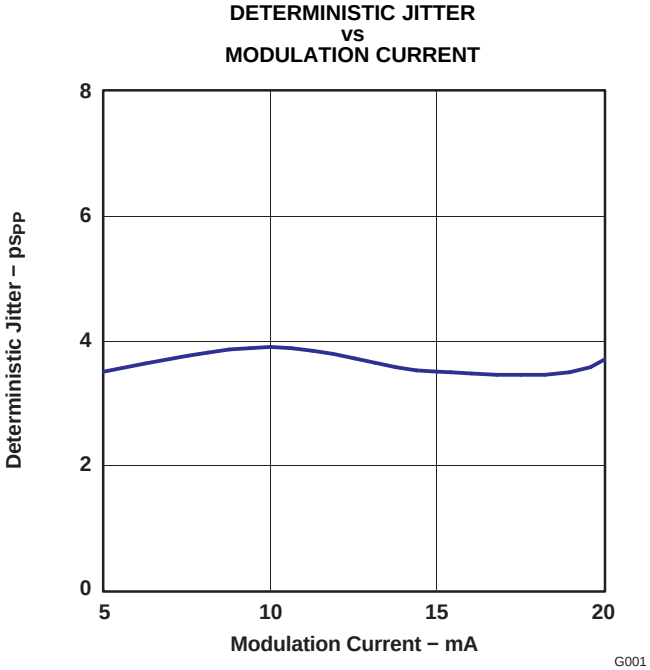

Figure 5.

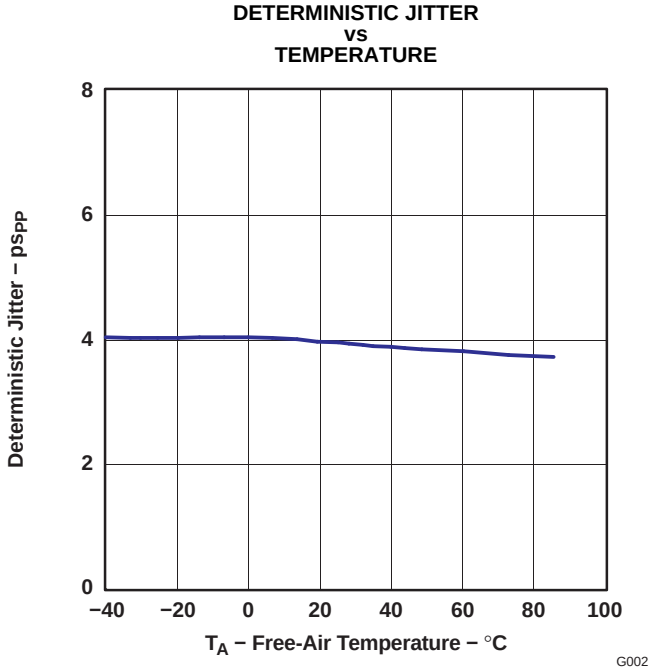

Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, MODR = 0 (unless otherwise noted).

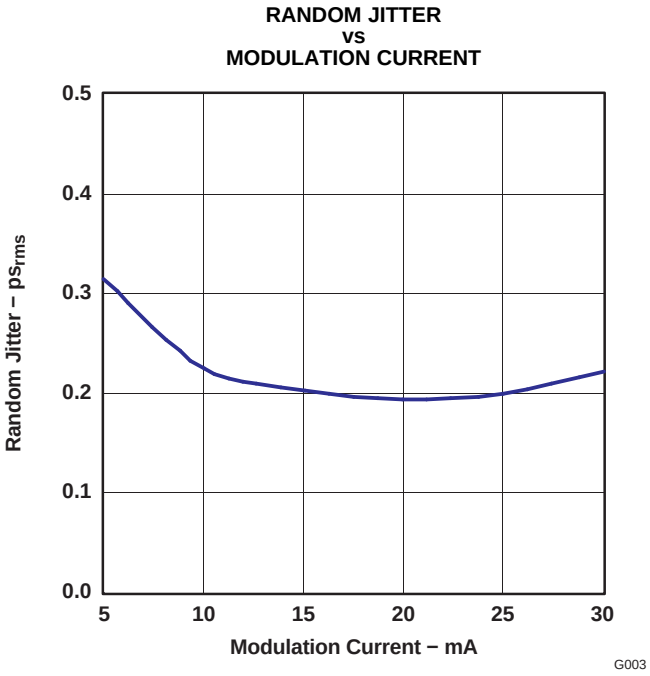

Figure 7.

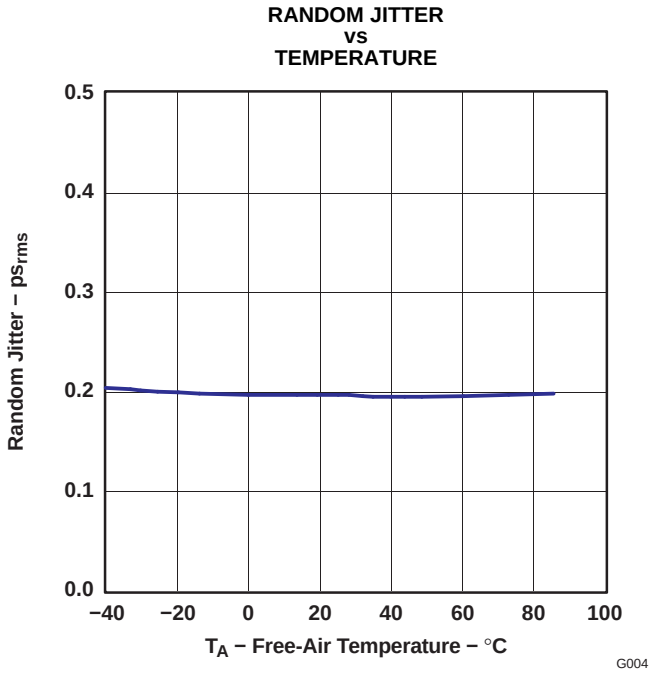

Figure 8.

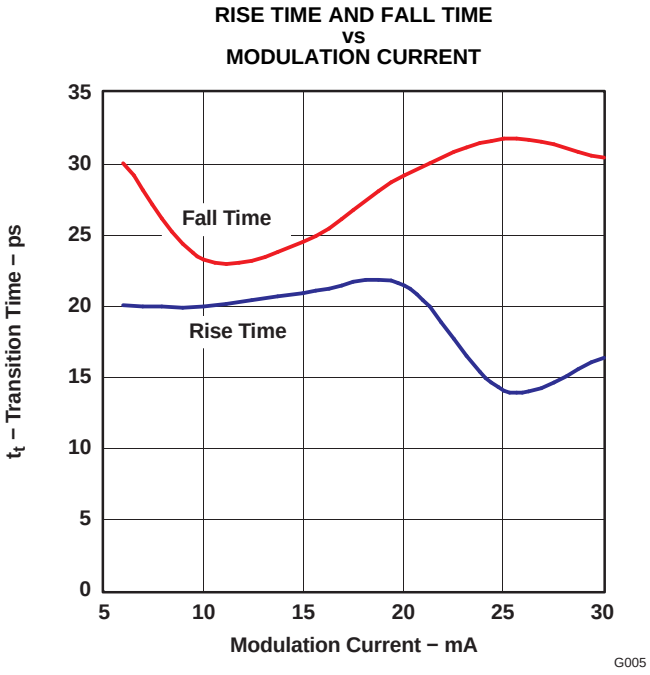

Figure 9.

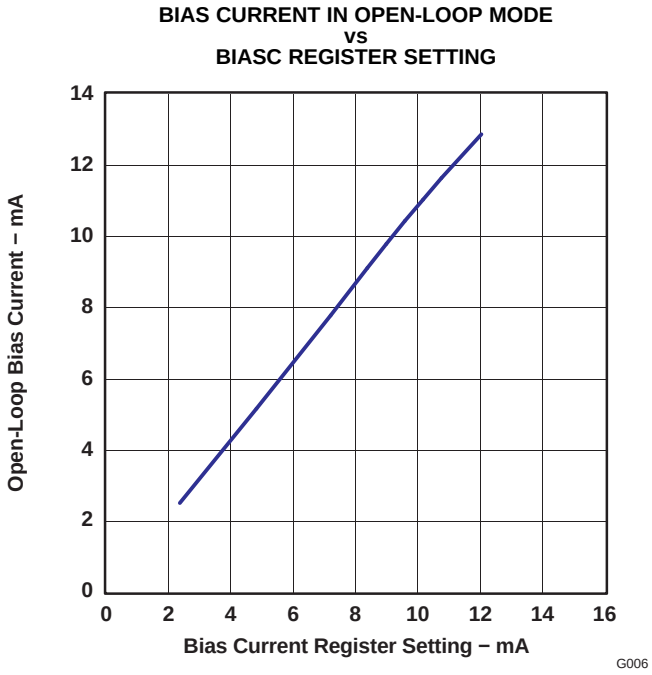

Figure 10.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, MODR = 0 (unless otherwise noted).

BIAS-MONITOR CURRENT I_{MONB} vs BIAS CURRENT

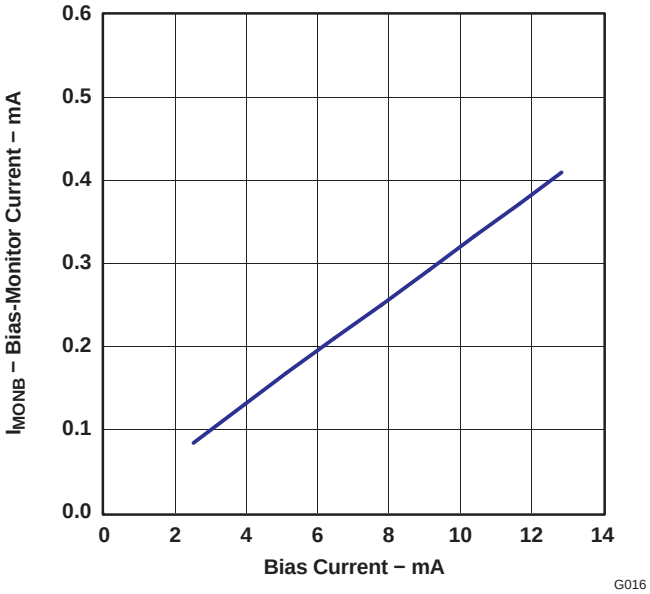

Figure 11.

MODULATION CURRENT vs MODC REGISTER SETTING, MODR = 1

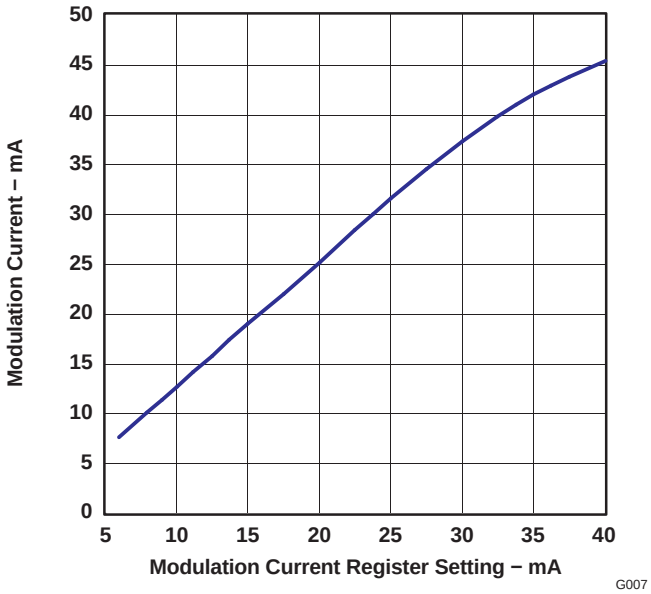

Figure 12.

SUPPLY CURRENT vs TEMPERATURE

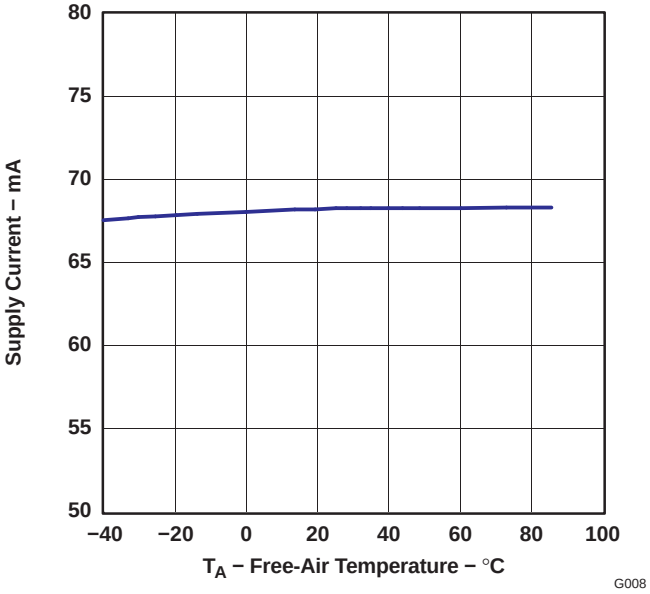

Figure 13.

EYE DIAGRAM AT 11.3 GBPS

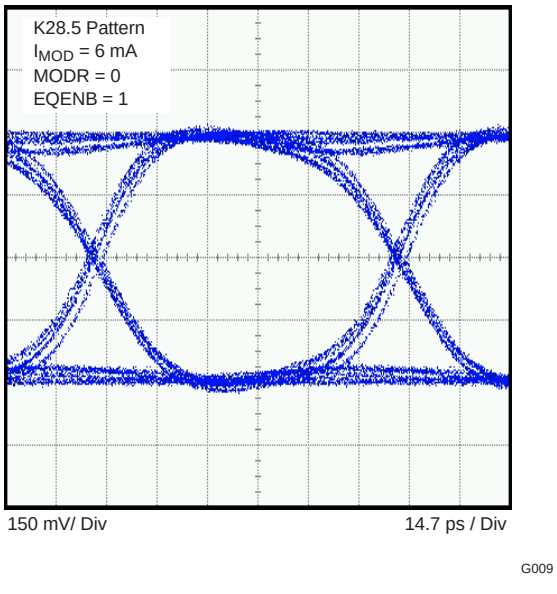

Figure 14.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, MODR = 0 (unless otherwise noted).

EYE DIAGRAM AT 11.3 GBPS

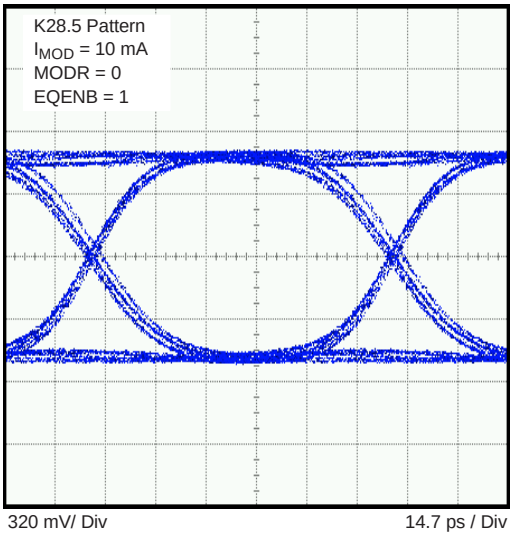

Figure 15.

EYE DIAGRAM AT 11.3 GBPS

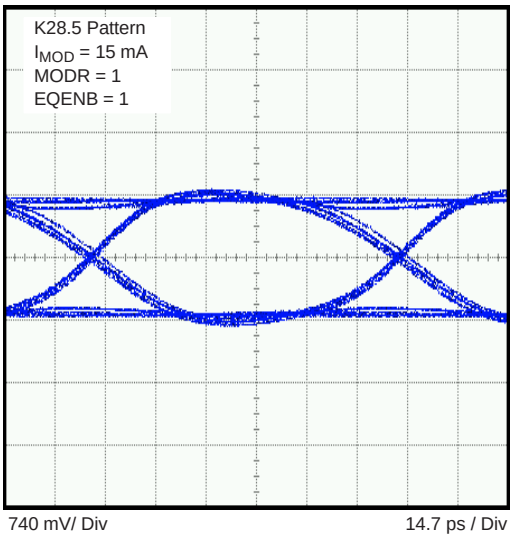

Figure 16.

EYE DIAGRAM AT 8.5 GBPS

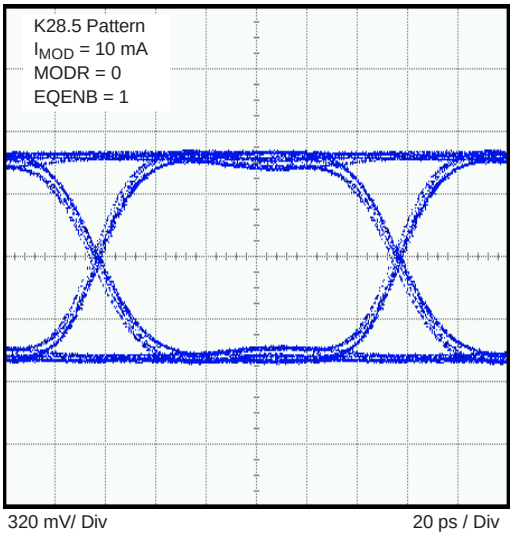

Figure 17.

EYE DIAGRAM AT 11.3 GBPS 12" OF FR4 AT INPUTS

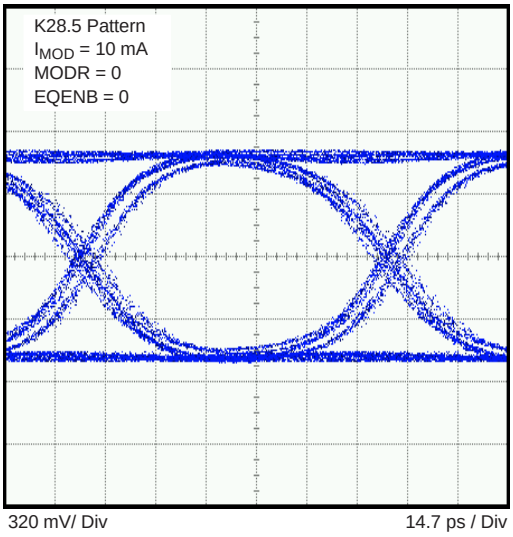

Figure 18.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C, I_{BIASC} = 6 mA, I_{MODC} = 12 mA, MODR = 0 (unless otherwise noted).

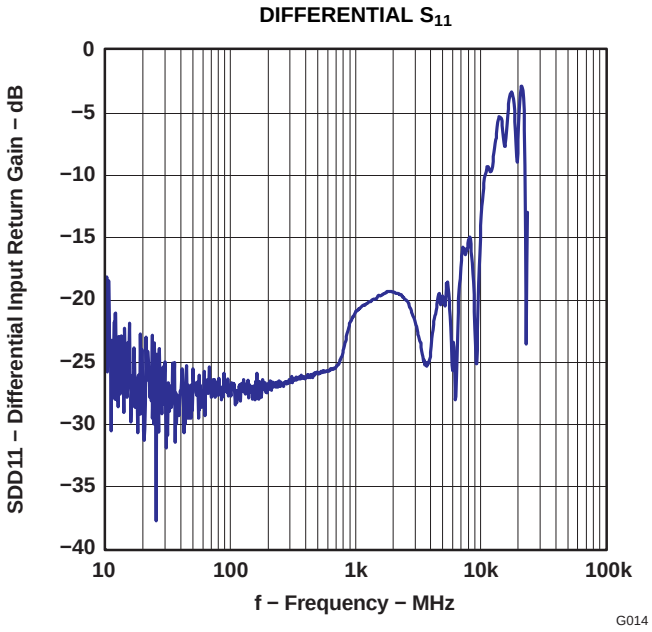

Figure 19.

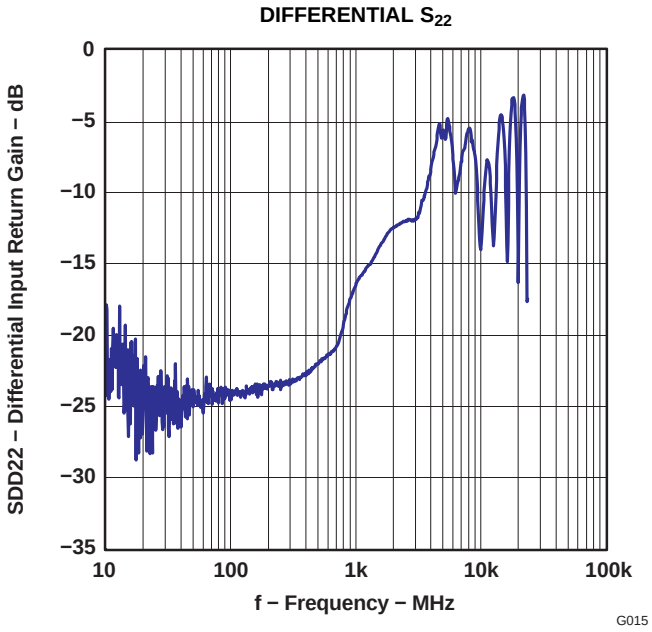

Figure 20.

APPLICATION INFORMATION

Figure 21 shows a typical application circuit using the ONET1191V with a common-cathode VCSEL, biased to V_{CC}, and driven differentially. The VCSEL driver is controlled via the two-wire interface SDA/SCK by a microprocessor. In a typical application, the FLT, MONP, MONB, and TS outputs are also connected to the microcontroller for transceiver management purposes. The monitor photodiode anode is grounded and the photodiode polarity bit, PDP, must be set to 0.

The component values in Figure 21 are typical examples and may be varied according to the intended application. For best performance, it is recommended to use differential drive. Single-ended VCSEL drive can be implemented by terminating the unused driver output in a resistance that matches the VCSEL series resistance; however, the available VCSEL modulation current is halved.

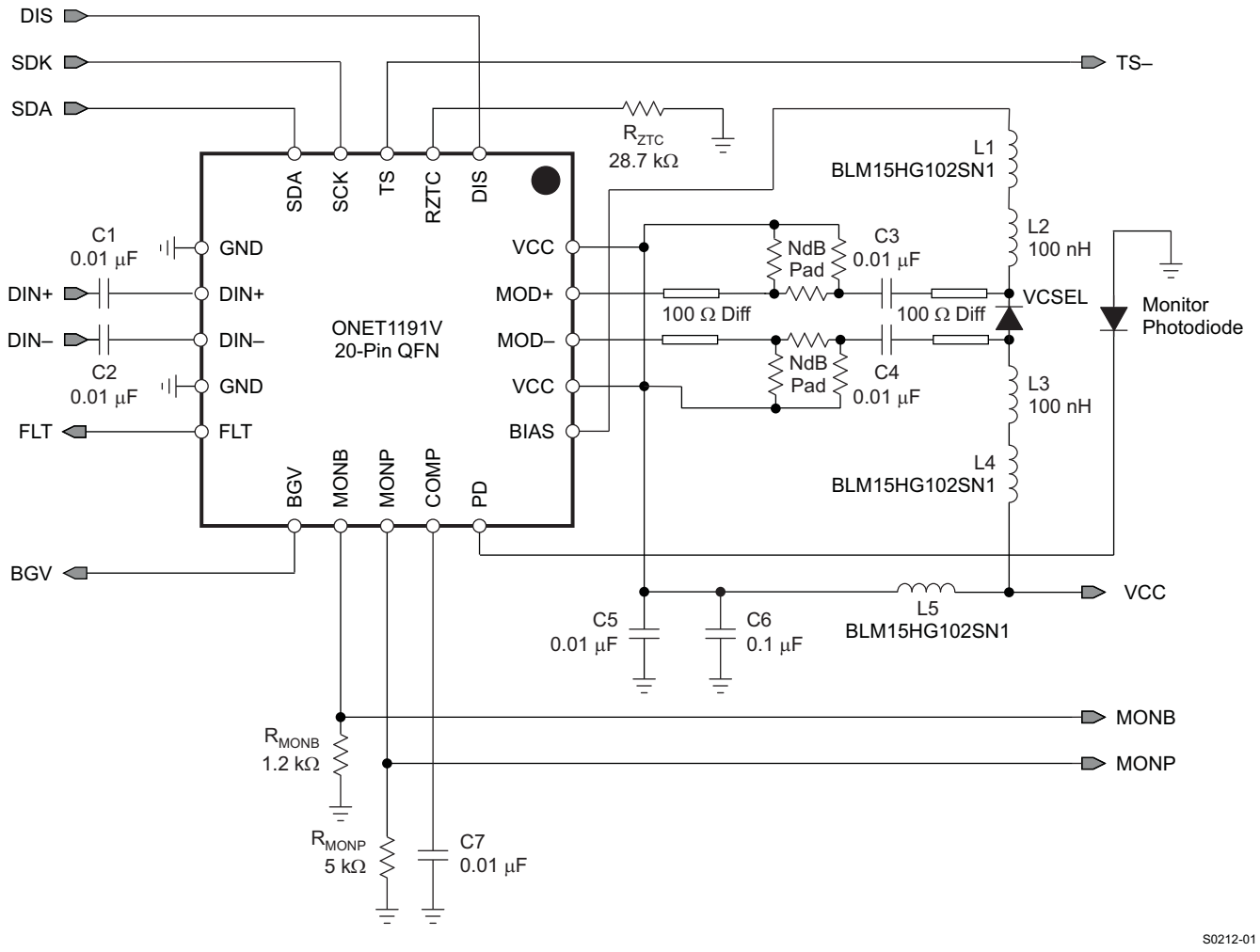

Figure 21. Typical Application Circuit With a Common Cathode VCSEL

In the recommended application circuit, the purpose of the attenuator pads is to improve the signal integrity between the VCSEL driver and the VCSEL. Because the VCSEL impedance is reactive, the pads attenuate reflections and provide a better matching impedance for the modulation current outputs. The disadvantage of using the attenuator pads is that the efficiency is reduced. That is, not all of the modulation current at the outputs of the VCSEL driver is available to drive the VCSEL. Table 7 lists the available modulation current at the VCSEL, I_{MOD}, depending on the modulation tail current register setting, I_{MODC}, the attenuator value, and the VCSEL series resistance. If care is taken in matching the output impedance of the ONET1191V to the impedance of the VCSEL, and if controlled-impedance transmission lines are used, attenuator pads may not be necessary.

Table 7. I_{MOD} vs I_{MODC} for a Given Attenuator Pad and VCSEL

I_{MODC} (mA): REGISTER SETTING	50-Ω PAD ATTENUATION (dB)	VCSEL SERIES RESISTANCE (Ω)	I_{MOD} (mA): MODULATION CURRENT AT THE VCSEL
40	3	100	14.76
40	6	100	10.52
30	3	100	11.07
30	6	100	7.89
20	3	100	7.38
20	6	100	5.26
40	3	60	18.33
40	6	60	13.12
30	3	60	13.75
30	6	60	9.84
20	3	60	9.17
20	6	60	6.56

LAYOUT GUIDELINES

For optimum performance, use 50-Ω transmission lines (100-Ω differential) for connecting the signal source to the DIN+ and DIN– pins and for connecting the modulation current outputs, MOD+ and MOD–, to the VCSEL. The length of the transmission lines should be kept as short as possible to reduce loss and pattern-dependent jitter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET1191VRGPT	ACTIVE	QFN	RGP	20	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ONET 1191V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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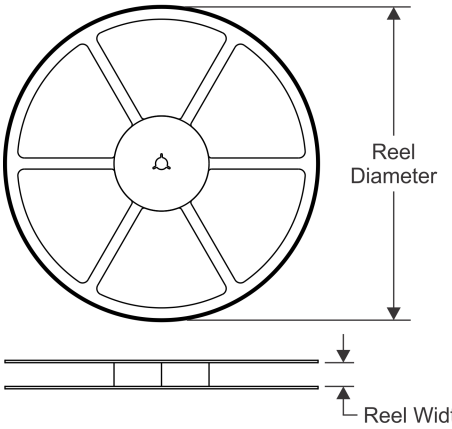
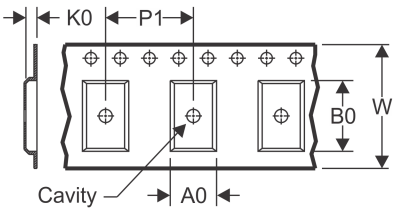
TAPE AND REEL INFORMATION

REEL DIMENSIONS

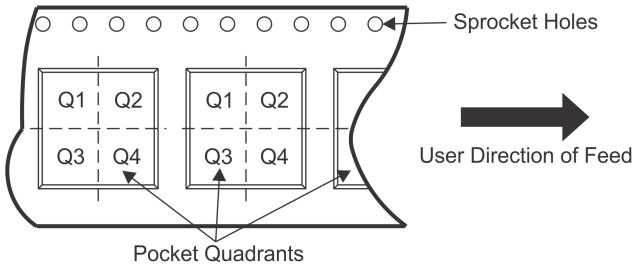


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

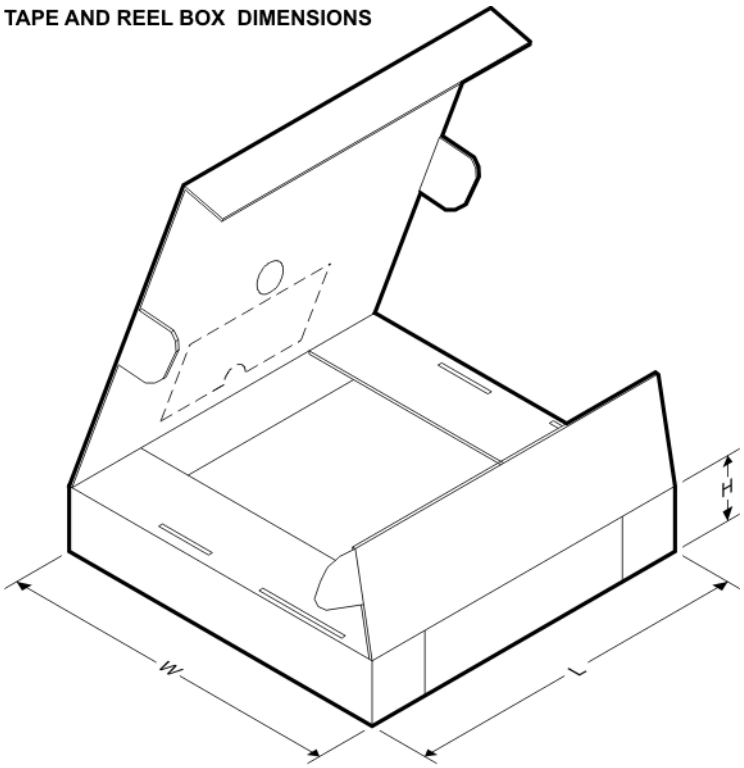
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET1191VRGPT	QFN	RGP	20	250	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

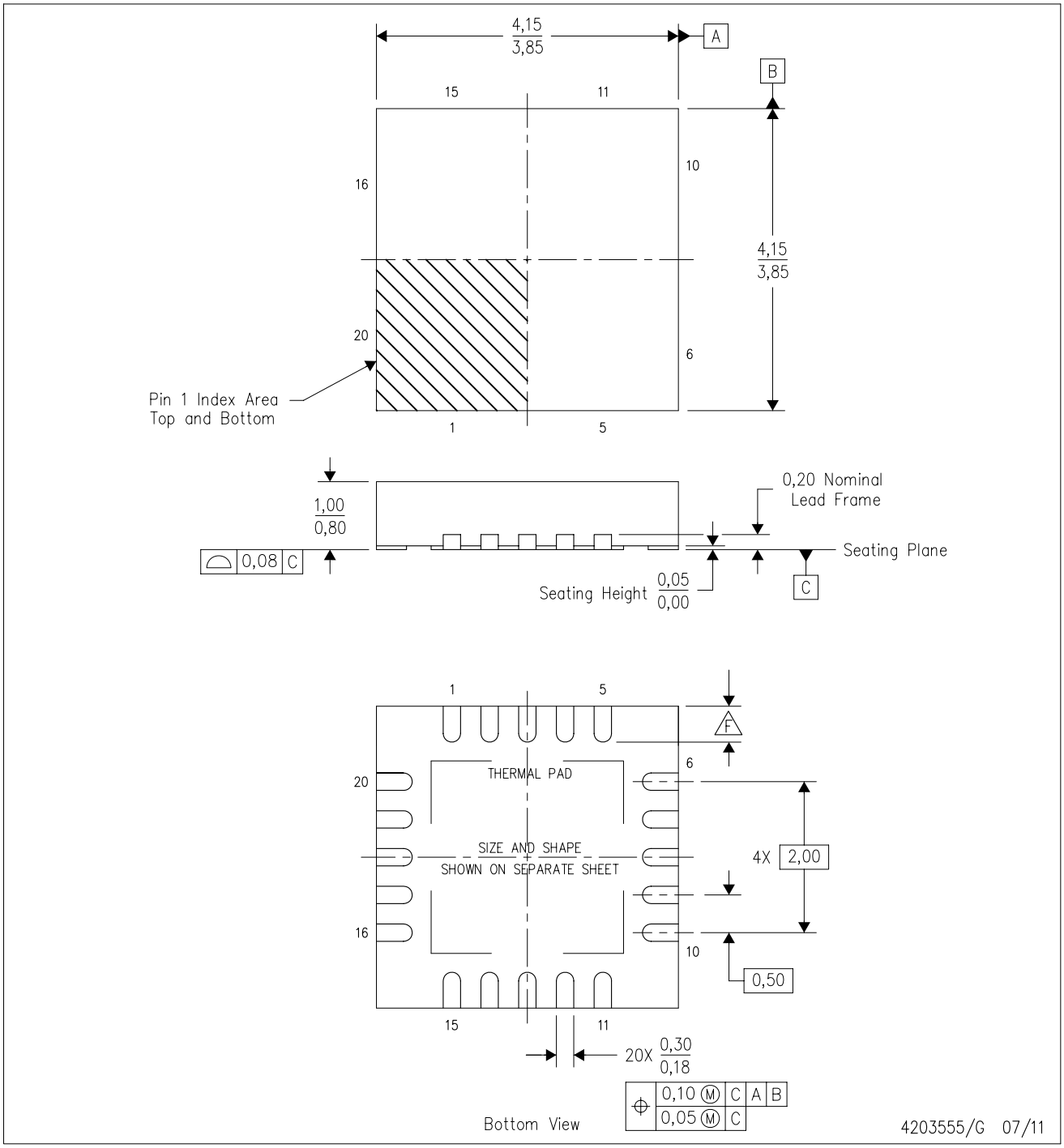
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ONET1191VRGPT	QFN	RGP	20	250	367.0	367.0	38.0

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

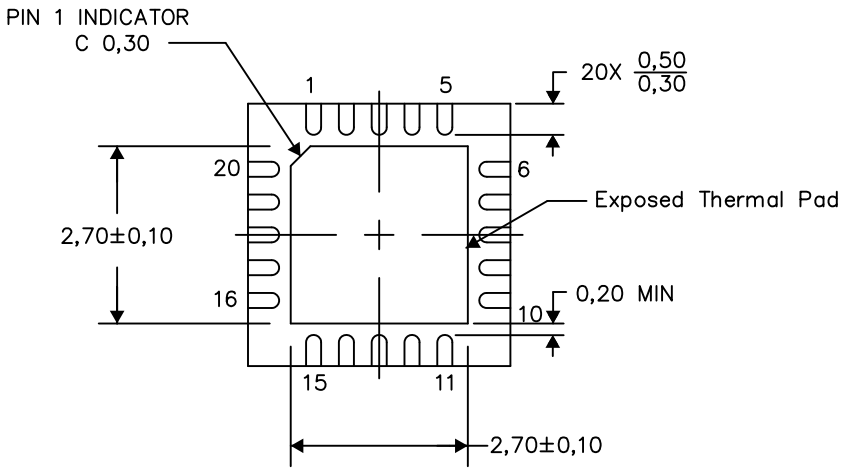
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



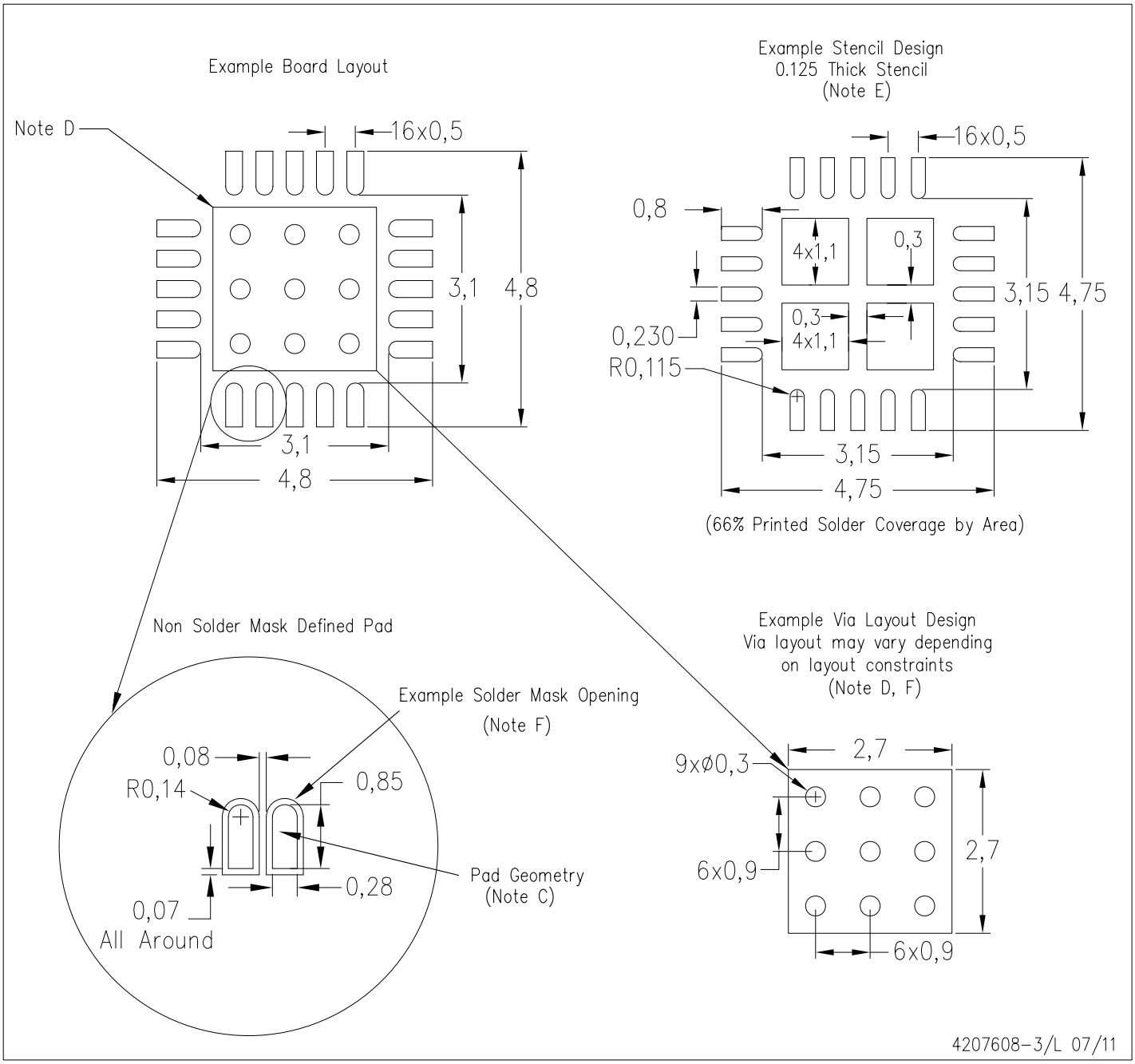
Bottom View

Exposed Thermal Pad Dimensions

4206346–3/AA 11/13

NOTES: A. All linear dimensions are in millimeters

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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