FAIRCHILD SEMICONDUCTOR™

April 1993
Revised January 1999

# 74ABT16500
# 18-Bit Universal Bus Transceivers with 3-STATE Outputs

## General Description

The ABT16500 18-bit universal bus transceiver combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock ($\overline{\text{CLKAB}}$ and $\overline{\text{CLKBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{\text{CLKAB}}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{\text{CLKAB}}$. Output-enable OEAB is active-high. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$. The output enables are complementary (OEAB is active HIGH and $\overline{\text{OEBA}}$ is active LOW).

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

## Features

- Combines D-Type latches and D-Type flip-flops for operation in transparent, latched, or clocked mode
- Flow-through architecture optimizes PCB layout
- Guaranteed latch-up protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

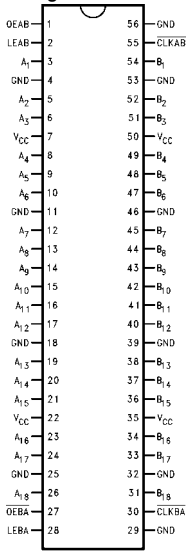
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ABT16500CSSC | MS56A | 56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide |
| 74ABT16500CMTD | MTD56 | 56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide |

Devices also available in Tape and Reel. Specify by appending the letter suffix "X" to the ordering code.

## Connection Diagram

**Pin Assignment for SSOP**




## Function Table (Note 1)

| Inputs | | | | Output |
|---|---|---|---|---|
| OEAB | LEAB | $\overline{\text{CLKAB}}$ | A | B |
| L | X | X | X | Z |
| H | H | X | L | L |
| H | H | X | H | H |
| H | L | ↓ | L | L |
| H | L | ↓ | H | H |
| H | L | H | X | $B_0$ (Note 2) |
| H | L | L | X | $B_0$ (Note 3) |

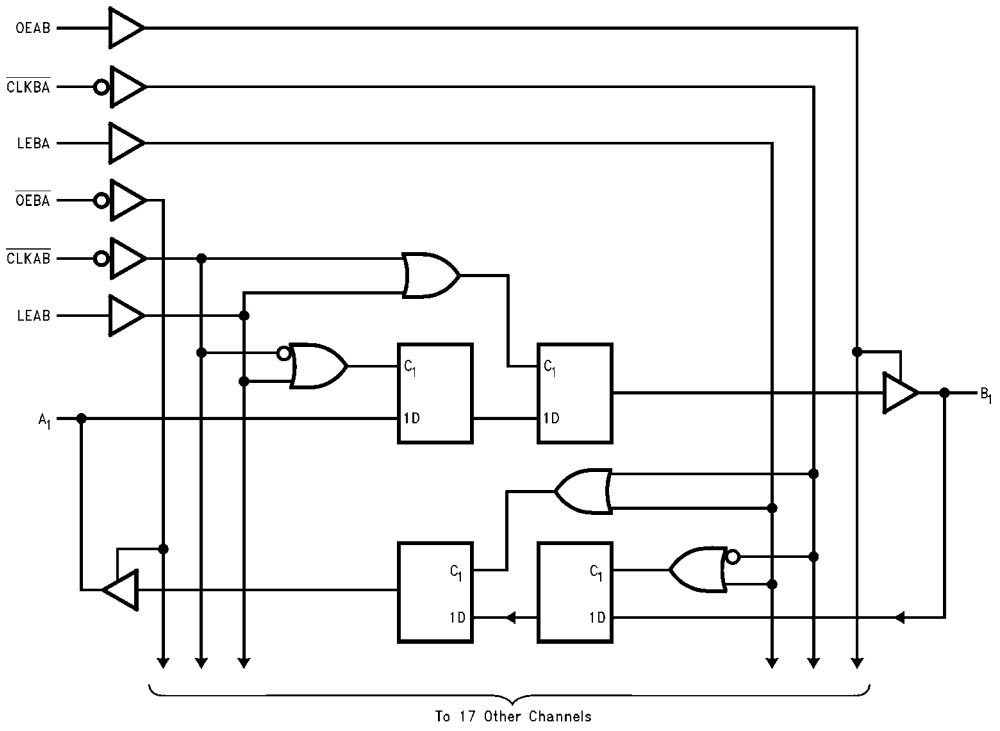
**Note 1:** A-to-B data flow is shown: B-to-A flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and $\overline{\text{CLKBA}}$.

**Note 2:** Output level before the indicated steady-state input conditions were established.

**Note 3:** Output level before the indicated steady-state input conditions were established, provided that $\overline{\text{CLKAB}}$ was LOW before LEAB went LOW.

## Logic Diagram



## Absolute Maximum Ratings(Note 4)

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +150°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 5) | −0.5V to +7.0V |
| Input Current (Note 5) | −30 mA to +5.0 mA |
| Voltage Applied to Any Output in the Disabled or Power-off State | −0.5V to 5.5V |
| in the HIGH State | −0.5V to $V_{CC}$ |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| DC Latchup Source Current | −500 mA |
| Over Voltage Latchup (I/O) | 10V |

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | −40°C to +85°C |
| Supply Voltage | +4.5V to +5.5V |
| Minimum Input Edge Rate (ΔV/Δt) | |
| Data Input | 50 mV/ns |
| Enable Input | 20 mV/ns |

**Note 4:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 5:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | V | | Recognized HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | V | | Recognized LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | −1.2 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 2.5 | | | V | Min | $I_{OH}$ = −3 mA |
| | | 2.0 | | | V | Min | $I_{OH}$ = −32 mA |
| $V_{OL}$ | Output LOW Voltage | | | 0.55 | V | Min | $I_{OL}$ = 64 mA |
| $I_{IH}$ | Input HIGH Current | | | 1 | µA | Max | $V_{IN}$ = 2.7V (Note 6) |
| | | | | 1 | | | $V_{IN}$ = $V_{CC}$ |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | 7 | µA | Max | $V_{IN}$ = 7.0V |
| $I_{IL}$ | Input LOW Current | | | −1 | µA | Max | $V_{IN}$ = 0.5V (Note 6) |
| | | | | −1 | | | $V_{IN}$ = 0.0V |
| $V_{ID}$ | Input Leakage Test | 4.75 | | | V | 0.0 | $I_{ID}$ = 1.9 µA<br>All Other Pins Grounded |
| $I_{IH}$ + $I_{OZH}$ | Output Leakage Current | | | 10 | µA | 0 – 5.5V | $V_{OUT}$ = 2.7V; $\overline{OE}$, OE = 2.0V |
| $I_{IL}$ + $I_{OZL}$ | Output Leakage Current | | | −10 | µA | 0 – 5.5V | $V_{OUT}$ = 0.5V; $\overline{OE}$, OE = 2.0V |
| $I_{OS}$ | Output Short-Circuit Current | −100 | | −275 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | µA | Max | $V_{OUT}$ = $V_{CC}$ |
| $I_{ZZ}$ | Bus Drainage Test | | | 100 | µA | 0.0 | $V_{OUT}$ = 5.5V; All Others GND |
| $I_{CCH}$ | Power Supply Current | | | 1.0 | mA | Max | All Outputs HIGH |
| $I_{CCL}$ | Power Supply Current | | | 68 | µA | Max | An or Bn Outputs Low |
| $I_{CCZ}$ | Power Supply Current | | | 1.0 | mA | Max | $\overline{OE}_n$ = $V_{CC}$,<br>All Others at $V_{CC}$ or GND |
| $I_{CCT}$ | Additional $I_{CC}$/Input | | | 2.5 | mA | Max | $V_I$ = $V_{CC}$ − 2.1V<br>All Others at $V_{CC}$ or GND |
| $I_{CCD}$ | Dynamic $I_{CC}$ No Load (Note 6) | | | 0.23 | mA/MHz | Max | Outputs Open<br>Transparent Mode<br>One Bit Toggling, 50% Duty Cycle |

**Note 6:** Guaranteed, but not tested.

## DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | $V_{CC}$ | Conditions $C_L$ = 50 pF; $R_L$ = 500Ω |
|---|---|---|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | | 0.7 | 1.2 | V | 5.0 | $T_A$ = 25°C (Note 7) |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | −1.5 | −1.0 | | V | 5.0 | $T_A$ = 25°C (Note 7) |
| $V_{OHV}$ | Minimum HIGH Level Dynamic Output Voltage | 2.5 | 3.0 | | V | 5.0 | $T_A$ = 25°C (Note 8) |
| $V_{IHD}$ | Minimum HIGH Level Dynamic Input Voltage | 2.2 | 1.8 | | V | 5.0 | $T_A$ = 25°C (Note 9) |
| $V_{ILD}$ | Maximum LOW Level Dynamic Input Voltage | | 1.2 | 0.8 | V | 5.0 | $T_A$ = 25°C (Note 9) |

**Note 7:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output at LOW. Guaranteed, but not tested.

**Note 8:** Max number of outputs defined as (n). n − 1 data inputs are driven 0V to 3V. One output HIGH. Guaranteed, but not tested.

**Note 9:** Max number of data inputs (n) switching. n − 1 inputs switching 0V to 3V. Input-under-test switching: 3V to threshold ($V_{ILD}$), 0V to threshold ($V_{IHD}$). Guaranteed, but not tested.

## AC Electrical Characteristics

| Symbol | Parameter | $T_A$ = +25°C, $V_{CC}$ = +5V, $C_L$ = 50 pF | | | $T_A$ = −40°C to +85°C, $V_{CC}$ = 4.5V–5.5V, $C_L$ = 50 pF | | Units |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | |
| $f_{max}$ | Maximum Clock Frequency | 150 | 200 | | 150 | | MHz |
| $t_{PLH}$ | Propagation Delay | 1.5 | 2.7 | 4.6 | 1.5 | 4.6 | ns |
| $t_{PHL}$ | A or B to B or A | 1.5 | 3.2 | 4.6 | 1.5 | 4.6 | |
| $t_{PLH}$ | Propagation Delay | 1.5 | 3.1 | 5.0 | 1.5 | 5.0 | ns |
| $t_{PHL}$ | LEAB or LEBA to B or A | 1.5 | 3.6 | 5.0 | 1.5 | 5.0 | |
| $t_{PLH}$ | Propagation Delay | 1.5 | 3.4 | 5.3 | 1.5 | 5.3 | ns |
| $t_{PHL}$ | $\overline{CLKAB}$ or $\overline{CLKBA}$ to B or A | 1.5 | 3.7 | 5.3 | 1.5 | 5.3 | |
| $t_{PZH}$ | Propagation Delay | 1.5 | 2.7 | 5.6 | 1.5 | 5.6 | ns |
| $t_{PZL}$ | OEAB or $\overline{OEBA}$ to B or A | 1.5 | 3.0 | 5.6 | 1.5 | 5.6 | |
| $t_{PHZ}$ | Propagation Delay | 1.5 | 3.7 | 6.0 | 1.5 | 6.0 | ns |
| $t_{PLZ}$ | OEAB or $\overline{OEBA}$ to B or A | 1.5 | 3.2 | 6.0 | 1.5 | 6.0 | |

## AC Operating Requirements

| Symbol | Parameter | $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF | | $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_S(H)$ | Setup Time, | 4.5 | | 4.5 | | ns |
| $t_S(L)$ | A to $\overline{CLKAB}$ | 4.5 | | 4.5 | | |
| $t_H(H)$ | Hold Time, | 0 | | 0 | | ns |
| $t_H(L)$ | A to $\overline{CLKAB}$ | 0 | | 0 | | |
| $t_S(H)$ | Setup Time, | 4.0 | | 4.0 | | ns |
| $t_S(L)$ | B to $\overline{CLKBA}$ | 4.0 | | 4.0 | | |
| $t_H(H)$ | Hold Time, | 0 | | 0 | | ns |
| $t_H(L)$ | B to $\overline{CLKBA}$ | 0 | | 0 | | |
| $t_S(H)$ | Setup Time, A to LEAB | 1.5 | | 1.5 | | ns |
| $t_S(L)$ | or B to LEBA, $\overline{CLK}$ HIGH | 1.5 | | 1.5 | | |
| $t_H(H)$ | Hold Time, A to LEAB | 1.5 | | 1.5 | | ns |
| $t_H(L)$ | or B to LEBA, $\overline{CLK}$ HIGH | 1.5 | | 1.5 | | |
| $t_S(H)$ | Setup Time, A to LEAB | 4.5 | | 4.5 | | ns |
| $t_S(L)$ | or B to LEBA, $\overline{CLK}$ LOW | 4.5 | | 4.5 | | |
| $t_H(H)$ | Hold Time, A to LEAB | 1.5 | | 1.5 | | ns |
| $t_H(L)$ | or B to LEBA, $\overline{CLK}$ LOW | 1.5 | | 1.5 | | |
| $t_W(H)$ | Pulse Width, | 3.3 | | 3.3 | | ns |
| $t_W(L)$ | LEAB or LEBA, HIGH | 3.3 | | 3.3 | | |
| $t_W(H)$ | Pulse Width, $\overline{CLKAB}$ | 3.3 | | 3.3 | | ns |
| $t_W(L)$ | or $\overline{CLKBA}$, HIGH or LOW | 3.3 | | 3.3 | | |

## Extended AC Electrical Characteristics

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 50$ pF, 18 Outputs Switching (Note 10) | | | $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 1 Output Switching (Note 11) | | $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V–5.5V$, $C_L = 250$ pF, 18 Outputs Switching (Note 12) | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Max | Min | Max | |
| $t_{PLH}$ | Propagation Delay | 1.5 | | 6.5 | 2.0 | 7.0 | 2.5 | 9.9 | ns |
| $t_{PHL}$ | Data to Outputs | 1.5 | | 6.5 | 2.0 | 7.0 | 2.5 | 9.2 | |
| $t_{PLH}$ | Propagation Delay | 1.5 | | 6.0 | 2.0 | 7.5 | 2.5 | 8.5 | ns |
| $t_{PHL}$ | LEAB or LEBA to B or A | 1.5 | | 6.0 | 2.0 | 7.5 | 2.5 | 8.5 | |
| $t_{PLH}$ | Propagation Delay | 1.5 | | 6.2 | 2.0 | 7.7 | 2.5 | 8.5 | ns |
| $t_{PHL}$ | $\overline{CLKAB}$ or $\overline{CLKBA}$ to B or A | 1.5 | | 6.2 | 2.0 | 7.7 | 2.5 | 8.5 | |
| $t_{PZH}$ | Output Enable Time | 1.5 | | 6.5 | 2.0 | 7.0 | 2.5 | 8.5 | ns |
| $t_{PZL}$ | | 1.5 | | 6.5 | 2.5 | 7.0 | 2.5 | 8.5 | |
| $t_{PHZ}$ | Output Disable | 1.5 | | 6.5 | (Note 13) | | (Note 13) | | ns |
| $t_{PLZ}$ | Time | 1.5 | | 6.5 | | | | | |

**Note 10:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.).

**Note 11:** This specification is guaranteed but not tested. The limits represent propagation delay with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.

**Note 12:** This specification is guaranteed but not tested. The limits represent propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.) with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 13:** 3-STATE delays are dominated by the RC network (500Ω, 250 pF) on the output and have been excluded from the datasheet.

## Skew

| Symbol | Parameter | $T_A = -40°C$ to $+85°C$<br>$V_{CC} = 4.5V–5.5V$<br>$C_L = 50$ pF<br>18 Outputs Switching<br>(Note 14) | $T_A = -40°C$ to $+85°C$<br>$V_{CC} = 4.5V–5.5V$<br>$C_L = 250$ pF<br>18 Outputs Switching<br>(Note 15) | Units |
|---|---|---|---|---|
| | | Max | Max | |
| $t_{OSHL}$<br>(Note 16) | Pin to Pin Skew<br>HL Transitions | 2.0 | 2.8 | ns |
| $t_{OSLH}$<br>(Note 16) | Pin to Pin Skew<br>LH Transitions | 2.0 | 2.5 | ns |
| $t_{PS}$<br>(Note 17) | Duty Cycle<br>LH–HL Skew | 2.0 | 2.8 | ns |
| $t_{OST}$<br>(Note 16) | Pin to Pin Skew<br>LH/HL Transitions | 2.5 | 3.0 | ns |
| $t_{PV}$<br>(Note 18) | Device to Device Skew<br>LH/HL Transitions | 3.0 | 3.5 | ns |

**Note 14:** This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all LOW-to-HIGH, HIGH-to-LOW, etc.)

**Note 15:** These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

**Note 16:** Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH-to-LOW ($t_{OSHL}$), LOW-to-HIGH ($t_{OSLH}$), or any combination switching LOW-to-HIGH and/or HIGH-to-LOW ($t_{OST}$). The specification is guaranteed but not tested.

**Note 17:** This describes the difference between the delay of the LOW-to-HIGH and the HIGH-to-LOW transition on the same pin. It is measured across all the outputs (drivers) on the same chip, the worst (largest delta) number is the guaranteed specification. This specification is guaranteed but not tested.

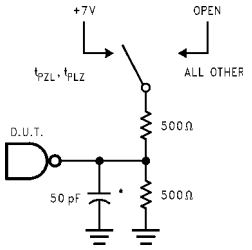
**Note 18:** Propagation delay variation for a given set of conditions (i.e., temperature and $V_{CC}$) from device to device. This specification is guaranteed but not tested.

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions<br>$T_A = 25°C$ |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5.0 | pF | $V_{CC} = 0.0V$ |
| $C_{I/O}$ (Note 19) | Output Capacitance | 11.0 | pF | $V_{CC} = 5.0V$ |

**Note 19:** $C_{I/O}$ is measured at frequency f = 1 MHz per MIL-STD-883, Method 3012.

## AC Loading




*Includes jig and probe capacitance.

**FIGURE 1. Standard AC Test Load**

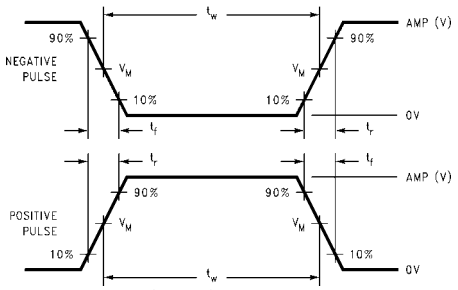



**FIGURE 2. $V_M$ = 1.5V**

**Input Pulse Requirements**

| Amplitude | Rep. Rate | $t_W$ | $t_r$ | $t_f$ |
|---|---|---|---|---|
| 3.0V | 1 MHz | 500 ns | 2.5 ns | 2.5 ns |

**FIGURE 3. Test Input Signal Requirements**

## AC Waveforms

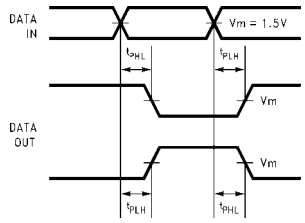



**FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions**

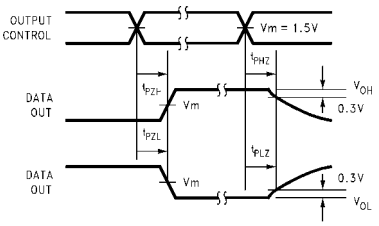



**FIGURE 6. 3-STATE Output HIGH and LOW Enable and Disable Times**

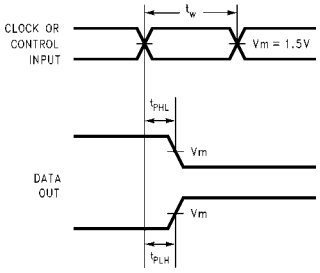



**FIGURE 5. Propagation Delay, Pulse Width Waveforms**

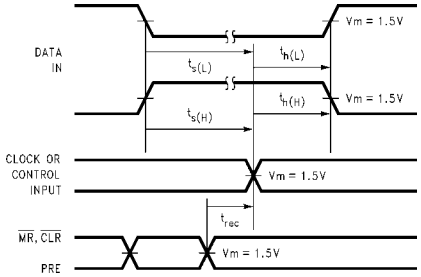
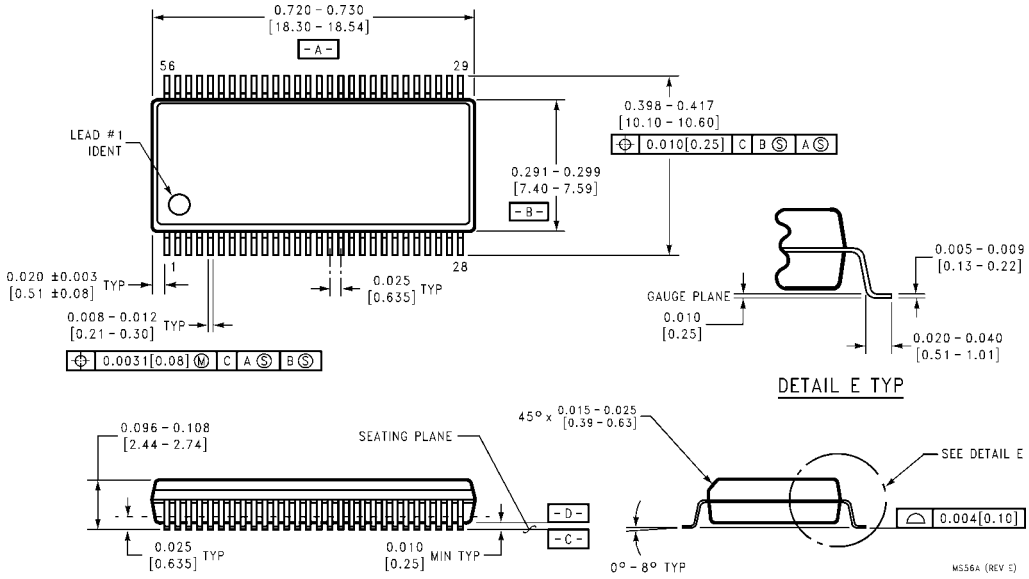


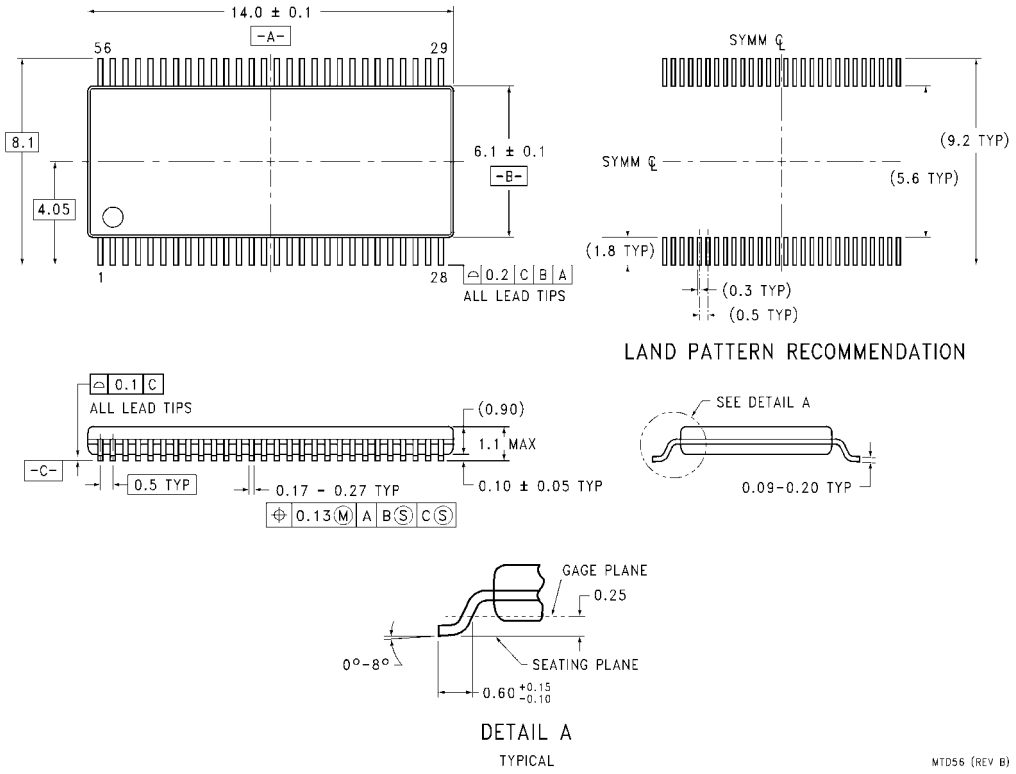

**FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms**

## Physical Dimensions inches (millimeters) unless otherwise noted




**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide**
**Package Number MS56A**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)




**56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide**
**Package Number MTD56**

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