

MM74HC157 Quad 2-Input Multiplexer

General Description

The MM74HC157 high speed Quad 2-to-1 Line data selector/Multiplexers utilizes advanced silicon-gate CMOS technology. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

This device consists of four 2-input digital multiplexers with common select and STROBE inputs. When the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0".

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2–6V
- Low power supply quiescent current: 80 μ A maximum (74HC Series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μ A maximum

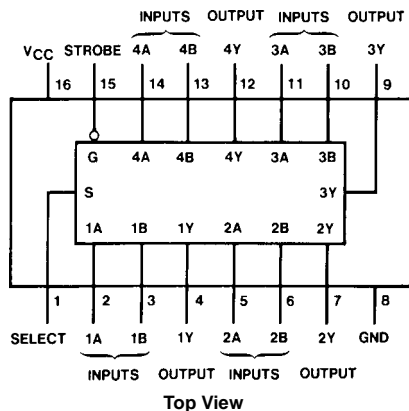
Ordering Code:

| Order Number | Package Number | Package Description |
|--------------|----------------|--|
| MM74HC157M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow |
| MM74HC157SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| MM74HC157MTC | MTC16 | 16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| MM74HC157N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP

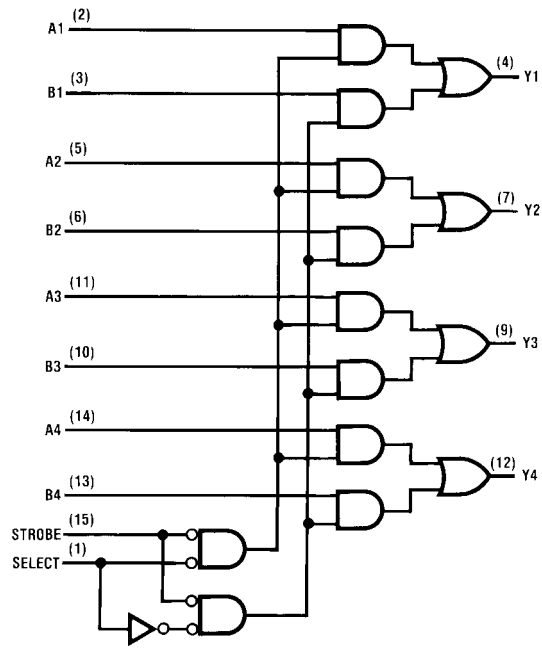


Function Table

| Strobe | Inputs | | Output |
|--------|--------|---|--------|
| | Select | Y | |
| H | X | X | L |
| L | L | L | L |
| L | L | H | H |
| L | H | X | L |
| L | H | X | H |

H = HIGH Level,
L = LOW Level
X = Irrelevant

Logic Diagram

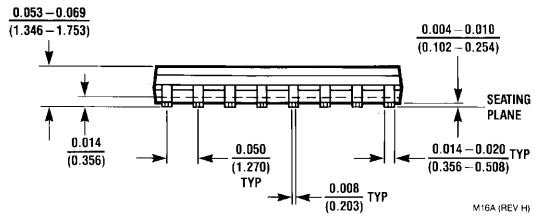
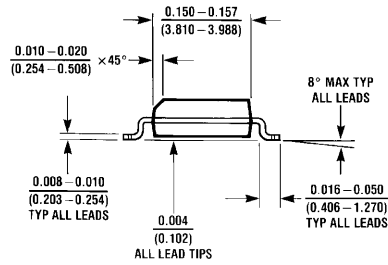
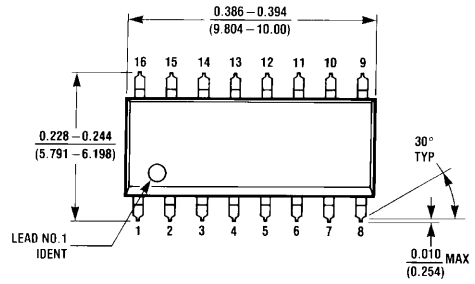


| AC Electrical Characteristics | | | | | |
|--|---|------------|-----|------------------|-------|
| $V_{CC} = 5V, T_A = 25^\circ C, C_L = 15 \text{ pF}, t_r = t_f = 6 \text{ ns}$ | | | | | |
| Symbol | Parameter | Conditions | Typ | Guaranteed Limit | Units |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Data to Output | | 14 | 20 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Select to Output | | 14 | 20 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Strobe to Output | | 12 | 18 | ns |

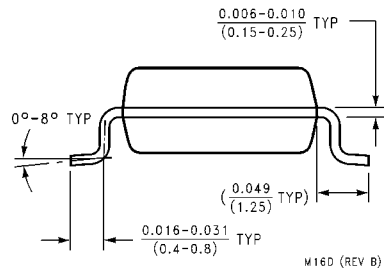
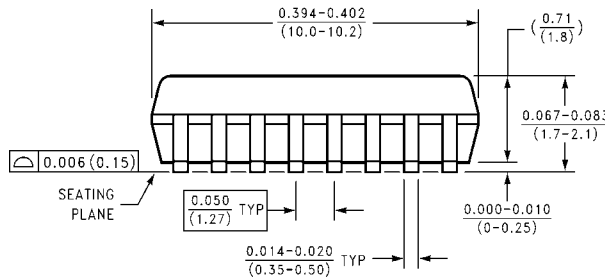
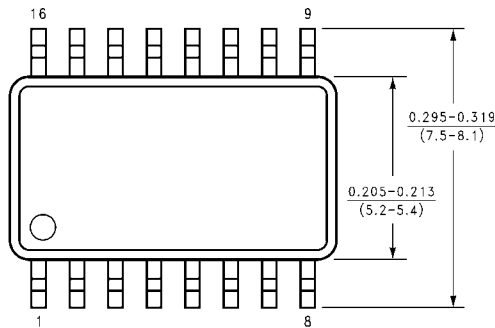
| AC Electrical Characteristics | | | | | | | | |
|--|---|-------------------|----------|--------------------|------------------------------------|-------------------------------------|-------|----|
| $C_L = 50 \text{ pF}, t_r = t_f = 6 \text{ ns}$ (unless otherwise specified) | | | | | | | | |
| Symbol | Parameter | Conditions | V_{CC} | $T_A = 25^\circ C$ | $T_A = -40 \text{ to } 85^\circ C$ | $T_A = -55 \text{ to } 125^\circ C$ | Units | |
| | | | | Typ | Guaranteed Limits | | | |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Data to Output | | 2.0V | 63 | 125 | 158 | 186 | ns |
| | | | 4.5V | 13 | 25 | 32 | 37 | ns |
| | | | 6.0V | 11 | 21 | 27 | 32 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Select to Output | | 2.0V | 63 | 125 | 158 | 186 | ns |
| | | | 4.5V | 13 | 25 | 32 | 37 | ns |
| | | | 6.0V | 11 | 21 | 27 | 32 | ns |
| t_{PHL}, t_{PLH} | Maximum Propagation Delay, Strobe to Output | | 2.0V | 58 | 115 | 145 | 171 | ns |
| | | | 4.5V | 12 | 23 | 29 | 34 | ns |
| | | | 6.0V | 10 | 20 | 25 | 29 | ns |
| t_{TLH}, t_{THL} | Maximum Output Rise and Fall Time | | 2.0V | 30 | 75 | 95 | 110 | ns |
| | | | 4.5V | 8 | 15 | 19 | 22 | ns |
| | | | 6.0V | 7 | 13 | 16 | 19 | ns |
| C_{IN} | Maximum Input Capacitance | | | 5 | 10 | 10 | 10 | pF |
| C_{PD} | Power Dissipation Capacitance (Note 5) | (per Multiplexer) | | 57 | | | | pF |

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches (millimeters) unless otherwise noted

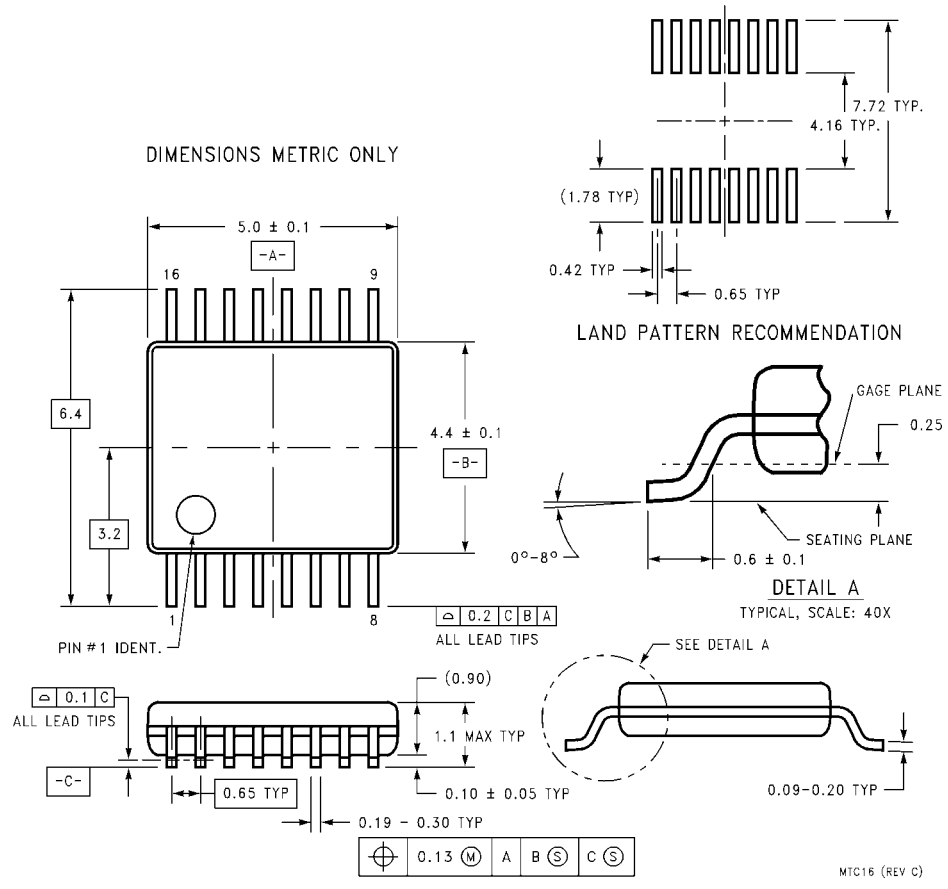


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow Package Number M16A



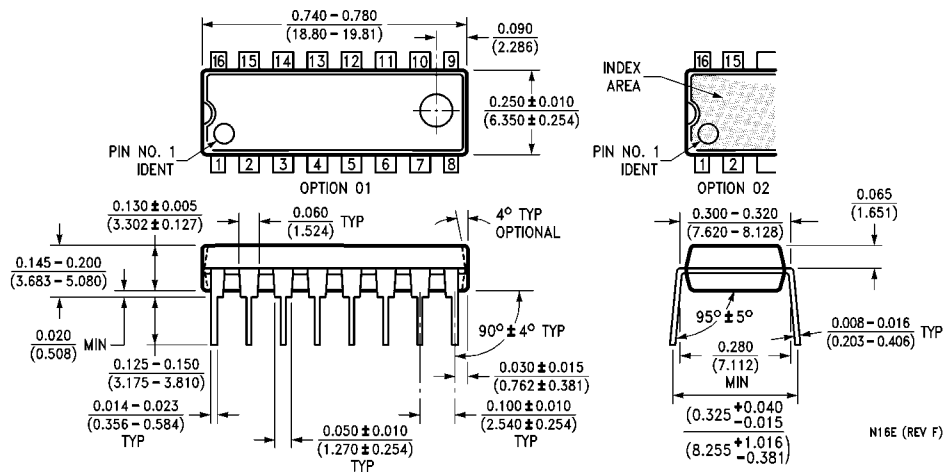
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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