



4 X 4 Register File With 3-State Outputs

**ELECTRICALLY TESTED PER:
MIL-M-38510/31901**

The 54LS670 is a high-speed, low-power 4 x 4 Register File organized as four words by four bits. Separate read and write inputs, both address and enable, allow simultaneous read and write operation.

The 3-state outputs make it possible to connect up to 128 outputs to increase the word capacity up to 512 words. Any number of these devices can be operated in parallel to generate an n-bit length.

- Simultaneous Read/Write Operation
- Expandable to 512 Words of n-Bits
- Typical Access Time of 20 ns
- 3-State Outputs for Expansion
- Typical Power Dissipation of 125 mW

Write Inputs			Word			
W _B	W _A	W̄	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

NOTES:

- A. H = high level, L = low level, X = irrelevant.
- B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
- C. Q₀ = the level of Q before the indicated input conditions were established.
- D. W0B1 = The first bit of word 0, etc.

Read Inputs			Outputs			
R _B	R _A	R̄	Q ₁	Q ₂	Q ₃	Q ₄
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

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- C. Q₀ = the level of Q before the indicated input conditions were established.
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Military 54LS670



AVAILABLE AS:

- 1) JAN: JM38510/31901BXA
- 2) SMD: 7704201
- 3) 883: 54LS670/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

**THE LETTER "M" APPEARS
BEFORE THE / ON LCC.**

PIN ASSIGNMENTS

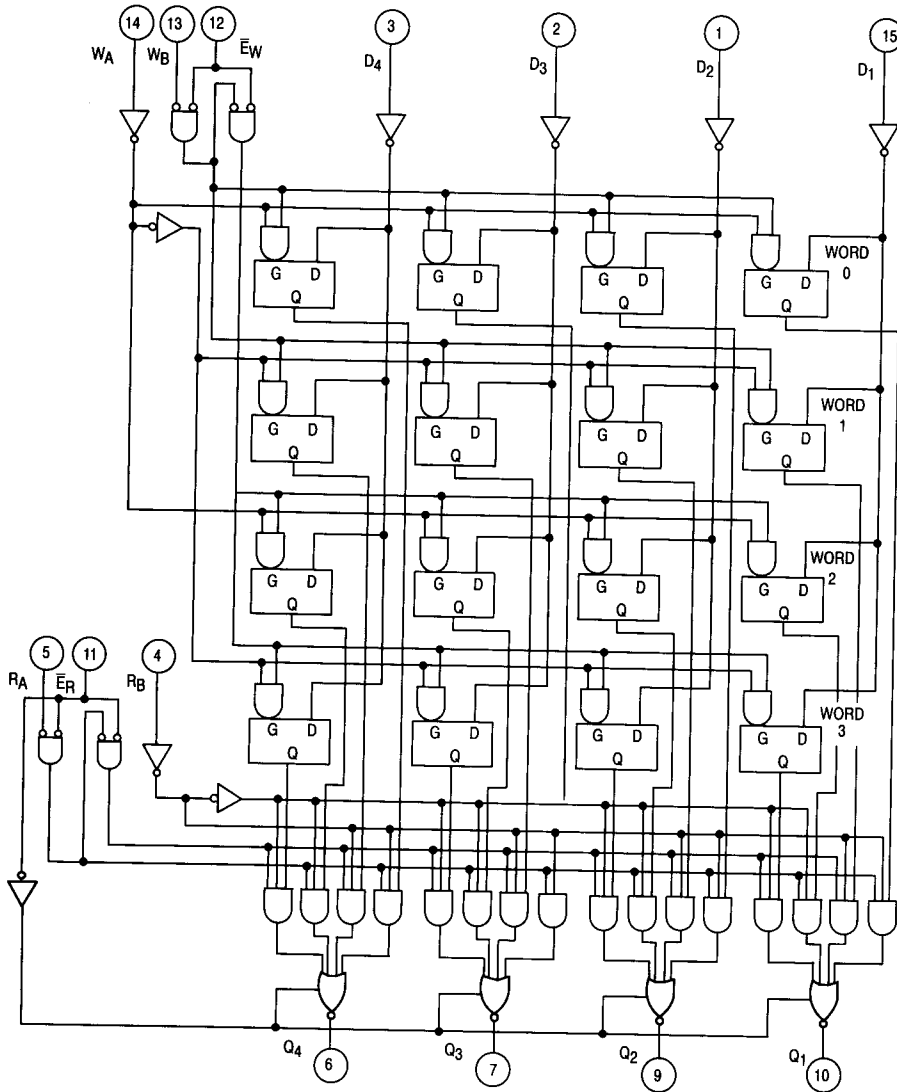
FUNCT.	DIL 620-09	FLATS 650-05	LCC 756A-02	BURN-IN (COND. A)
D ₂	1	1	2	VCC
D ₃	2	2	3	VCC
D ₄	3	3	4	VCC
R _B	4	4	5	VCC
R _A	5	5	7	VCC
Q ₄	6	6	8	VCC
Q ₃	7	7	9	VCC
GND	8	8	10	GND
Q ₂	9	9	12	VCC
Q ₁	10	10	13	VCC
R̄	11	11	14	VCC
W̄	12	12	15	VCC
W _B	13	13	17	VCC
W _A	14	14	18	VCC
D ₁	15	15	19	VCC
VCC	16	16	20	VCC

BURN-IN CONDITIONS:

VCC = 5.0 V MIN/6.0 V MAX

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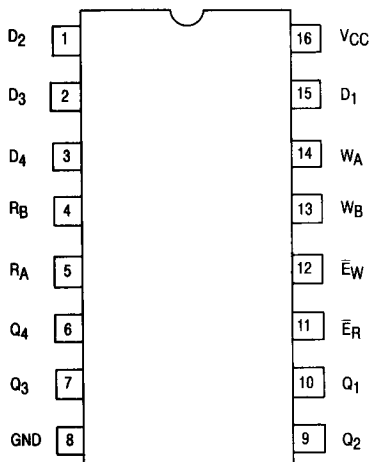
LOGIC DIAGRAM



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CONNECTION DIAGRAM



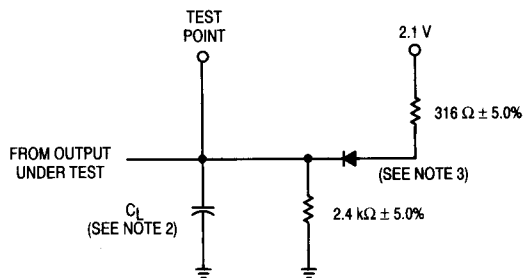
NOTES:

1. The input pulse has the following characteristics: PRR ≤ 1.0 MHz, $t_r \leq 15$ ns, and $t_f \leq 6.0$ ns; duty cycle = $50\% \pm 15\%$.
2. $C_L = 50$ pF $\pm 10\%$, including scope probe and jig capacitance.
3. All diodes are 1N3064 and 1N916.
4. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.7 V, or open)
5. Voltage measurements are made with respect to network ground terminal.

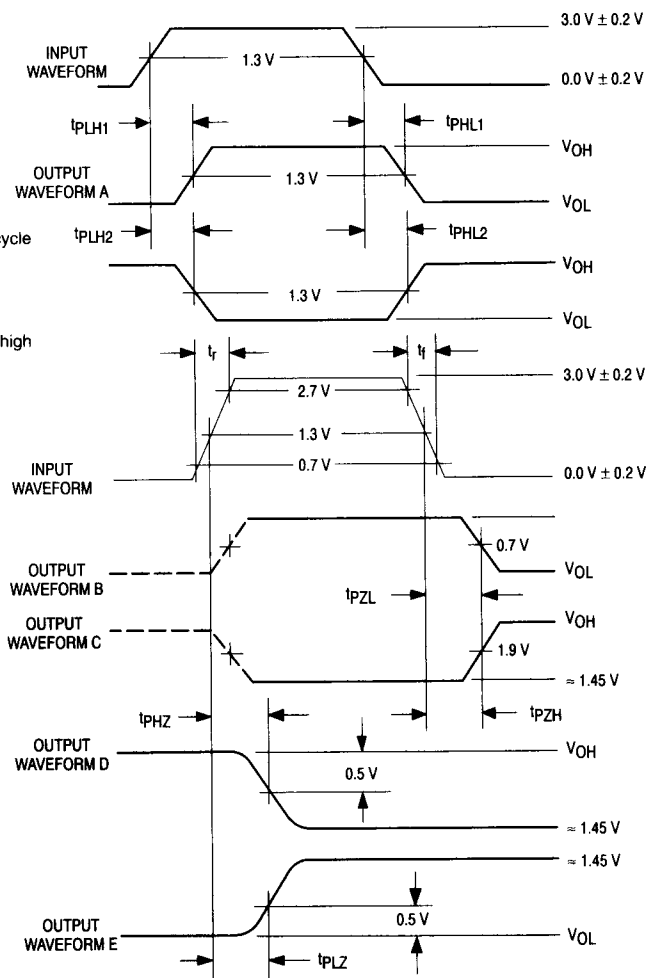
SWITCH POSITIONS

Symbol	SW1	SW2
t_{pZH}	Open	Closed
t_{pZL}	Closed	Open
t_{pLZ}	Closed	Closed
t_{pHZ}	Closed	Closed

AC TEST CIRCUIT

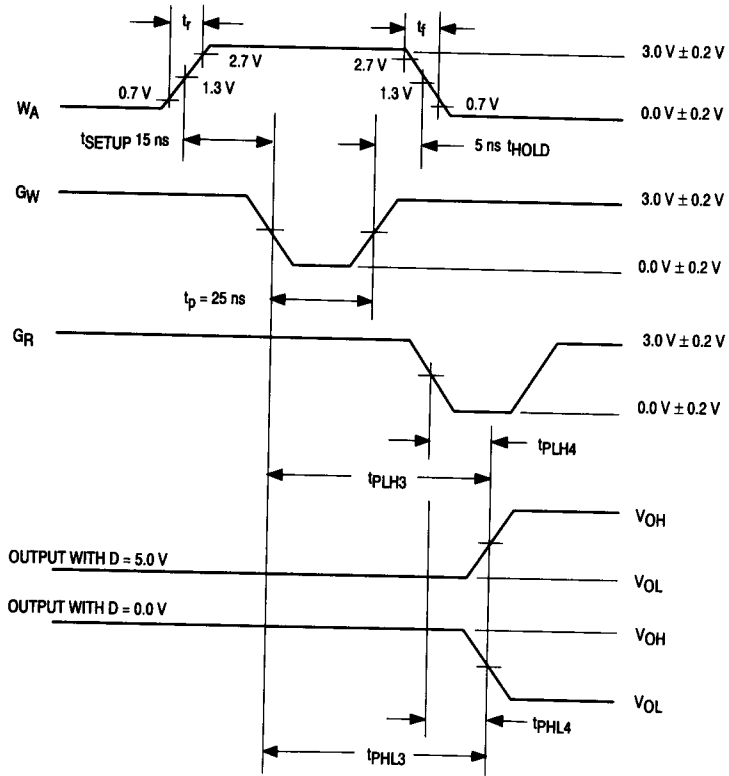


WAVEFORMS



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WAVEFORMS



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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
		Min	Max	Min	Max	Min	Max		
V _{OH}	Logical "1" Output Voltage	2.4		2.4		2.4		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{IH} = 2.0 V, other inputs = 0.7 V.
V _{OL}	Logical "0" Output Voltage		0.4		0.4		0.4	V	V _{CC} = 4.5 V, I _{OL} = 4.0 mA, V _{IL} = 0.7 V.
V _{IC}	Input Clamping Voltage		- 1.5					V	V _{CC} = 4.5 V, I _{IN} = - 18 mA, other inputs are open.
I _{IL1}	Logical "0" Input Current	- 135	- 370	- 135	- 370	- 135	- 370	μA	V _{CC} = 5.5 V, V _{IN} = 0.4 V, other inputs are open.
I _{IL2}	Logical "0" Input Current	- 0.48	- 1.2	- 0.48	- 1.2	- 0.48	- 1.2	mA	V _{CC} = 5.5 V, V _{IN(ER)} = 0.4 V, other inputs are open.
I _{IL3}	Logical "0" Input Current	- 0.32	- 0.8	- 0.32	- 0.8	- 0.32	- 0.8	mA	V _{CC} = 5.5 V, V _{IN(RA)} = 0.4 V, other inputs are open.
I _{IL4}	Logical "0" Input Current	- 150	- 380	- 150	- 380	- 150	- 380	μA	V _{CC} = 5.5 V, V _{IN(EW)} = 0.4 V, other inputs are open.
I _{IH1}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open.
I _{IHH1}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 5.5 V, other inputs are open.
I _{IH2}	Logical "1" Input Current		40		40		40	μA	V _{CC} = 5.5 V, V _{IH(EW)} = 2.7 V, other inputs are open.
I _{IHH2}	Logical "1" Input Current		300		300		300	μA	V _{CC} = 5.5 V, V _{IHH(ER)} = 5.5 V, other inputs are open.
I _{IH3}	Logical "1" Input Current		60		60		60	μA	V _{CC} = 5.5 V, V _{IH(ER)} = 2.7 V, other inputs are open.
I _{IHH3}	Logical "1" Input Current		200		200		200	μA	V _{CC} = 5.5 V, V _{IHH(EW)} = 5.5 V, other inputs are open.
I _{OS}	Output Short Circuit Current	- 30	- 130	- 30	- 130	- 30	- 130	mA	V _{CC} = 5.5 V, V _{IN} = 5.5 V, other inputs are GND, V _{OUT} = GND.
I _{CC}	Power Supply Current Off		50		50		50	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V, other inputs are GND.
I _{OZH}	Output Off Current High		20		20		20	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other inputs = 0.7 V, V _{OUT} = 2.7 V.
I _{OZL}	Output Off Current Low		- 20		- 20		- 20	μA	V _{CC} = 5.5 V, V _{IN} = 2.0 V, other inputs = 0.7 V, V _{OUT} = 0.4 V.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.7		0.7		0.7	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 5.0 V, V _{INL} = 0.4 V, and V _{IINH} = 2.4 V.

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Symbol	Parameter	Limits						Unit	Test Condition (Unless Otherwise Specified)
		+ 25°C		+ 125°C		- 55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
tPHL1 tPHL1	Propagation Delay D to Q _n	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPLH1 tPLH1	Propagation Delay D to Q _n	2.0 —	50 45	2.0 —	65 60	2.0 —	65 60	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPHL2 tPHL2	Propagation Delay R _A or R _B to Q _n	2.0 —	50 45	2.0 —	65 60	2.0 —	65 60	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPLH2 tPLH2	Propagation Delay R _A or R _B to Q _n	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPHL3 tPHL3	Propagation Delay E _W to Q _n	2.0 —	55 50	2.0 —	72 67	2.0 —	72 67	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPLH3 tPLH3	Propagation Delay E _W to Q _n	2.0 —	50 45	2.0 —	65 60	2.0 —	65 60	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPHZ tPHZ	Propagation Delay Output Disable Time	2.0 —	55 50	2.0 —	72 67	2.0 —	72 67	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 5.0 pF.
tPLZ tPLZ	Propagation Delay Output Disable Time	2.0 —	40 35	2.0 —	52 48	2.0 —	52 48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 5.0 pF.
tPZH tPZH	Propagation Delay Output Enable Time	2.0 —	40 35	2.0 —	52 48	2.0 —	52 48	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.
tPZL tPZL	Propagation Delay Output Enable Time	2.0 —	45 40	2.0 —	58 53	2.0 —	58 53	ns	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 316 Ω V _{CC} = 5.0 V, C _L = 45 pF.