

74AHC594; 74AHCT594

8-bit shift register with output register

Rev. 02 — 9 June 2008

Product data sheet

1. General description

The 74AHC594; 74AHCT594 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC594; 74AHCT594 is an 8-bit, non-inverting, serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks (SHCP and STCP) and direct overriding clears (SHR and STR) are provided on both the shift and storage registers. A serial output (Q7S) is provided for cascading purposes.

Both the shift and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register will always be one count pulse ahead of the storage register.

2. Features

- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Wide supply voltage range from 2.0 V to 5.5 V
- 8-bit serial-in, parallel-out shift register with storage
- Independent direct overriding clears on shift and storage registers
- Independent clocks for shift and storage registers
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Input levels:
 - ◆ For 74AHC594: CMOS level
 - ◆ For 74AHCT594: TTL level
- ESD protection:
 - ◆ HBM EIA/JESD22-A114E exceeds 2000 V
 - ◆ MM EIA/JESD22-A115-A exceeds 200 V
 - ◆ CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$

3. Applications

- Serial-to parallel data conversion
- Remote control holding register

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AHC594				
74AHC594D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHC594DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHC594PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHC594BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74AHCT594				
74AHCT594D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74AHCT594DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74AHCT594PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74AHCT594BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

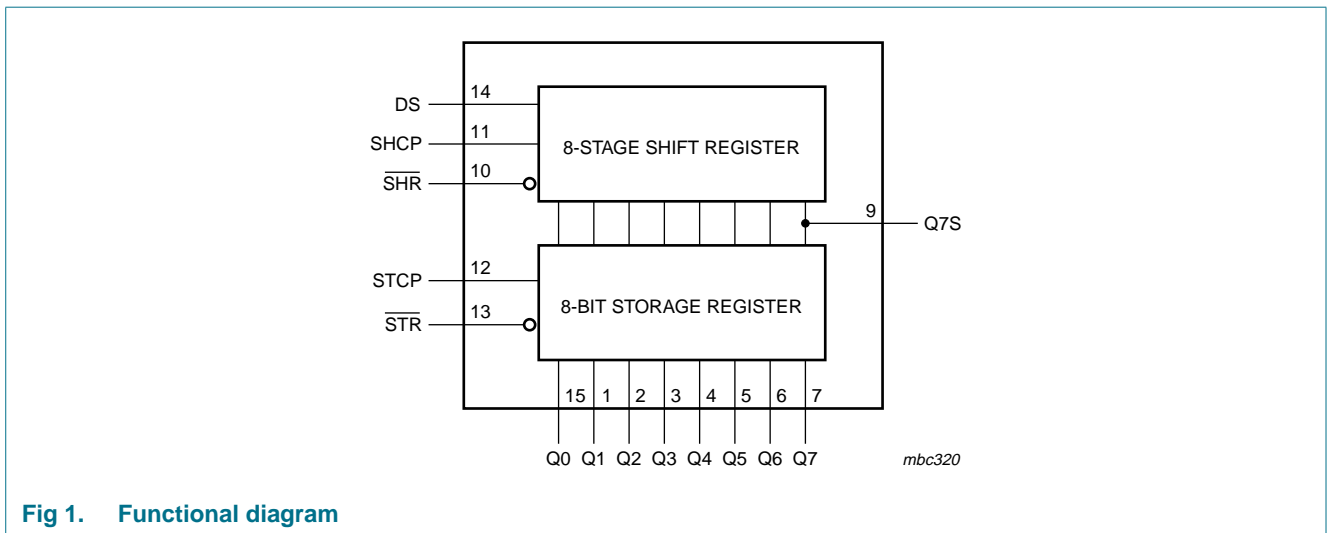


Fig 1. Functional diagram

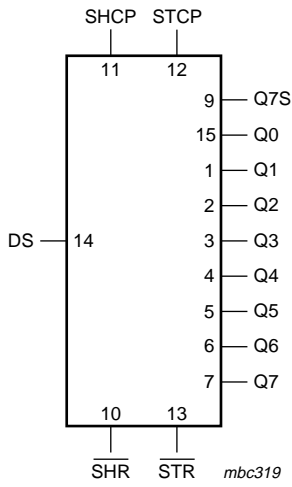


Fig 2. Logic symbol

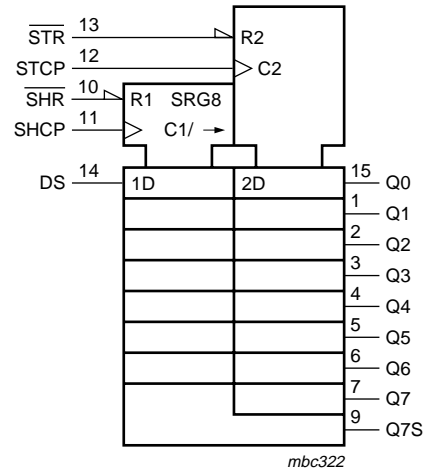


Fig 3. IEC logic symbol

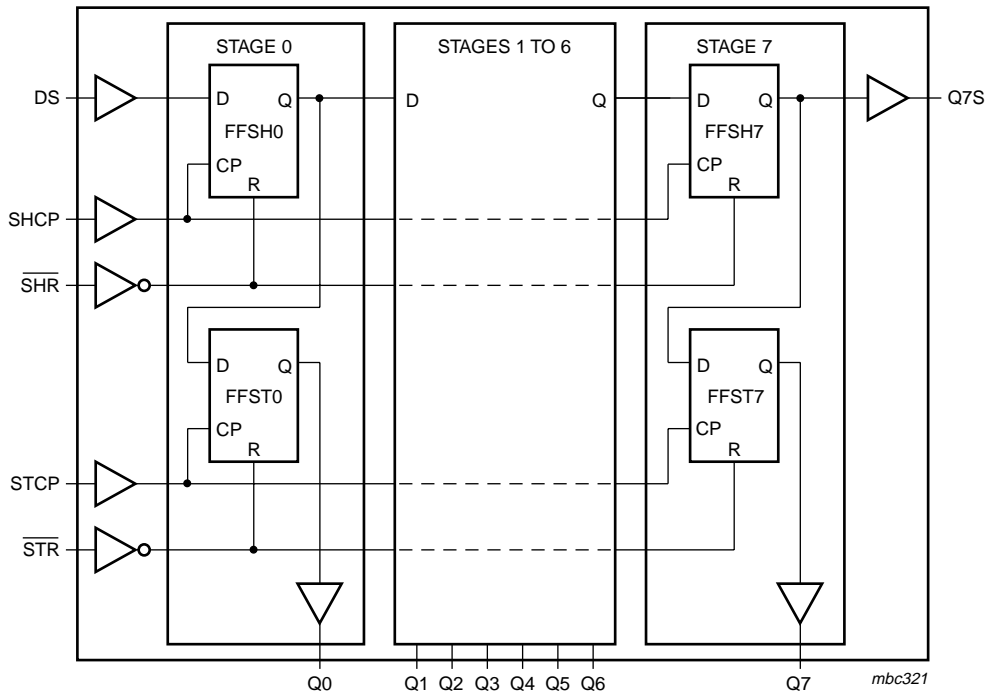


Fig 4. Logic diagram

6. Pinning information

6.1 Pinning

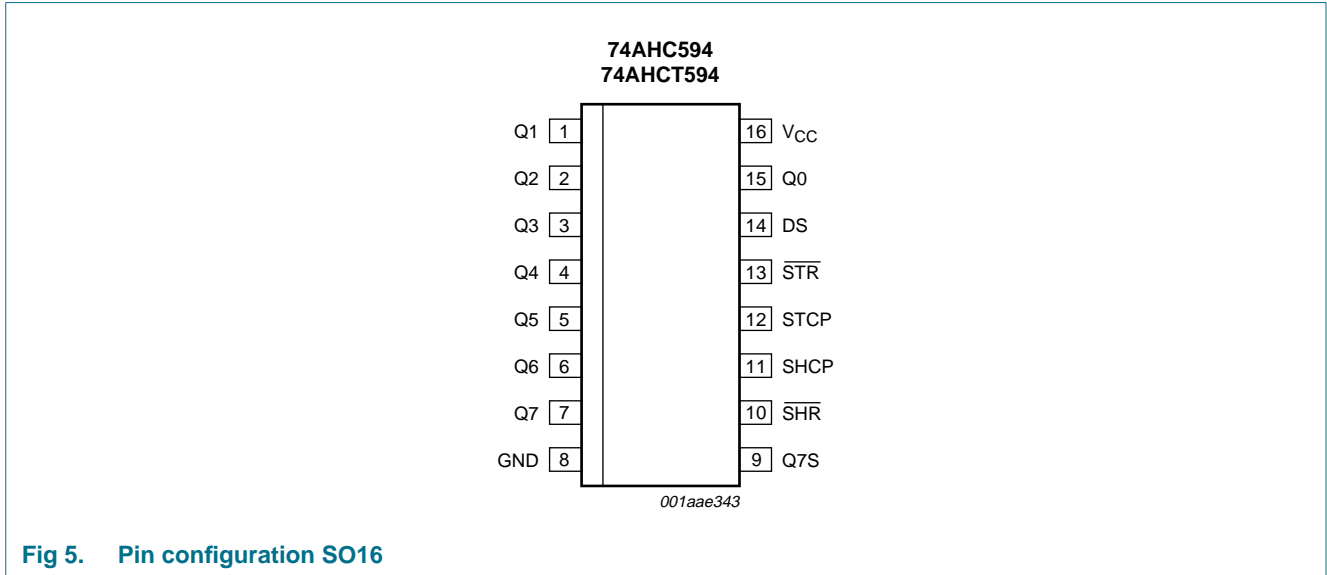


Fig 5. Pin configuration SO16

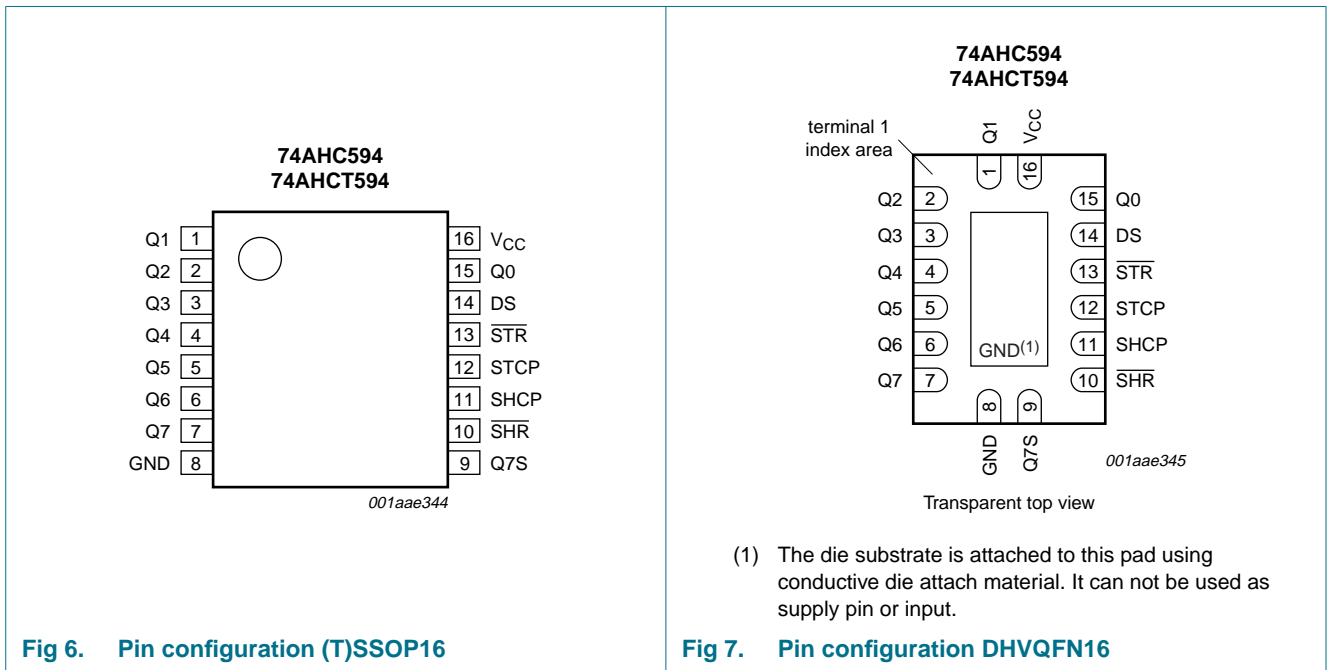
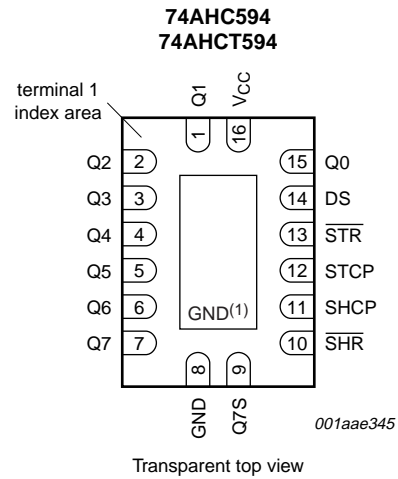


Fig 6. Pin configuration (T)SSOP16



- (1) The die substrate is attached to this pad using conductive die attach material. It can not be used as supply pin or input.

Fig 7. Pin configuration DHVQFN16

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
Q1	1	parallel data output
Q2	2	parallel data output
Q3	3	parallel data output
Q4	4	parallel data output
Q5	5	parallel data output
Q6	6	parallel data output
Q7	7	parallel data output
GND	8	ground (0 V)
Q7S	9	serial data output
$\overline{\text{SHR}}$	10	shift register reset input (active LOW)
SHCP	11	shift register clock input
STCP	12	storage register clock input
$\overline{\text{STR}}$	13	storage register reset input (active LOW)
DS	14	serial data input
Q0	15	parallel data output
V _{CC}	16	supply voltage

7. Functional description

Table 3. Function table^[1]

Input					Output		Function
SHCP	STCP	$\overline{\text{SHR}}$	$\overline{\text{STR}}$	DS	Q7S	Qn	
X	X	L	X	X	L	NC	a LOW-state on $\overline{\text{SHR}}$ only affects the shift register
X	X	X	L	X	NC	L	a LOW-state on $\overline{\text{STR}}$ only affects the storage register
X	↑	L	H	X	L	L	empty shift register loaded into storage register
↑	X	H	X	H	Q6S	NC	logic HIGH level shifted into shift register stage 0. Contents of all shift register stages shifted through, e.g. previous state of stage 6 (internal Q6S) appears on the serial output (Q7S).
X	↑	H	H	X	NC	QnS	contents of shift register stages (internal QnS) are transferred to the storage register and parallel output stages
↑	↑	H	H	X	Q6S	QnS	contents of shift register shifted through; previous contents of the shift register is transferred to the storage register and the parallel output stages

[1] H = HIGH voltage state;
 L = LOW voltage state;
 ↑ = LOW to HIGH transition;
 X = don't care;
 NC = no change;

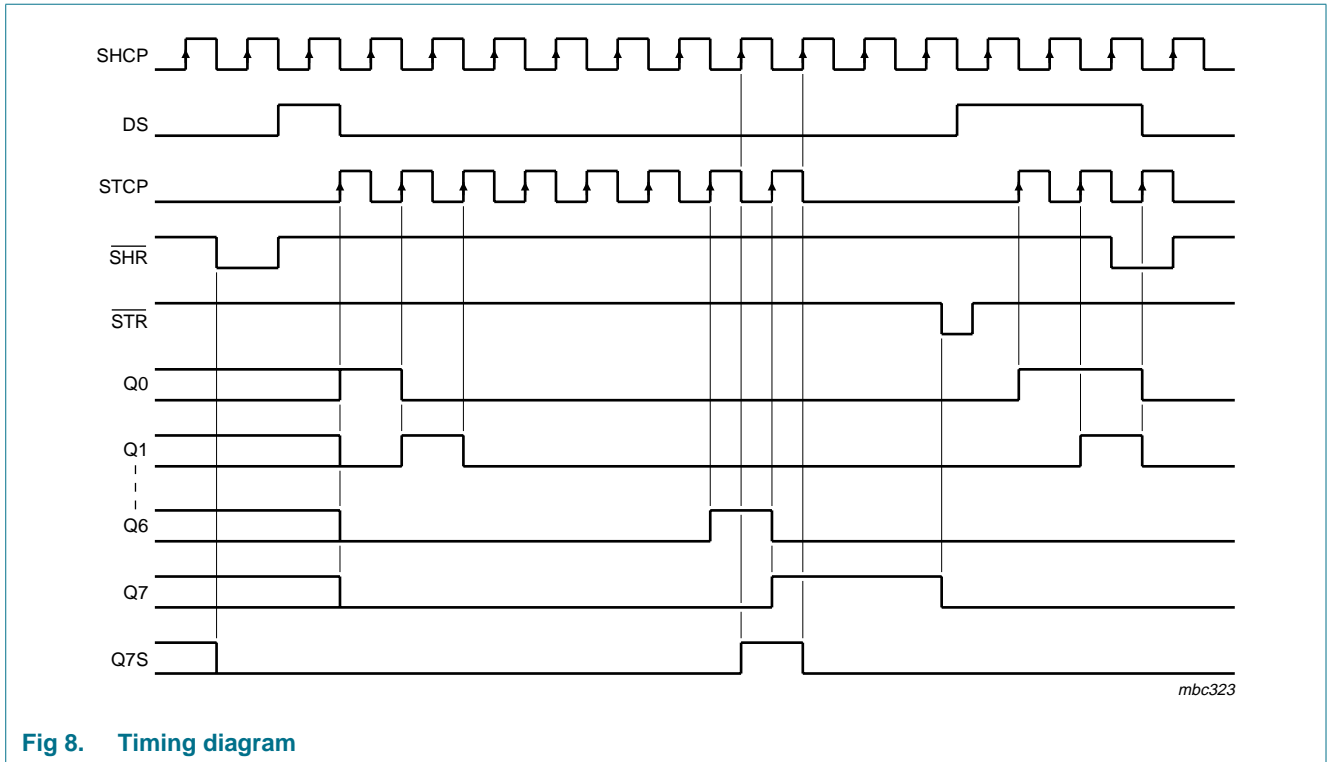


Fig 8. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage		-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V	[1] -20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1] -20	+20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5)$ V	-25	+25	mA
I_{CC}	supply current		-	+75	mA
I_{GND}	ground current		-75	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO16 packages: above 70 °C the value of P_{tot} derates linearly at 8 mW/K.
 For (T)SSOP16 packages: above 60 °C the value of P_{tot} derates linearly at 5.5 mW/K.
 For DHVQFN16 packages: above 60 °C the value of P_{tot} derates linearly at 4.5 mW/K.

9. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
74AHC594						
V_{CC}	supply voltage		2.0	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	100	ns/V
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V
74AHCT594						
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	-	-	20	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC594										
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.5	-	-	1.5	-	1.5	-	V
		$V_{CC} = 3.0\text{ V}$	2.1	-	-	2.1	-	2.1	-	V
		$V_{CC} = 5.5\text{ V}$	3.85	-	-	3.85	-	3.85	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	-	0.5	-	0.5	-	0.5	V
		$V_{CC} = 3.0\text{ V}$	-	-	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	-	1.65	-	1.65	-	1.65	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	2.9	3.0	-	2.9	-	2.9	-	V
		$I_O = -50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 3.0\text{ V}$	2.58	-	-	2.48	-	2.40	-	V
	$I_O = -8.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.94	-	-	3.80	-	3.70	-	V	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 50\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 3.0\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 50\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.1	-	0.1	-	0.1	V
		$I_O = 4\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.36	-	0.44	-	0.55	V
	$I_O = 8\text{ mA}; V_{CC} = 4.5\text{ V}$	-	-	0.36	-	0.44	-	0.55	V	

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF

74AHCT594

V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	4.0	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	

74AHC594

t _{PLH}	LOW to HIGH propagation delay	SHCP to Q7S; see Figure 9								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.2	8.5	2.2	9.7	2.2	10.6	ns
		C _L = 50 pF	-	7.4	11.5	3.0	13.2	3.0	14.3	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.8	6.3	1.7	7.2	1.7	7.8	ns
		C _L = 50 pF	-	4.8	8.0	2.4	9.1	2.4	10.0	ns

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	STCP to Qn; see Figure 10								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.1	8.3	2.3	9.5	2.3	10.6	ns
		C _L = 50 pF	-	7.3	11.9	3.3	13.6	3.3	14.7	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.5	5.7	1.8	6.5	1.8	7.1	ns
		C _L = 50 pF	-	4.8	7.8	2.6	9.0	2.6	9.8	ns
		SHCP to Q7S; see Figure 9								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.5	8.9	2.3	10.2	2.3	11.0	ns
		C _L = 50 pF	-	7.4	12.1	3.0	13.9	3.0	15.1	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	4.1	6.7	1.9	7.6	1.9	8.2	ns
		C _L = 50 pF	-	5.4	8.8	2.5	10.1	2.5	11.0	ns
		STCP to Qn; see Figure 10								
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	5.5	9.1	2.4	10.4	2.4	11.3	ns
		C _L = 50 pF	-	7.3	12.0	3.2	13.8	3.2	15.0	ns
V _{CC} = 4.5 V to 5.5 V										
C _L = 15 pF	-	3.7	6.0	1.9	6.9	1.9	7.5	ns		
C _L = 50 pF	-	5.2	8.5	2.6	9.7	2.6	10.5	ns		
SHR to Q7S; see Figure 13										
V _{CC} = 3.0 V to 3.6 V										
C _L = 15 pF	-	5.7	9.5	2.3	10.8	2.3	11.7	ns		
C _L = 50 pF	-	7.5	12.2	3.6	14.0	3.6	15.2	ns		
V _{CC} = 4.5 V to 5.5 V										
C _L = 15 pF	-	4.1	6.7	2.0	7.6	2.0	8.2	ns		
C _L = 50 pF	-	5.4	8.8	2.8	10.1	2.8	11.0	ns		
STR to Qn; see Figure 14										
V _{CC} = 3.0 V to 3.6 V										
C _L = 15 pF	-	5.8	9.6	2.8	11.0	2.8	12.0	ns		
C _L = 50 pF	-	7.7	12.5	3.8	14.4	3.8	15.6	ns		
V _{CC} = 4.5 V to 5.5 V										
C _L = 15 pF	-	4.1	7.2	2.2	8.2	2.2	8.9	ns		
C _L = 50 pF	-	5.4	9.4	3.0	10.7	3.0	11.6	ns		
f _{max}	maximum frequency	SHCP or STCP; see Figure 9 and 10								
		V _{CC} = 3.0 V to 3.6 V	80	125	-	70	-	65	-	MHz
		V _{CC} = 4.5 V to 5.5 V	90	170	-	80	-	70	-	MHz

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit	
			Min	Typ ^[1]	Max	Min	Max	Min	Max		
t _W	pulse width	SHCP and STCP HIGH or LOW; see Figure 9 and 10									
		V _{CC} = 3.0 V to 3.6 V	6.0	-	-	6.5	-	7.0	-	ns	
		V _{CC} = 4.5 V to 5.5 V	5.5	-	-	6.0	-	6.5	-	ns	
		SHR and STR HIGH or LOW; see Figure 13 and 14									
		V _{CC} = 3.0 V to 3.6 V	5.0	-	-	5.0	-	5.5	-	ns	
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.2	-	5.7	-	ns	
t _{su}	set-up time	DS to SHCP; see Figure 11									
		V _{CC} = 3.0 V to 3.6 V	3.5	-	-	3.5	-	4.0	-	ns	
		V _{CC} = 4.5 V to 5.5 V	3.0	-	-	3.0	-	3.5	-	ns	
		SHR to STCP; see Figure 12									
		V _{CC} = 3.0 V to 3.6 V	8.0	-	-	9.0	-	9.5	-	ns	
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.5	-	ns	
		SHCP to STCP; see Figure 10									
		V _{CC} = 3.0 V to 3.6 V	8.0	-	-	8.5	-	9.0	-	ns	
V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.5	-	ns			
t _h	hold time	DS to SHCP; see Figure 11									
		V _{CC} = 3.0 V to 3.6 V	1.5	-	-	1.5	-	2.0	-	ns	
		V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.5	-	ns	
t _{rec}	recovery time	SHR to SHCP; see Figure 13									
		V _{CC} = 3.0 V to 3.6 V	4.2	-	-	4.8	-	5.3	-	ns	
		V _{CC} = 4.5 V to 5.5 V	2.9	-	-	3.3	-	3.8	-	ns	
		STR to STCP; see Figure 14									
		V _{CC} = 3.0 V to 3.6 V	4.6	-	-	5.3	-	5.8	-	ns	
		V _{CC} = 4.5 V to 5.5 V	3.2	-	-	3.7	-	4.3	-	ns	
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [2]	-	55	-	-	-	-	-	pF	

74AHCT594; V_{CC} = 4.5 V to 5.5 V

t _{PLH}	LOW to HIGH propagation delay	SHCP to Q7S; see Figure 9									
		C _L = 15 pF	-	3.8	6.3	1.7	7.2	1.7	7.8	ns	
		C _L = 50 pF	-	4.8	8.0	2.2	9.1	2.2	9.9	ns	
		STCP to Qn; see Figure 10									
		C _L = 15 pF	-	3.5	5.7	1.8	6.5	1.8	7.1	ns	
		C _L = 50 pF	-	4.6	7.7	2.6	8.8	2.6	9.6	ns	

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); for test circuit see [Figure 15](#).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	Min	Max	
t _{PHL}	HIGH to LOW propagation delay	SHCP to Q7S; see Figure 9								
		C _L = 15 pF	-	4.1	6.7	1.8	7.6	1.8	8.3	ns
		C _L = 50 pF	-	5.4	8.8	2.4	10.1	2.4	11.0	ns
		STCP to Qn; see Figure 10								
		C _L = 15 pF	-	3.7	6.1	1.9	6.9	1.9	7.2	ns
		C _L = 50 pF	-	5.2	8.5	2.6	9.7	2.6	10.5	ns
		SHR to Q7S; see Figure 13								
		C _L = 15 pF	-	4.3	7.0	2.4	8.0	2.4	8.7	ns
		C _L = 50 pF	-	5.4	8.8	2.7	10.1	2.7	11.0	ns
t _{max}	maximum frequency	STR to Qn; see Figure 14								
		C _L = 15 pF	-	4.5	7.4	2.3	8.4	2.3	9.2	ns
		C _L = 50 pF	-	5.7	9.4	3.1	10.7	3.1	11.7	ns
f _{max}	maximum frequency	SHCP or STCP; see Figure 9 and 10	90	160	-	80	-	70	-	MHz
		t _W	pulse width	SHCP and STCP HIGH or LOW; see Figure 9 and 10	5.5	-	-	6.0	-	6.5
	SHR and STR HIGH or LOW; see Figure 13 and 14	5.2		-	-	5.5	-	6.0	-	ns
t _{su}	set-up time	DS to SHCP; see Figure 11	3.0	-	-	3.0	-	3.5	-	ns
		SHR to STCP; see Figure 12	5.0	-	-	5.0	-	5.5	-	ns
		SHCP to STCP; see Figure 10	5.0	-	-	5.0	-	5.5	-	ns
t _h	hold time	DS to SHCP; see Figure 11	2.0	-	-	2.0	-	2.5	-	ns
t _{rec}	recovery time	SHR to SHCP; see Figure 13	2.9	-	-	3.3	-	3.8	-	ns
		STR to STCP; see Figure 14	3.4	-	-	3.8	-	4.3	-	ns
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} ^[2]	-	55	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

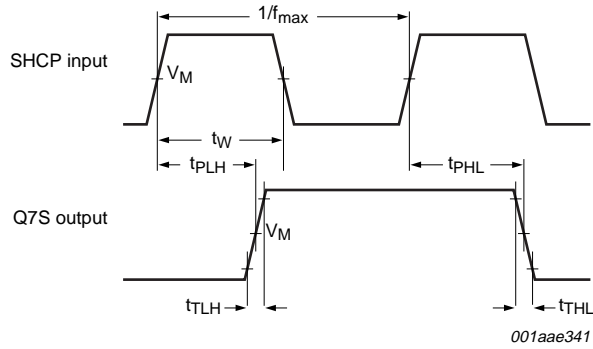
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

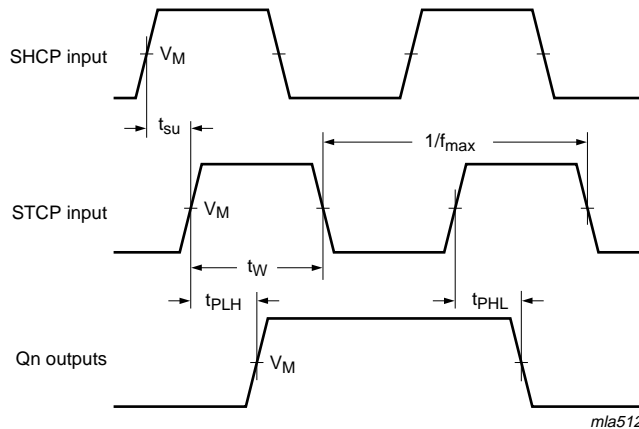
Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

12. Waveforms



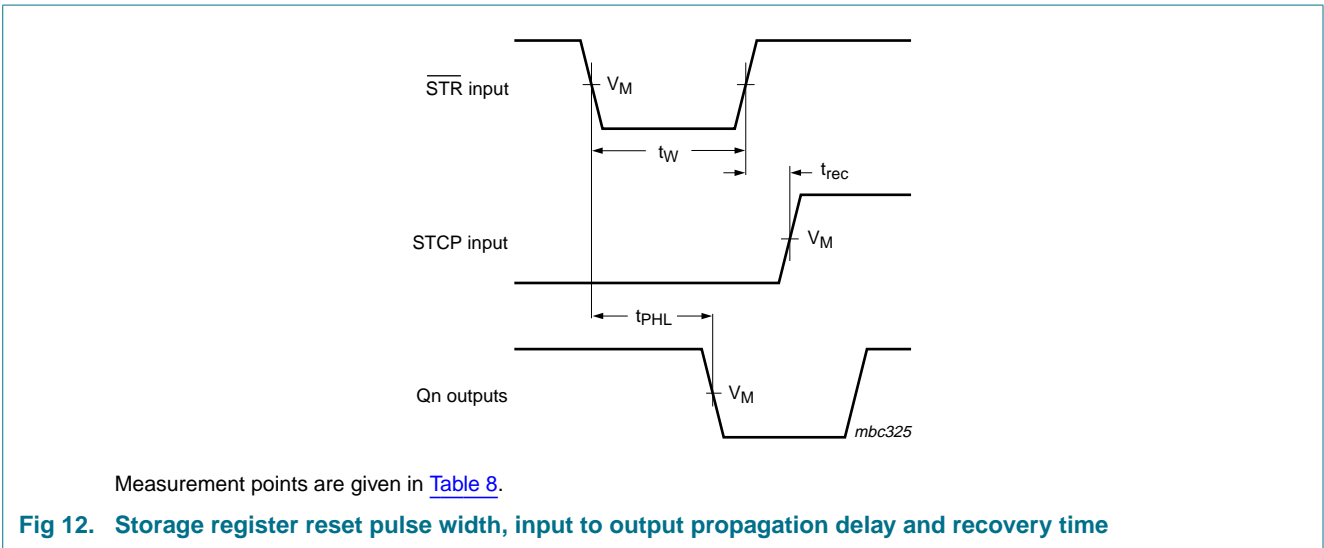
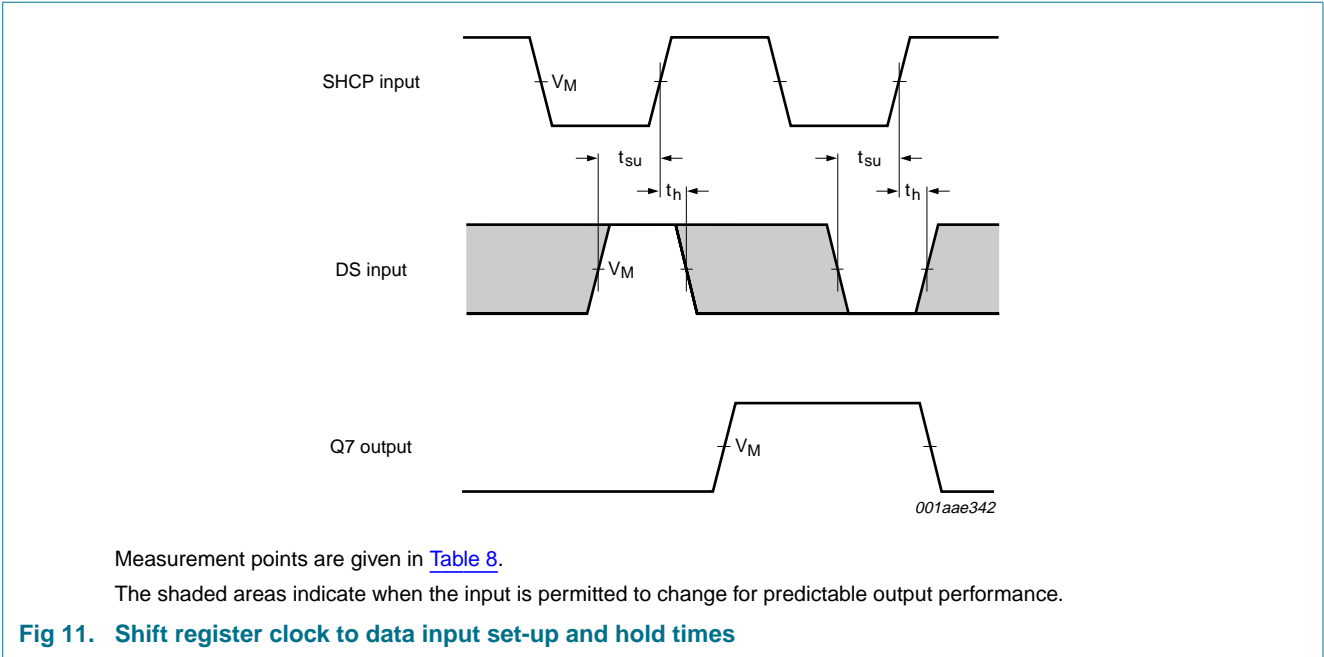
Measurement points are given in [Table 8](#).

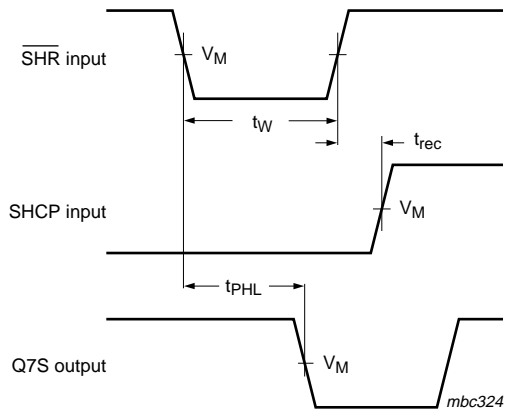
Fig 9. Shift register clock pulse width, maximum frequency and input to output propagation delays



Measurement points are given in [Table 8](#).

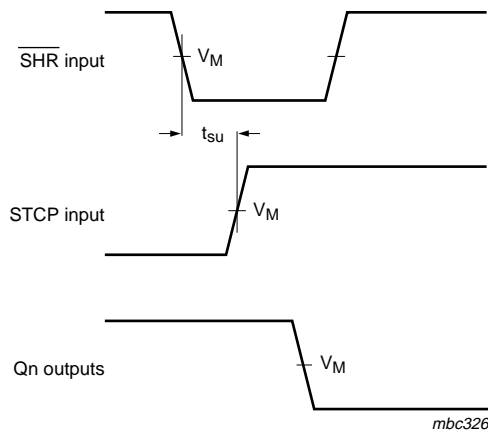
Fig 10. Shift register clock to storage register clock set-up time and storage clock pulse width, maximum frequency and input to output propagation delays





Measurement points are given in [Table 8](#).

Fig 13. Shift register reset pulse width, input to output propagation delay and recovery time

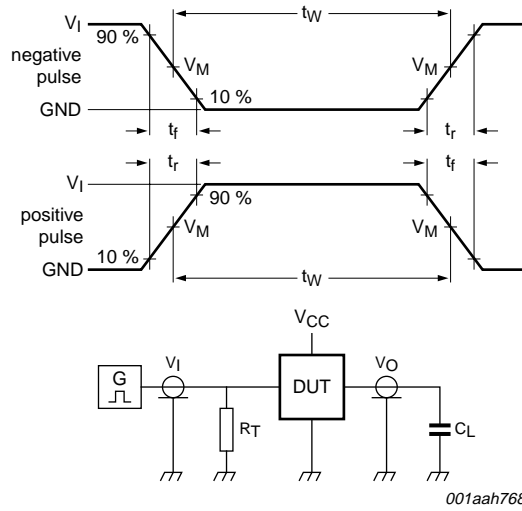


Measurement points are given in [Table 8](#).

Fig 14. Shift register reset to storage register clock set-up time

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74AHC594	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74AHCT594	1.5 V	$0.5 \times V_{CC}$



For test data see [Table 9](#).

Definitions for test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

Fig 15. Load circuitry for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC594	V_{CC}	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74AHCT594	3.0 V	≤ 3.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

13. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

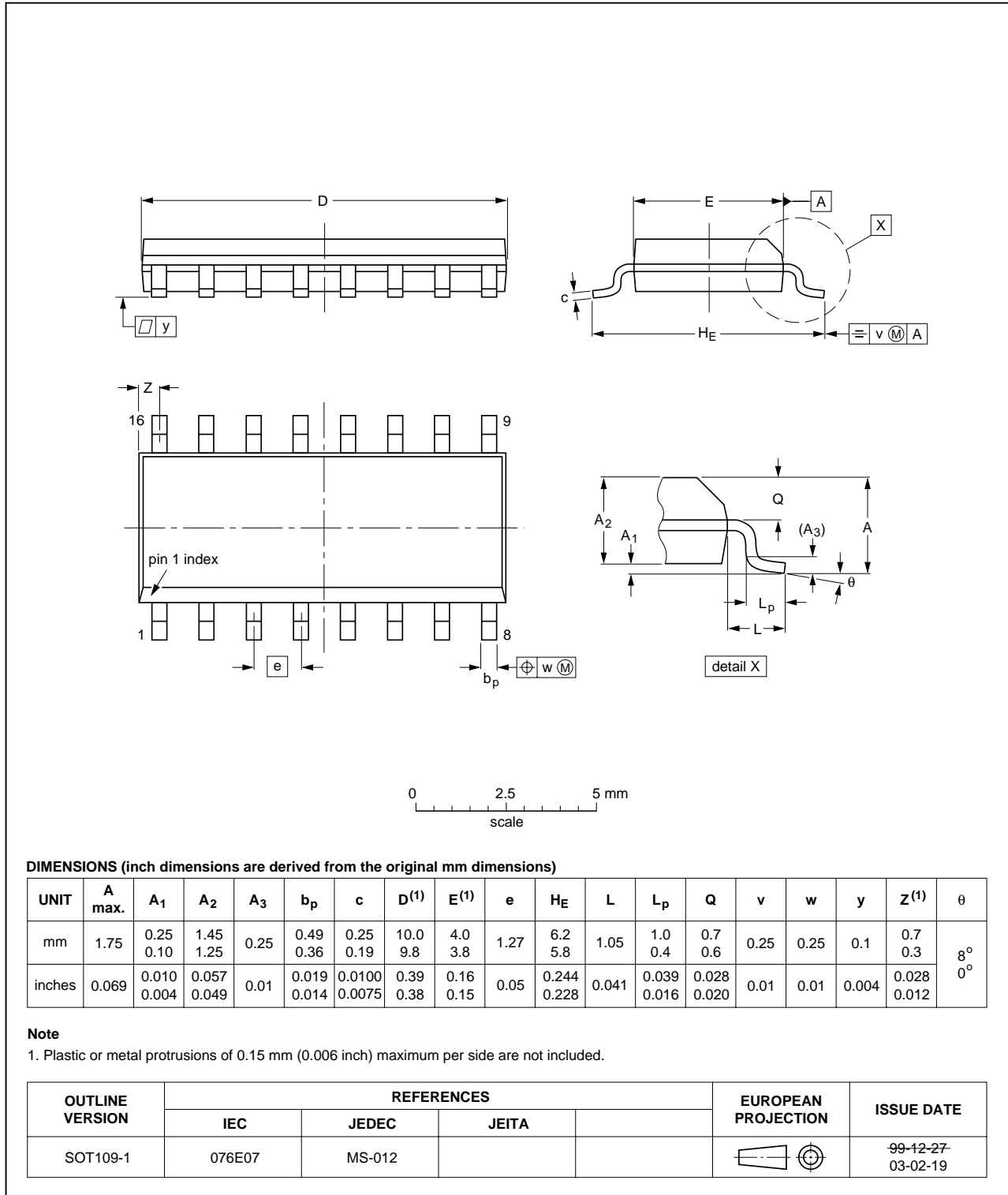


Fig 16. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

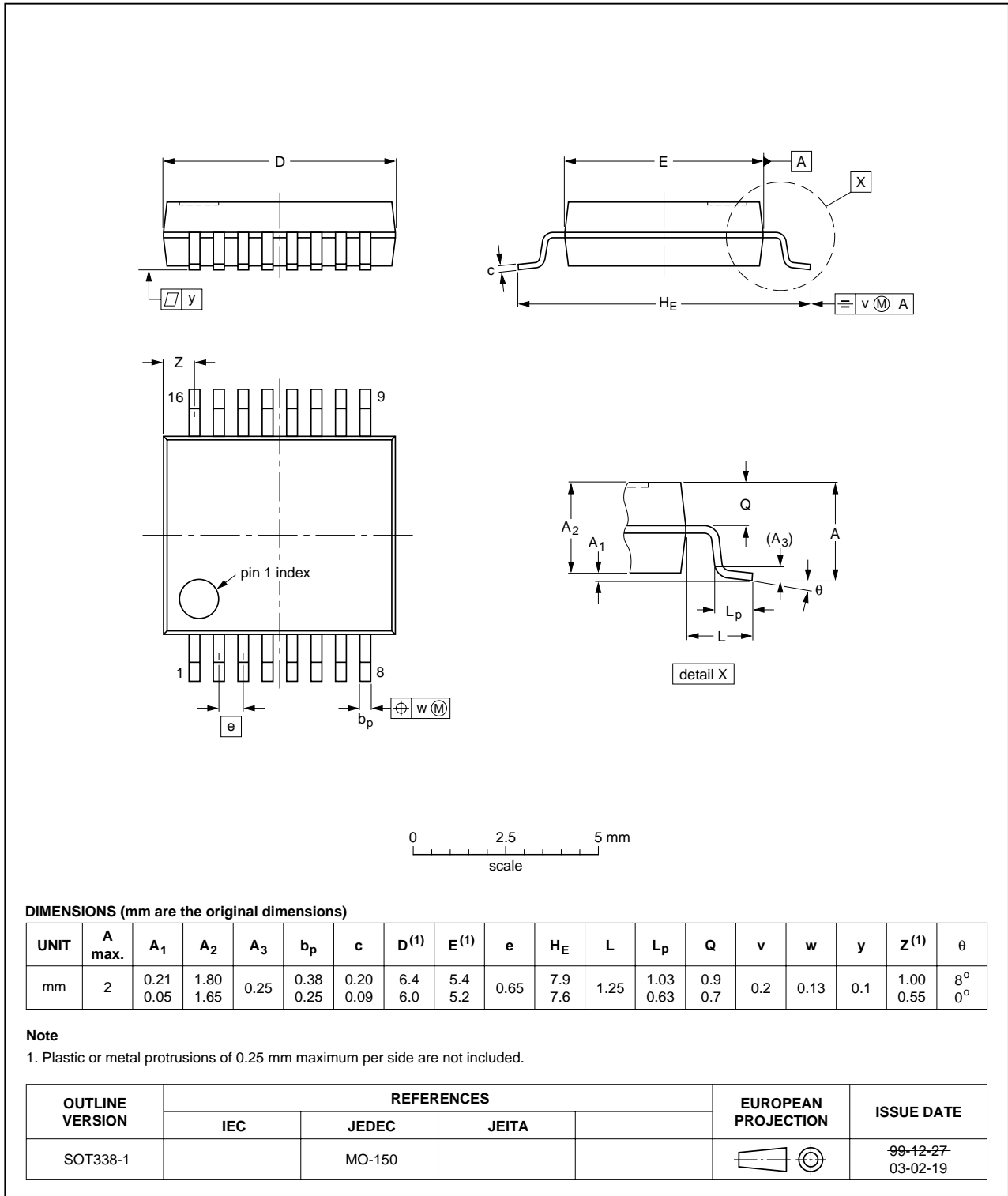


Fig 17. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

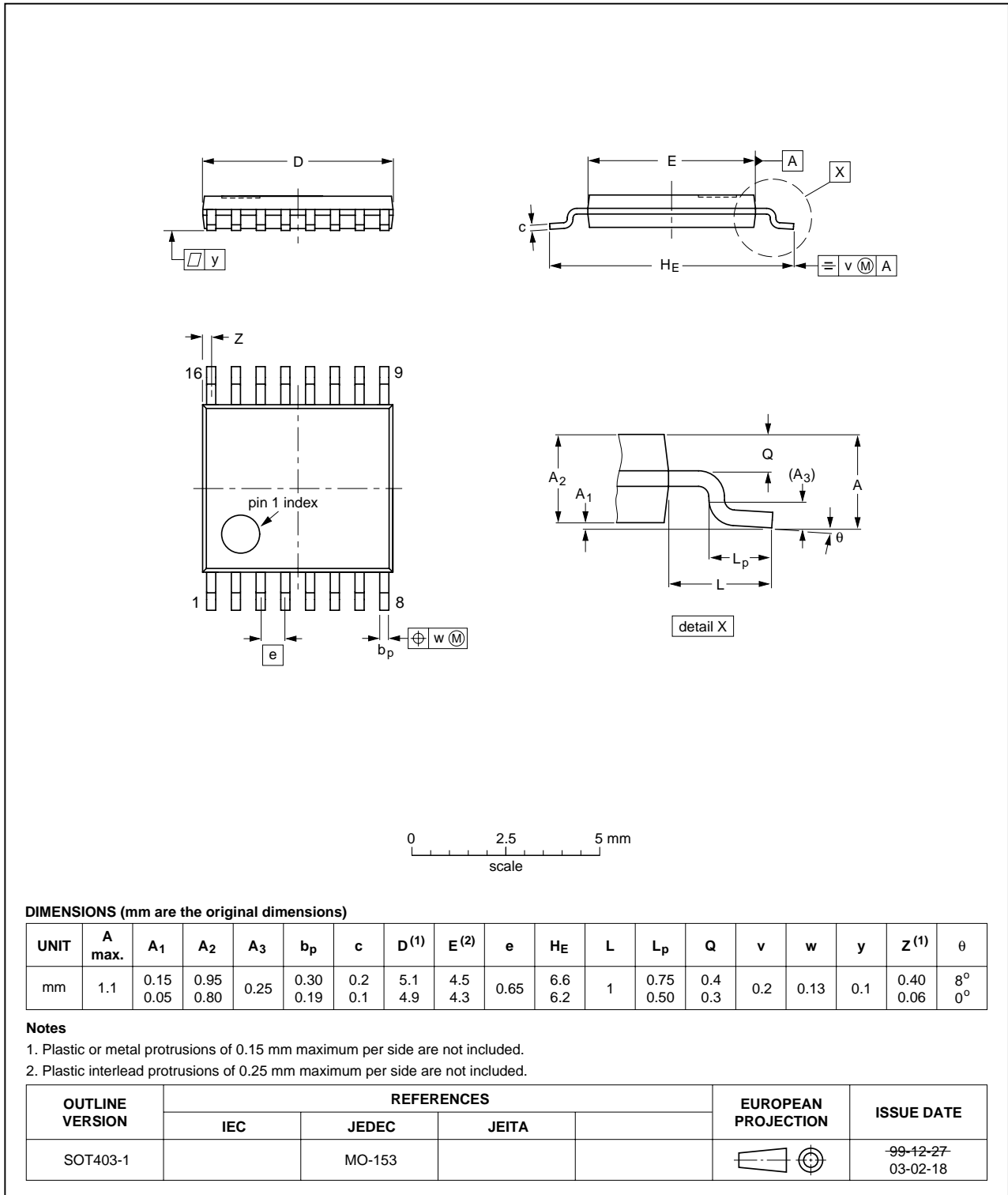


Fig 18. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

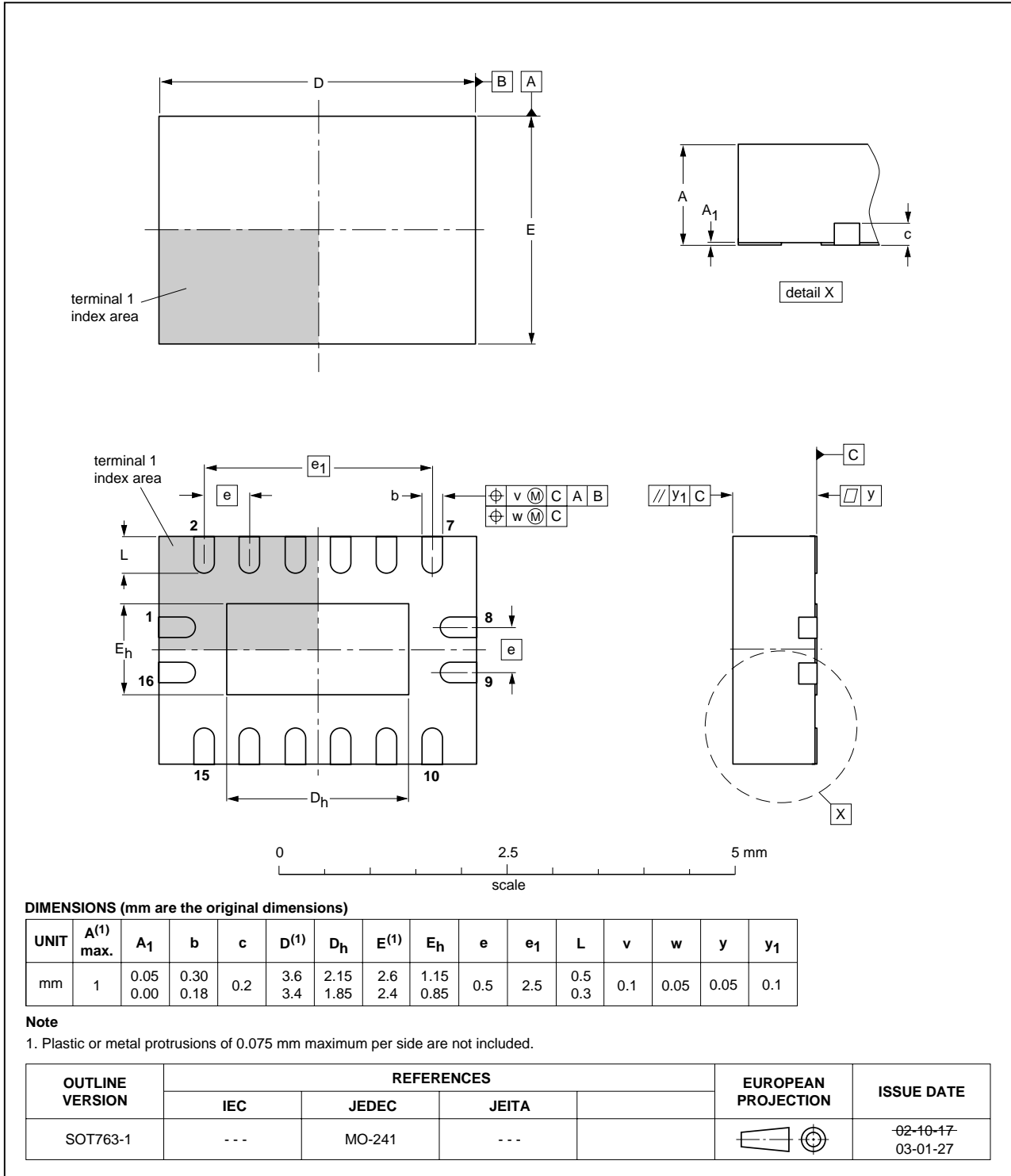


Fig 19. Package outline SOT763-1 (DHVQFN16)

14. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

15. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT594_2	20080609	Product data sheet	-	74AHC_AHCT594_1
Modifications:	<ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 6: the conditions for input leakage current have been changed. 			
74AHC_AHCT594_1	20060704	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

16.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

18. Contents

1	General description	1
2	Features	1
3	Applications	1
4	Ordering information	2
5	Functional diagram	2
6	Pinning information	4
6.1	Pinning	4
6.2	Pin description	5
7	Functional description	5
8	Limiting values	6
9	Recommended operating conditions	7
10	Static characteristics	7
11	Dynamic characteristics	8
12	Waveforms	12
13	Package outline	16
14	Abbreviations	20
15	Revision history	20
16	Legal information	21
16.1	Data sheet status	21
16.2	Definitions	21
16.3	Disclaimers	21
16.4	Trademarks	21
17	Contact information	21
18	Contents	22

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.



© NXP B.V. 2008.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 9 June 2008

Document identifier: 74AHC_AHCT594_2