

# Am29C827/Am29C828 Am29C927/Am29C928

High-Performance CMOS Bus Buffers

Am29C827/Am29C828  
Am29C927/Am29C928

## DISTINCTIVE CHARACTERISTICS

- High-speed CMOS buffers and inverters
  - D-Y delay = 7 ns typical
- Low standby power
- JEDEC FCT-compatible specs
- $I_{OL} = 24$  mA, Commercial and Military
- 200-mV typical hysteresis on data input ports
- Am29C900 DIP pinout option reduces lead inductance on  $V_{CC}$  and GND pins

## GENERAL DESCRIPTION

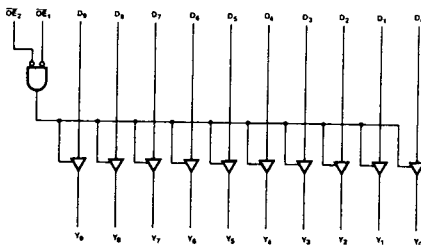
The Am29C827 and Am29C828 CMOS Bus Buffers provide high-performance bus interface buffering for wide address/data paths or buses carrying parity. Both devices feature 10-bit wide data paths and NORed output enables for maximum control flexibility. The Am29C827 has non-inverting outputs, while the Am29C828 has inverting outputs. Each device has data inputs with 200-mV typical input hysteresis to provide improved noise immunity. The Am29C827 and Am29C828 are produced with AMD's exclusive CS-11 CMOS process, and feature typical propa-

gation delays of 7 ns, as well as an output current drive of 24 mA.

The Am29C827 and Am29C828 are available in the standard package options: DIPs, PLCCs, LCCs, SOICs, and Flatpacks. In addition, a DIP pinout option, featuring center  $V_{CC}$  and GND pins, reduces the lead inductance of the  $V_{CC}$  and GND pins. The ordering part numbers for CMOS buffers with this pinout are the Am29C927 and Am29C928; their pinouts are shown later in this data sheet.

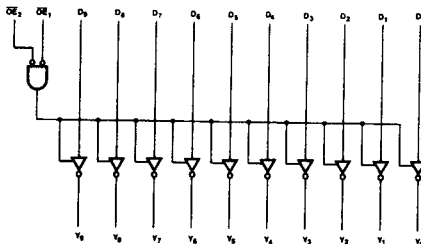
## BLOCK DIAGRAMS

### Am29C827 (Noninverting)



BD001092

### Am29C828 (Inverting)

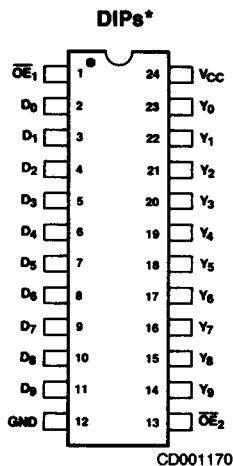
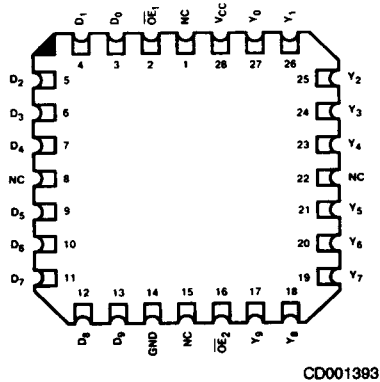
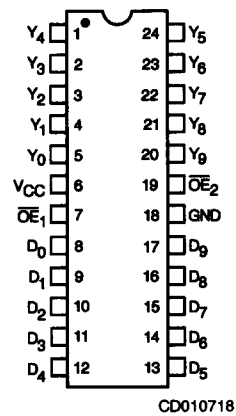


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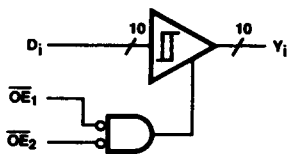
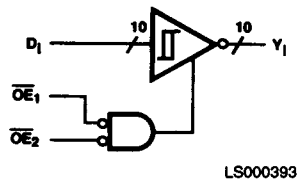
## CONNECTION DIAGRAMS Top View

 Am29C827/Am29C828  
Am29C927/Am29C928

**Am29C827/Am29C828**

**LCC\*\***

**Am29C927/  
Am29C928**
**DIPs**


\*Also available in 24-Pin Flatpack and Small Outline packages; pinout identical to DIPs.  
\*\*Also available in 28-Pin PLCC; pinout identical to LCC.

### LOGIC SYMBOLS

**Am29C827**

**Am29C828**


### FUNCTION TABLES

**Am29C827**

Inputs			Outputs	Function
OE <sub>1</sub>	OE <sub>2</sub>	D <sub>1</sub>	Y <sub>1</sub>	
L	L	H	H	Transparent
L	L	L	L	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

**Am29C828**

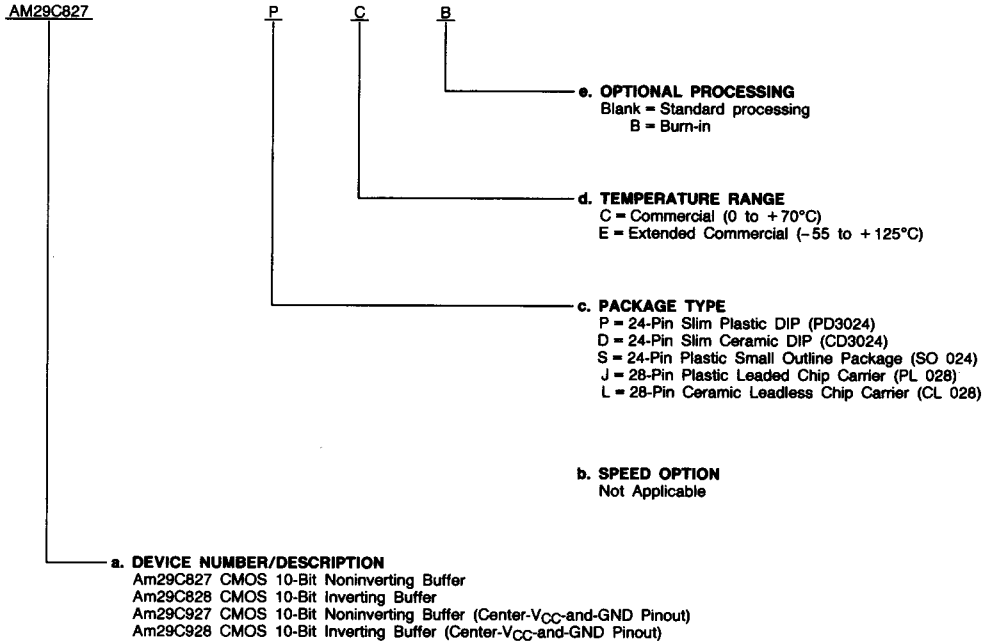
Inputs			Outputs	Function
OE <sub>1</sub>	OE <sub>2</sub>	D <sub>1</sub>	Y <sub>1</sub>	
L	L	H	L	Transparent
L	L	L	H	Transparent
X	H	X	Z	Hi-Z
H	X	X	Z	Hi-Z

H = HIGH  
L = LOW  
X = Don't Care  
Z = Hi-Z

## ORDERING INFORMATION Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Package Type**
- d. **Temperature Range**
- e. **Optional Processing**



Valid Combinations	
AM29C827	PC, PCB, DC, DCB,
AM29C828	DE, SC, JC, LC
AM29C927	PC, PCB, DC, DCB,
AM29C928	DE

### Valid Combinations

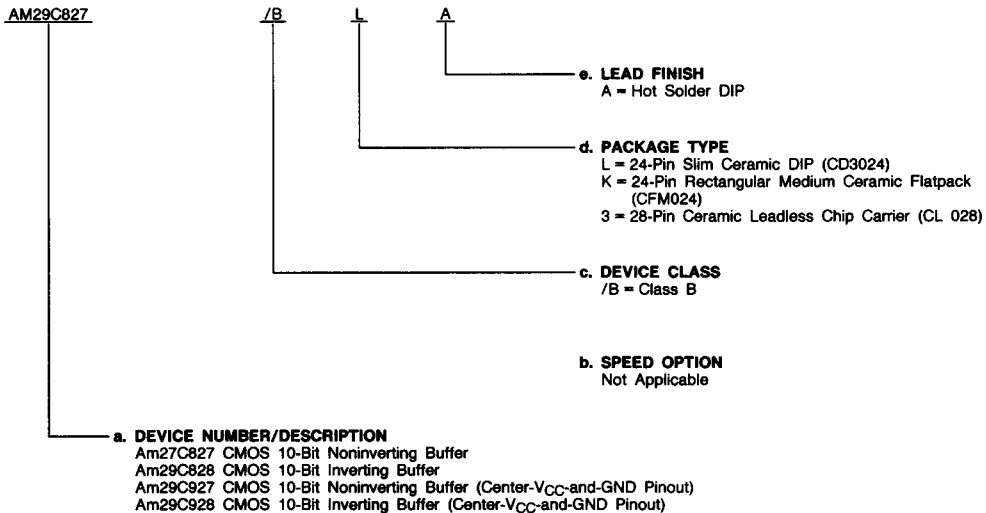
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

# ORDERING INFORMATION (Cont'd.)

## APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

- a. **Device Number**
- b. **Speed Option** (if applicable)
- c. **Device Class**
- d. **Package Type**
- e. **Lead Finish**



Valid Combinations	
AM29C827	/BLA, /BKA, /B3A
AM29C828	
AM29C927	/BLA
AM29C928	

### Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

### Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

## PIN DESCRIPTION

### $\overline{OE}_i$ Output Enables (Input, Active LOW)

When  $\overline{OE}_1$  and  $\overline{OE}_2$  are both LOW, the outputs are enabled. When either one or both are HIGH, the outputs are in the Hi-Z state.

### $D_i$ Data Inputs (Input)

$D_i$  are the 10-bit data inputs.

### $Y_i$ Data Output (Output)

$Y_i$  are the 10-bit data outputs.

**ABSOLUTE MAXIMUM RATINGS**

Storage Temperature .....	-65 to +150°C
Supply Voltage to Ground Potential	
Continuous .....	-0.5 V to +7.0 V
DC Output Voltage .....	-0.5 V to $V_{CC} + 0.5$ V
DC Input Voltage .....	-0.5 V to $V_{CC} + 0.5$ V
DC Output Diode Current: Into Output .....	+50 mA
Out of Output .....	-50 mA
DC Input Diode Current: Into Input .....	+20 mA
Out of Input .....	-20 mA
DC Output Current per Pin:	
$I_{SINK}$ .....	+48 mA ( $2 \times I_{OL}$ )
$I_{SOURCE}$ .....	-30 mA ( $2 \times I_{OH}$ )
Total DC Ground Current ( $n \times I_{OL} + m \times I_{CCT}$ ) mA (Note 1)	
Total DC $V_{CC}$ Current .... ( $n \times I_{OH} + m \times I_{CCT}$ ) mA (Note 1)	

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**OPERATING RANGES**

Commercial (C) Devices	
Temperature ( $T_A$ ) .....	0 to +70°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V
Military (M) and Extended Commercial (E) Devices	
Temperature ( $T_A$ ) .....	-55 to +125°C
Supply Voltage ( $V_{CC}$ ) .....	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

**DC CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Units
$V_{OH}$	Output HIGH Voltage	$V_{CC} = 4.5$ V $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15$ mA	2.4		Volts
$V_{OL}$	Output LOW Voltage	$V_{CC} = 4.5$ V $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 24$ mA		0.5	Volts
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs (Note 2)		2.0		Volts
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs (Note 2)			0.8	Volts
$V_I$	Input Clamp Voltage	$V_{CC} = 4.5$ V, $I_{IN} = -18$ mA			-1.2	Volts
$I_{IL}$	Input LOW Current	$V_{CC} = 5.5$ V, $V_{IN} = GND$			-10	$\mu$ A
		$V_{CC} = 5.5$ V, $V_{IN} = 0.4$ V			-5	
$I_{IH}$	Input HIGH Current	$V_{CC} = 5.5$ V, $V_{IN} = 2.7$ V			5	$\mu$ A
		$V_{CC} = 5.5$ V, $V_{IN} = 5.5$ V			10	
$I_{OZH}$	Output Off-State Current (High Impedance)	$V_{CC} = 5.5$ V, $V_O = 5.5$ V or 2.7 V (Note 3)			+10	$\mu$ A
$I_{OZL}$		$V_{CC} = 5.5$ V, $V_O = 0.4$ V or GND (Note 3)			-10	$\mu$ A
$I_{SC}$	Output Short-Circuit Current	$V_{CC} = 5.5$ V, $V_O = 0$ V (Note 4)		-60		mA
$I_{CCO}$	Static Supply Current	$V_{CC} = 5.5$ V Outputs Open	$V_{IN} = V_{CC}$ or GND	MIL	160	$\mu$ A
				COM'L	120	
$I_{CCT}$			$V_{IN} = 3.4$ V	Data Input	1.5	mA/Bit
				$\overline{OE}_1, \overline{OE}_2$	3.0	
$I_{CCD}^\dagger$	Dynamic Supply Current	$V_{CC} = 5.5$ V (Note 5)		275		$\mu$ A/MHz/ Bit

- Notes:**
1.  $n$  = number of outputs,  $m$  = number of inputs.
  2. Input thresholds are tested in combination with other DC parameters or by correlation.
  3. Off-state currents are only tested at worst-case conditions of  $V_{OUT} = 5.5$  V or 0.0 V.
  4. Not more than one output should be shorted at a time. Duration should not exceed 100 milliseconds.
  5. Measured at a frequency  $\leq 10$  MHz with 50% duty cycle.

$^\dagger$  Not included in Group A tests.

**SWITCHING CHARACTERISTICS** over operating range unless otherwise specified (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

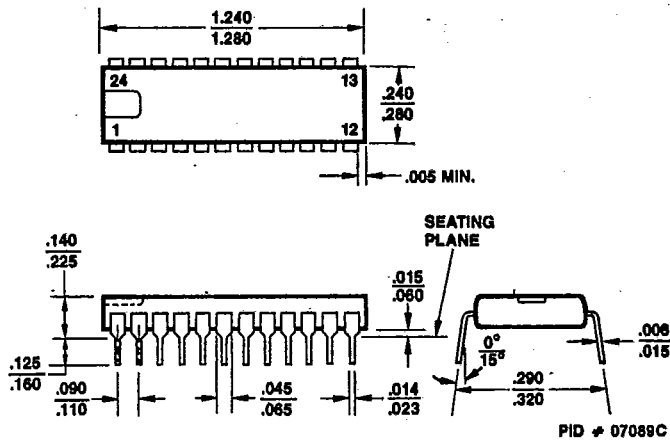
Parameter Symbol	Parameter Description	Test Conditions*	COMMERCIAL		MILITARY		Units
			Min.	Max.	Min.	Max.	
tPLH	Data (D <sub>i</sub> ) to Output (Y <sub>i</sub> ) Am29C827 (Noninverting)	C <sub>L</sub> = 50 pF R <sub>1</sub> = 500 Ω R <sub>2</sub> = 500 Ω		10		12	ns
tPHL				10		12	ns
tPLH	Data (D <sub>i</sub> ) to Output (Y <sub>i</sub> ) Am29C828 (Inverting)			10		12	ns
tPHL				10		12	ns
tZH	Output Enable Time $\overline{OE}$ to Y <sub>i</sub>			13		15	ns
tZL				13		15	ns
tHZ	Output Disable Time $\overline{OE}$ to Y <sub>i</sub>			13		15	ns
tLZ				13		15	ns

\*See Test Circuit and Waveforms.

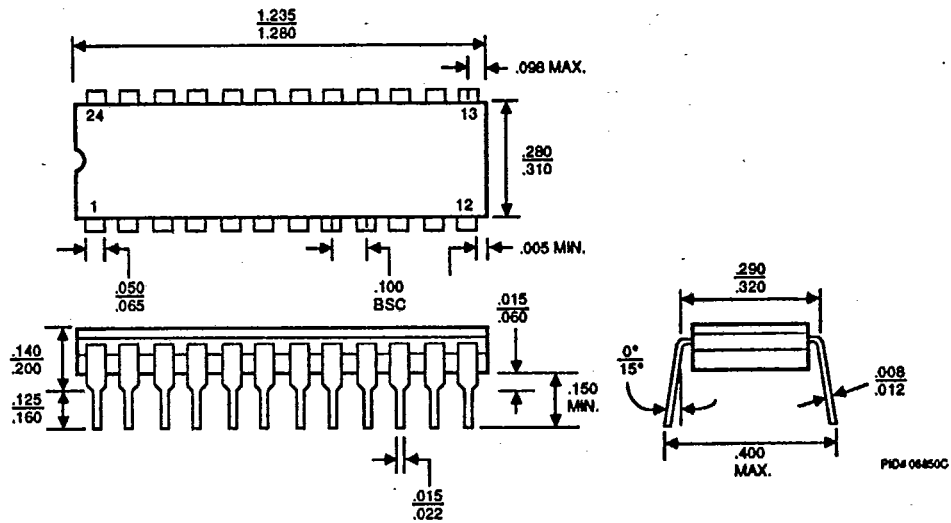
PACKAGE OUTLINES\*

T-90-20

PD3024



CD3024

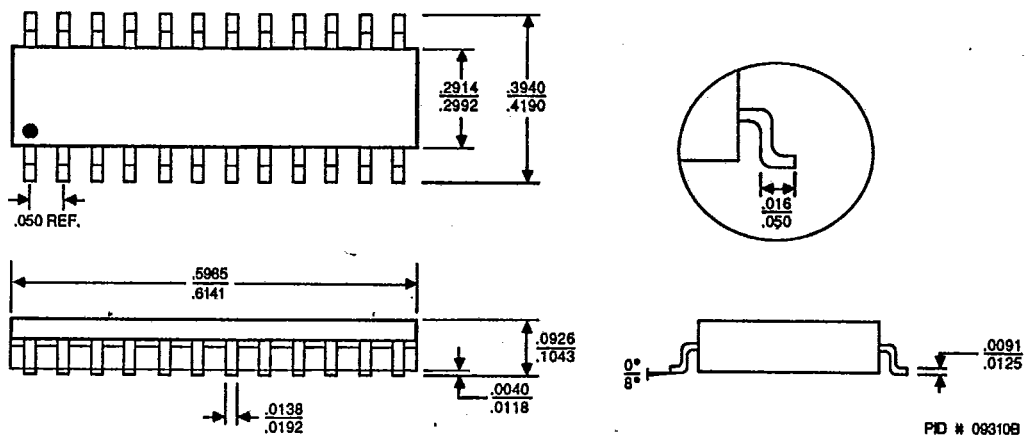


\*For reference only.

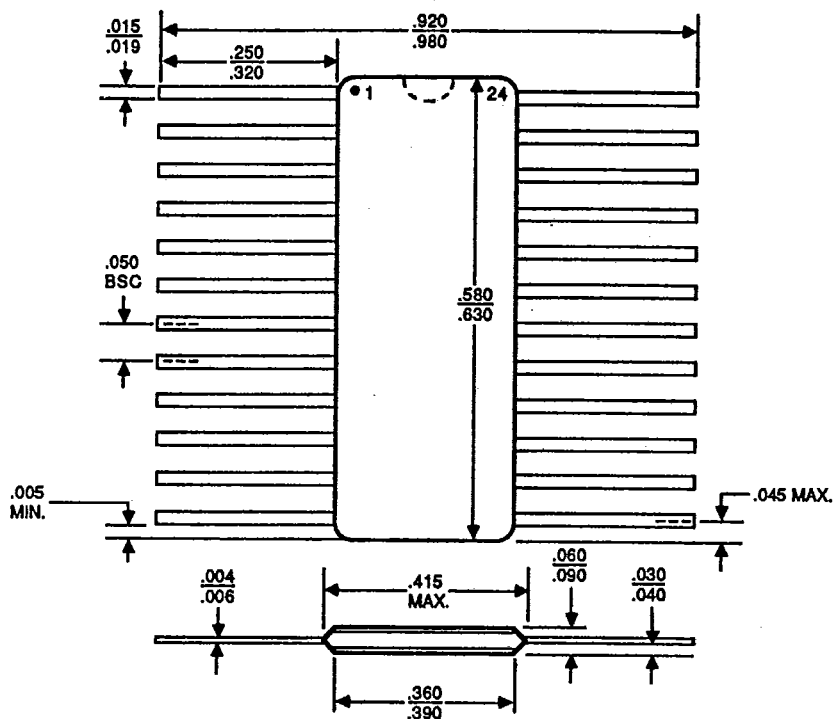
PACKAGE OUTLINES (Cont'd.)

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SO 024



CFM024

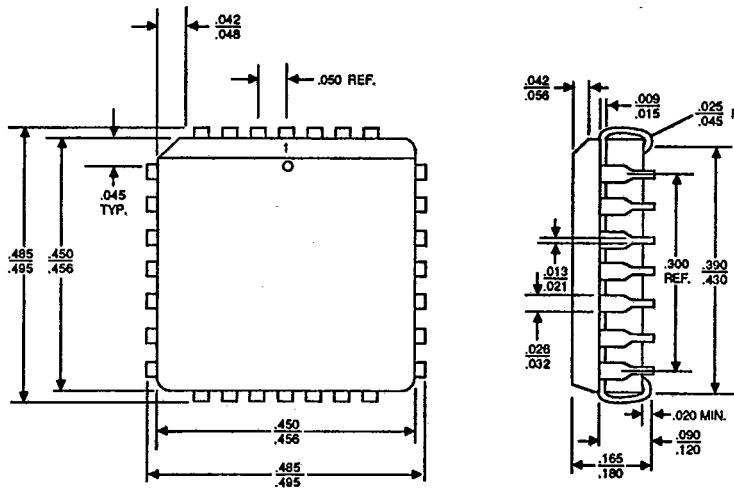




PACKAGE OUTLINES (Cont'd.)

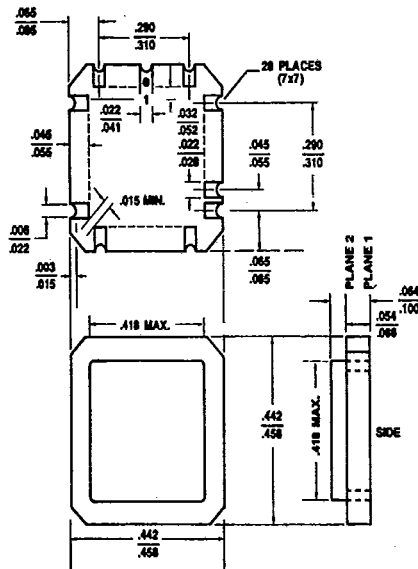
T-90-20

PL 028



PID # 06751E

CL 028



PID # 06595D

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