

# CD74HC165, CD74HCT165

## High Speed CMOS Logic 8-Bit Parallel-In/Serial-Out Shift Register

February 1998

### Features

- Buffered Inputs
- Asynchronous Parallel Load
- Complementary Outputs
- Typical  $f_{MAX} = 60\text{MHz}$  at  $V_{CC} = 5\text{V}$ ,  $C_L = 15\text{pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . .  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{V}$
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8\text{V}$  (Max),  $V_{IH} = 2\text{V}$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The Harris CD74HC165 and CD74HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs ( $Q_7$  and  $\overline{Q_7}$ ) available from the last stage. When the parallel load ( $\overline{PL}$ ) input is LOW, parallel data from the D0 to D7 inputs are loaded into the register asynchronously. When the  $\overline{PL}$  is HIGH, data enters the register serially at the DS input and shifts one place to the right ( $Q_0 \rightarrow Q_1 \rightarrow Q_2$ , etc.) with each positive-going clock transition. This feature allow parallel-to-serial converter expansion by typing the  $Q_7$  output to the DS input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of  $\overline{CE}$  should only take place while CP is HIGH. Also, CP and  $\overline{CE}$  should be LOW before the LOW-to-HIGH transition of PL to prevent shifting the data when  $\overline{PL}$  goes HIGH.

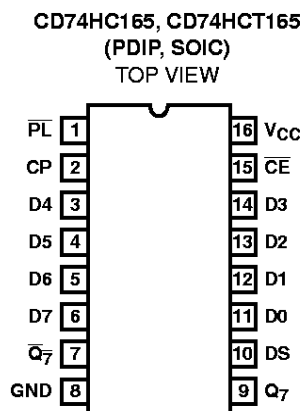
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74HC165E	-55 to 125	16 Ld PDIP	E16.3
CD74HCT165E	-55 to 125	16 Ld PDIP	E16.3
CD74HC165M	-55 to 125	16 Ld SOIC	M16.15
CD74HCT165M	-55 to 125	16 Ld SOIC	M16.15

### NOTES:

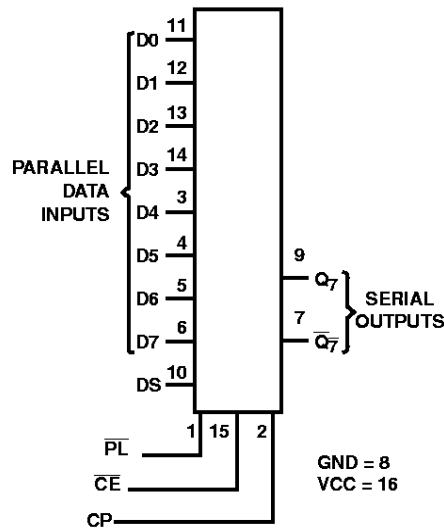
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout



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## Functional Diagram



TRUTH TABLE

OPERATING MODE	INPUTS					Q <sub>n</sub> REGISTER		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	DS	D0 - D7	Q <sub>0</sub>	Q <sub>1</sub> - Q <sub>6</sub>	Q <sub>7</sub>	$\overline{Q_7}$
Parallel Load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	↑	l	X	L	q <sub>0</sub> - q <sub>5</sub>	q <sub>6</sub>	$\overline{q_6}$
	H	L	↑	h	X	H	q <sub>0</sub> - q <sub>5</sub>	q <sub>6</sub>	$\overline{q_6}$
Hold Do Nothing	H	H	X	X	X	q <sub>0</sub>	q <sub>1</sub> - q <sub>6</sub>	q <sub>7</sub>	$\overline{q_7}$

NOTE:

- H = High Voltage Level
- h = High Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition
- l = Low Voltage Level One Set-up Time Prior To The Low-to-high Clock Transition
- L = Low Voltage Level
- X = Don't Care
- ↑ = Transition from Low to High Level
- q<sub>n</sub> = Lower Case Letters Indicate The State Of the Reference Output Clock Transition

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## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current per Output, $I_O$	
For $V_O < -0.5V$ $V_O > V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ or $I_{GND}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package .....	90
SOIC Package .....	115
Maximum Junction Temperature .....	$150^{\circ}C$
Maximum Storage Temperature Range .....	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s) .....	$300^{\circ}C$
(SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range ( $T_A$ ) .....	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I$ , $V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

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### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	-	8	-	80	-	160	$\mu$ A
<b>HCT TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads			-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads			4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ to GND	0	5.5	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu$ A
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	5.5	-	-	8	-	80	-	160	$\mu$ A
Additional Quiescent Device Current Per Input Pin: 1 Unit Load (Note 4)	$\Delta I_{CC}$ (Note 4)	$V_{CC}$ -2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	$\mu$ A

NOTE:

4. For dual-supply systems theoretical worst case ( $V_I = 2.4V$ ,  $V_{CC} = 5.5V$ ) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOADS
DS, D0 to D7	0.35
CP, $\overline{PL}$	0.65

NOTE: Unit Load is  $\Delta I_{CC}$  limit specified in DC Electrical Specifications table, e.g. 360 $\mu$ A max at 25°C.

### Prerequisite For Switching Specifications

PARAMETER	SYMBOL	$V_{CC}$ (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>									
CP Pulse Width	$t_{WL}, t_{WH}$	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns

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### Prerequisite For Switching Specifications (Continued)

PARAMETER	SYMBOL	V <sub>CC</sub> (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
PL Pulse Width	t <sub>WL</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Set-up Time DS to CP	t <sub>SU</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
CE to CP	t <sub>SU(L)</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
D0-D7 to PL	t <sub>SU</sub>	2	80	-	100	-	120	-	ns
		4.5	16	-	20	-	24	-	ns
		6	14	-	17	-	20	-	ns
Hold Time DS to CP or CE	t <sub>H</sub>	2	35	-	45	-	55	-	ns
		4.5	7	-	9	-	11	-	ns
		6	6	-	8	-	9	-	ns
CE to CP	t <sub>H</sub>	2	0	-	0	-	0	-	ns
		4.5	0	-	0	-	0	-	ns
		6	0	-	0	-	0	-	ns
Recovery Time PL to CP	t <sub>REC</sub>	2	100	-	125	-	150	-	ns
		4.5	20	-	25	-	30	-	ns
		6	17	-	21	-	26	-	ns
Maximum Clock Pulse Frequency	f <sub>MAX</sub>	2	6	-	5	-	4	-	MHz
		4.5	30	-	24	-	20	-	MHz
		6	35	-	28	-	24	-	MHz

#### HCT TYPES

CP Pulse Width	t <sub>WL</sub> , t <sub>WH</sub>	4.5	18	-	23	-	27	-	ns
PL Pulse Width	t <sub>WL</sub>	4.5	20	-	25	-	30	-	ns
Set-up Time DS to CP	t <sub>SU</sub>	4.5	20	-	25	-	30	-	ns
CE to CP	t <sub>SU(L)</sub>	4.5	20	-	25	-	30	-	ns
D0-D7 to PL	t <sub>SU</sub>	6	20	-	25	-	30	-	ns
Hold Time DS to CP or CE	t <sub>H</sub>	4.5	7	-	9	-	11	-	ns
CE to CP	t <sub>S</sub> , t <sub>H</sub>	4.5	0	-	0	-	0	-	ns
Recovery Time PL to CP	t <sub>REC</sub>	4.5	20	-	25	-	30	-	ns
Maximum Clock Pulse Frequency	f <sub>MAX</sub>	4.5	27	-	22	-	18	-	MHz

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### Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C		-40°C TO 85°C	-55°C TO 125°C	UNITS
				TYP	MAX	MAX	MAX	
<b>HC TYPES</b>								
Propagation Delay CP or $\overline{CE}$ to $Q_7$ or $\overline{Q_7}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	165	205	250	ns
			4.5	-	33	41	50	ns
		$C_L = 15\text{pF}$	5	13	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	28	35	43	ns
$\overline{PL}$ to $Q_7$ or $\overline{Q_7}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	175	220	265	ns
			4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	30	37	45	ns
D7 to $Q_7$ or $\overline{Q_7}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	150	190	225	ns
			4.5	-	30	38	45	ns
		$C_L = 15\text{pF}$	5	12	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	26	33	38	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	75	95	110	ns
			4.5	-	15	19	22	ns
			6	-	13	16	19	ns
Input Capacitance	$C_{IN}$	-	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	17	-	-	-	pF
<b>HCT TYPES</b>								
Propagation Delay CP or $\overline{CE}$ to $Q_7$ or $\overline{Q_7}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	40	50	60	ns
		$C_L = 15\text{pF}$	5	17	-	-	-	ns
$\overline{PL}$ to $Q_7$ or $\overline{Q_7}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	40	50	60	ns
		$C_L = 15\text{pF}$	5	17	-	-	-	ns
D7 to $Q_7$ or $\overline{Q_7}$	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	35	44	53	ns
		$C_L = 15\text{pF}$	5	14	-	-	-	ns
Output Transition Times	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	4.5	-	15	19	22	ns
Input Capacitance	$C_{IN}$	$C_L = 50\text{pF}$	-	-	10	10	10	pF
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	24	-	-	-	pF

**NOTES:**

5.  $C_{PD}$  is used to determine the dynamic power consumption, per package.
6.  $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 + f_O)$  where  $f_i$  = Input Frequency,  $f_O$  = Output Frequency,  $C_L$  = Output Load Capacitance,  $V_{CC}$  = Supply Voltage.

Test Circuits and Waveforms

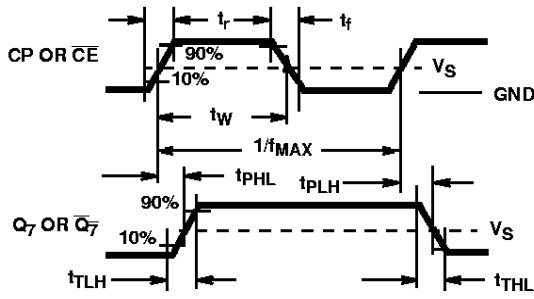


FIGURE 1. SERIAL-SHIFT MODE

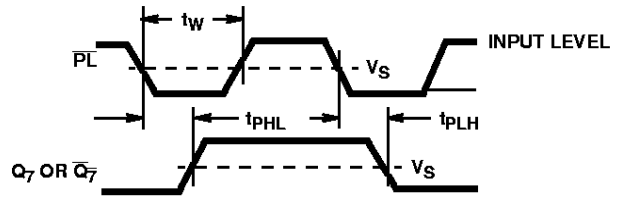


FIGURE 2. PARALLEL-LOAD MODE

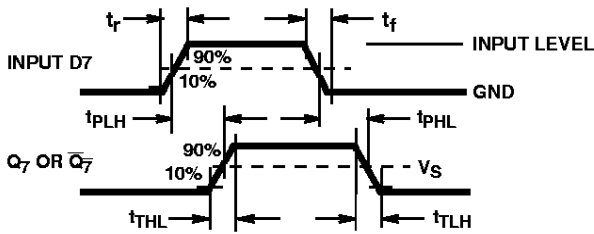


FIGURE 3. PARALLEL-LOAD MODE

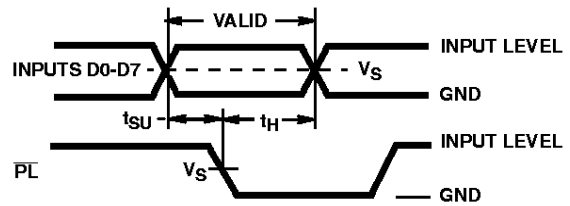


FIGURE 4. PARALLEL-LOAD MODE

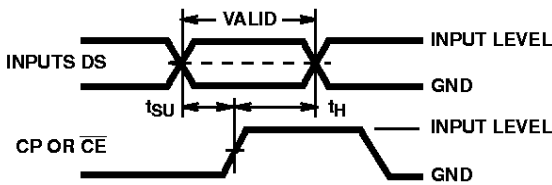


FIGURE 5. SERIAL-SHIFT MODE

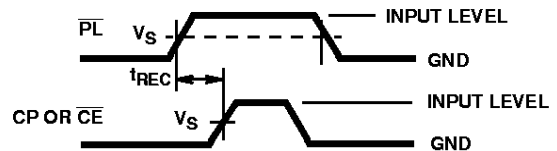


FIGURE 6. SERIAL-SHIFT MODE

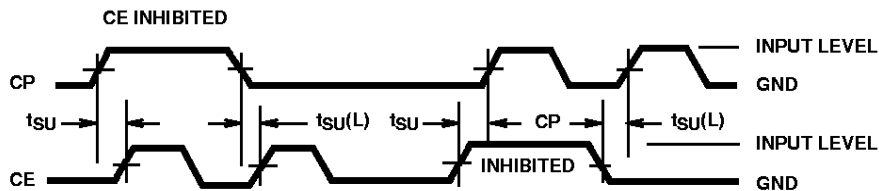


FIGURE 7. SERIAL-SHIFT, CLOCK-INHIBIT MODE