

MC74VHC138

3-to-8 Line Decoder

The MC74VHC138 is an advanced high speed CMOS 3-to-8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled, three Binary Select inputs (A0 - A2) determine which one of the outputs ($\overline{Y0}$ - $\overline{Y7}$) will go Low. When enable input E3 is held Low or either $\overline{E2}$ or $\overline{E1}$ is held High, decoding function is inhibited and all outputs go high. E3, $\overline{E2}$, and $\overline{E1}$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

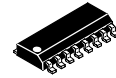
The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: $t_{PD} = 5.7ns$ (Typ) at $V_{CC} = 5V$
- Low Power Dissipation: $I_{CC} = 4\mu A$ (Max) at $T_A = 25^\circ C$
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: $V_{OLP} = 0.8 V$ (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates
- **These devices are available in Pb-free package(s). Specifications herein apply to both standard and Pb-free devices. Please see our website at www.onsemi.com for specific Pb-free orderable part numbers, or contact your local ON Semiconductor sales office or representative.**



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**SOIC-16
D SUFFIX
CASE 751B**

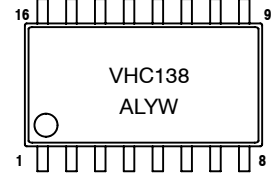
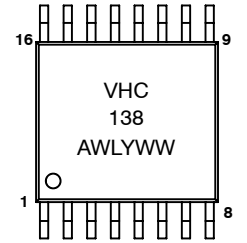
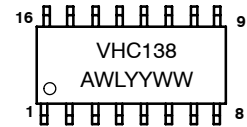


**TSSOP-16
DT SUFFIX
CASE 948F**



**SOIC EIAJ-16
M SUFFIX
CASE 966**

MARKING DIAGRAMS



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

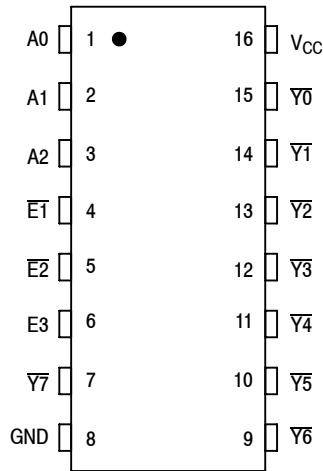
A = Assembly Location A = Assembly Location
WL = Wafer Lot L = Wafer Lot
Y = Year Y = Year
WW = Work Week W = Work Week

ORDERING INFORMATION

| Device | Package | Shipping |
|----------------|-----------------|-----------------|
| MC74VHC138D | SOIC-16 | 48 Units/Rail |
| MC74VHC138DR2 | SOIC-16 | 2500 Units/Reel |
| MC74VHC138DT | TSSOP-16 | 96 Units/Rail |
| MC74VHC138DTR2 | TSSOP-16 | 2500 Units/Reel |
| MC74VHC138M | SOIC EIAJ-16 | 48 Units/Rail |
| MC74VHC138MEL | SOIC EIAJ-16 | 2000 Units/Reel |

MC74VHC138

PIN ASSIGNMENT

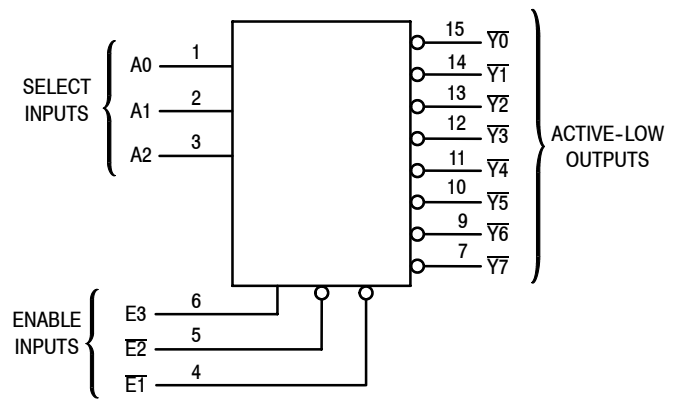


FUNCTION TABLE

| Inputs | | | | | | Outputs | | | | | | | |
|--------|----|----|----|----|----|---------|----|----|----|----|----|----|----|
| E3 | E2 | E1 | A2 | A1 | A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | H | X | X | X | X | H | H | H | H | H | H | H | H |
| L | X | X | X | X | X | H | H | H | H | H | H | H | H |
| H | L | L | L | L | L | L | H | H | H | H | H | H | H |
| H | L | L | L | L | H | H | L | H | H | H | H | H | H |
| H | L | L | L | H | L | H | H | L | H | H | H | H | H |
| H | L | L | H | L | L | H | H | H | H | H | L | H | H |
| H | L | L | H | H | L | H | H | H | H | H | H | L | H |
| H | L | L | H | H | H | H | H | H | H | H | H | H | L |

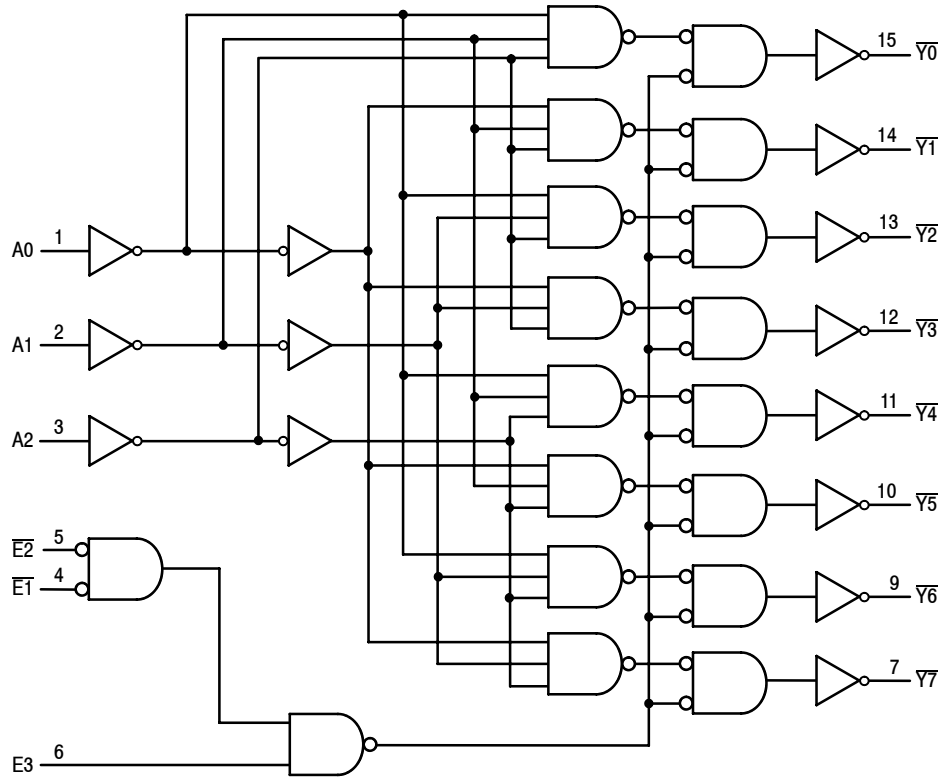
H = high level (steady state); L = low level (steady state);
X = don't care

LOGIC DIAGRAM

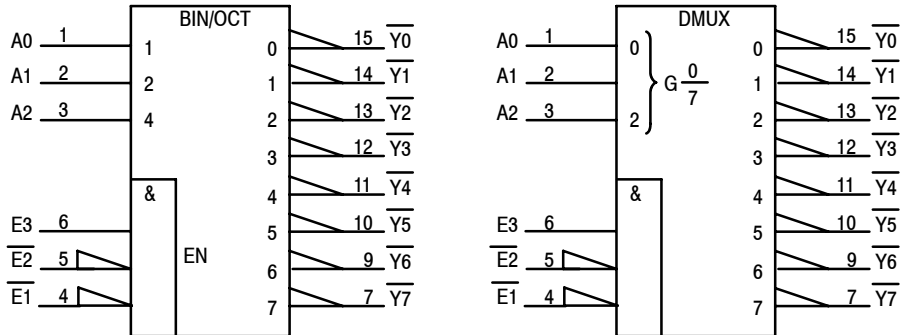


MC74VHC138

EXPANDED LOGIC DIAGRAM



IEC LOGIC DIAGRAM



MC74VHC138

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|--|-------------------------|------|
| V_{CC} | DC Supply Voltage | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage | - 0.5 to + 7.0 | V |
| V_{out} | DC Output Voltage | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{IK} | Input Diode Current | - 20 | mA |
| I_{OK} | Output Diode Current | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air, SOIC Packages† TSSOP Package† | 500 450 | mW |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

†Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------|--|------|-----------|------|
| V_{CC} | DC Supply Voltage | 2.0 | 5.5 | V |
| V_{in} | DC Input Voltage | 0 | 5.5 | V |
| V_{out} | DC Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature | - 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$ | 0 | 100 20 | ns/V |

The θ_{JA} of the package is equal to 1/Derating. Higher junction temperatures may affect the expected lifetime of the device per the table and figure below.

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

| Junction Temperature °C | Time, Hours | Time, Years |
|-------------------------|-------------|-------------|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |

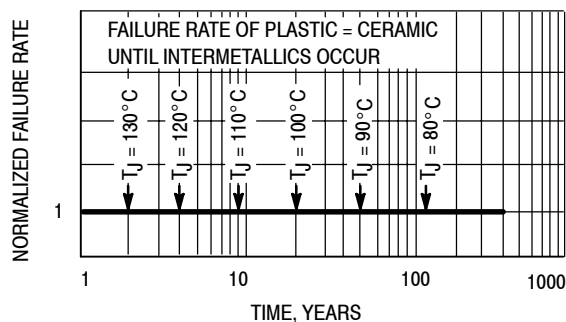


Figure 1. Failure Rate vs. Time Junction Temperature

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Test Conditions | V _{CC} (V) | T _A = 25°C | | | T _A = ≤ 85°C | | T _A = ≤ 125°C | | Unit |
|-----------------|---|--|------------------------|-----------------------|------|-------|-------------------------|-------|--------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 2.0 | 1.5 | | | 1.5 | | 1.5 | | V |
| | | | 3.0 | 2.1 | | | 2.1 | | 2.1 | | |
| | | | 4.5 | 3.15 | | | 3.15 | | 3.15 | | |
| | | | 5.5 | 3.85 | | | 3.85 | | 3.85 | | |
| V _{IL} | Maximum Low-Level Input Voltage | | 2.0 | | | 0.5 | | 0.5 | | 0.5 | V |
| | | | 3.0 | | | 0.9 | | 0.9 | | 0.9 | |
| | | | 4.5 | | | 1.35 | | 1.35 | | 1.35 | |
| | | | 5.5 | | | 1.65 | | 1.65 | | 1.65 | |
| V _{OH} | Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OH} = - 50 μA | 2.0 | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | | 3.0 | 2.9 | 3.0 | | 2.9 | | 2.9 | | |
| | | 4.5 | 4.4 | 4.5 | | 4.4 | | 4.4 | | 4.4 | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OH} = - 4 mA I _{OH} = - 8 mA | 3.0 | 2.58 | | | 2.48 | | 2.34 | | |
| 4.5 | 3.94 | | | | 3.80 | | 3.66 | | | | |
| V _{OL} | Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL} | V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 μA | 2.0 | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | | 3.0 | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 | | 0.0 | 0.1 | | 0.1 | | 0.1 | | |
| | | V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA | 3.0 | | | 0.36 | | 0.44 | | 0.52 | |
| 4.5 | | | | 0.36 | | 0.44 | | 0.52 | | | |
| I _{IN} | Maximum Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 5.5 | | | ± 0.1 | | ± 1.0 | | μA | |
| I _{CC} | Maximum Quiescent Supply Current | V _{IN} = V _{CC} or GND | 5.5 | | | 4.0 | | 40.0 | | μA | |

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0ns)

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | T _A = - 40 to 85°C | | T _A = - 55 to 125°C | | Unit |
|--|---|---|-----------------------|------|------|-------------------------------|------|--------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to Y | V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF | | 8.2 | 11.4 | 1.0 | 13.5 | 1.0 | 13.5 | ns |
| | | | | 10.0 | 15.8 | 1.0 | 18.0 | 1.0 | 18.0 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, E3 to Y | V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF | | 5.7 | 8.1 | 1.0 | 9.5 | 1.0 | 9.5 | ns |
| | | | | 7.2 | 10.1 | 1.0 | 11.5 | 1.0 | 11.5 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, E2 or E1 to Y | V _{CC} = 3.3 ± 0.3V C _L = 15pF C _L = 50pF | | 8.1 | 12.8 | 1.0 | 15.0 | 1.0 | 15.0 | ns |
| | | | | 10.6 | 16.3 | 1.0 | 18.5 | 1.0 | 18.5 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, E2 or E1 to Y | V _{CC} = 5.0 ± 0.5V C _L = 15pF C _L = 50pF | | 5.6 | 8.1 | 1.0 | 9.5 | 1.0 | 9.5 | ns |
| | | | | 7.1 | 10.1 | 1.0 | 11.5 | 1.0 | 11.5 | |
| C _{IN} | Maximum Input Capacitance | | | 4 | 10 | | 10 | | 10 | pF |
| | | | | | | | | | | |

| C _{PD} | Power Dissipation Capacitance (Note 1) | Typical @ 25°C, V _{CC} = 5.0V | | pF |
|-----------------|--|--|--|----|
| | | 34 | | |
| | | | | |

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

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SWITCHING WAVEFORMS

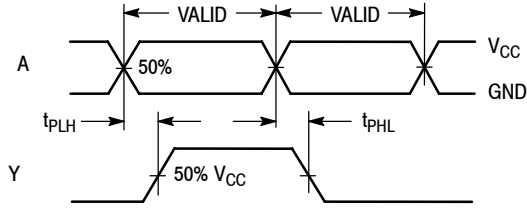


Figure 2.

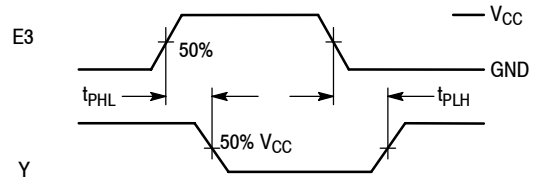


Figure 3.

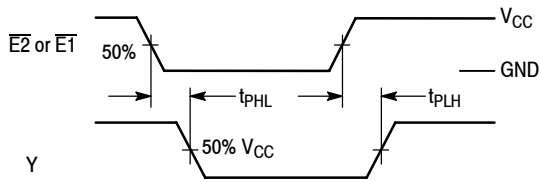
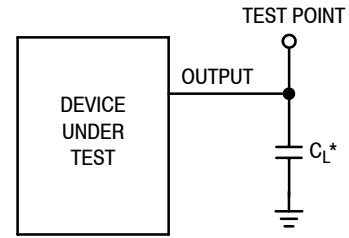


Figure 4.



*Includes all probe and jig capacitance

Figure 5. Test Circuit

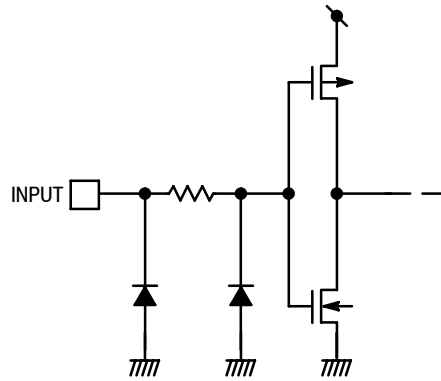
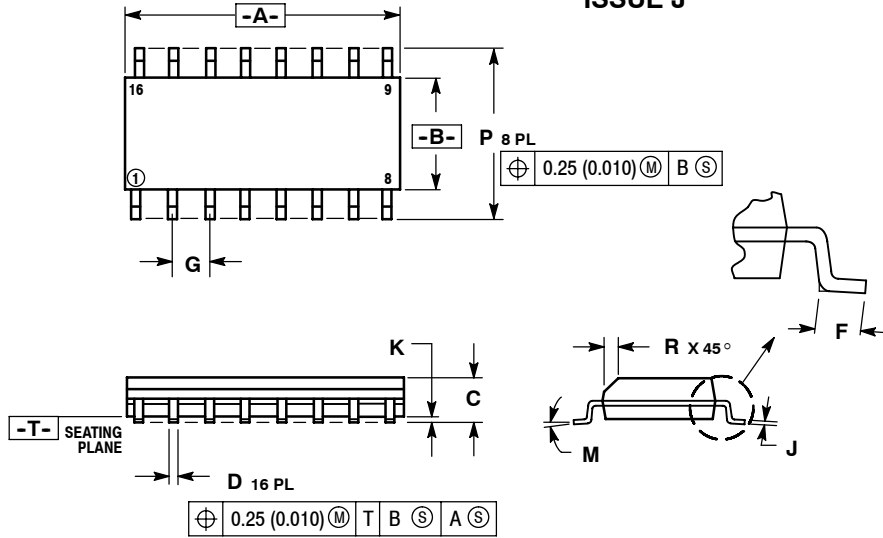


Figure 6. Input Equivalent Circuit

MC74VHC138

PACKAGE DIMENSIONS

D SUFFIX SOIC CASE 751B-05 ISSUE J

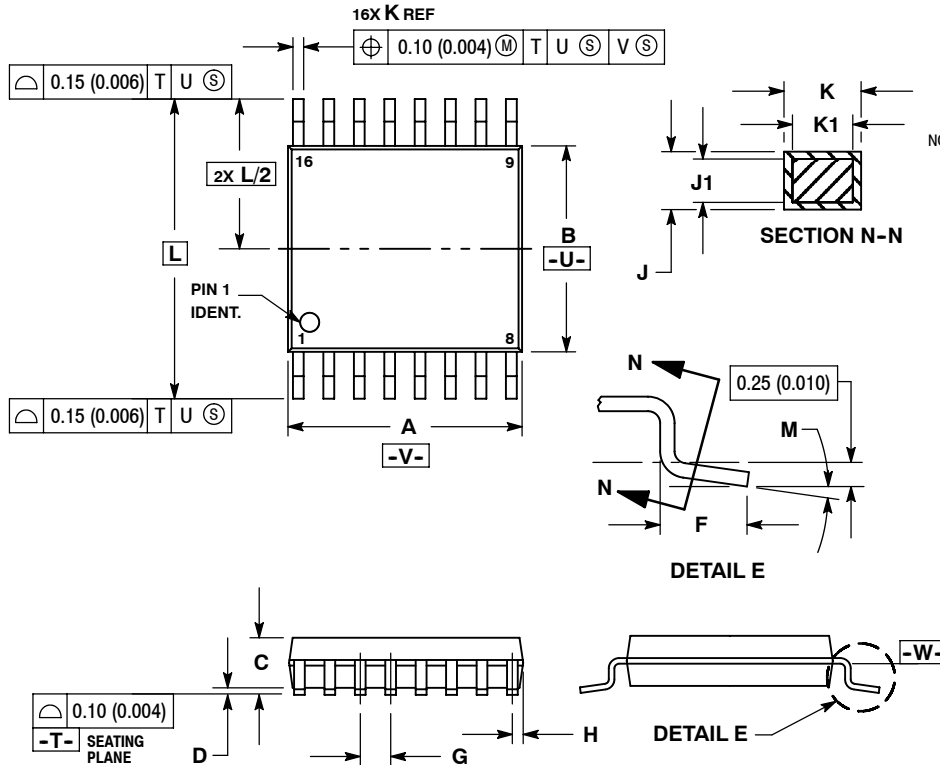


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

DT SUFFIX TSSOP CASE 948F-01 ISSUE O



NOTES:

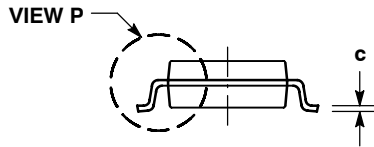
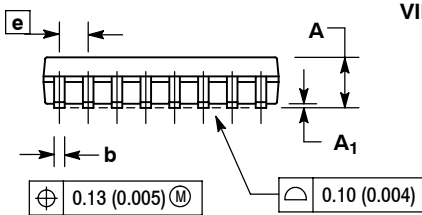
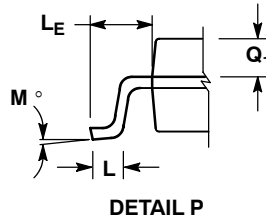
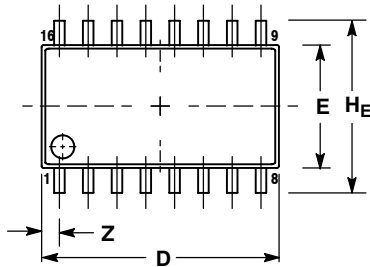
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74VHC138

PACKAGE DIMENSIONS

M SUFFIX SOIC EIAJ-16 CASE 966-01 ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM | MILLIMETERS | | INCHES | |
|----------------|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | --- | 2.05 | --- | 0.081 |
| A ₁ | 0.05 | 0.20 | 0.002 | 0.008 |
| b | 0.35 | 0.50 | 0.014 | 0.020 |
| c | 0.18 | 0.27 | 0.007 | 0.011 |
| D | 9.90 | 10.50 | 0.390 | 0.413 |
| E | 5.10 | 5.45 | 0.201 | 0.215 |
| e | 1.27 BSC | | 0.050 BSC | |
| H _E | 7.40 | 8.20 | 0.291 | 0.323 |
| L | 0.50 | 0.85 | 0.020 | 0.033 |
| L _E | 1.10 | 1.50 | 0.043 | 0.059 |
| M | 0° 10° | | 0° 10° | |
| Q ₁ | 0.70 | 0.90 | 0.028 | 0.035 |
| Z | --- | 0.78 | --- | 0.031 |

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