- Functionally Equivalent to AMD's AM29825 and AM29826
- Improved I_{OH} Specifications
- Multiple Output Enables Allow Multiuser Control of the Interface
- Outputs Have Undershoot Protection Circuitry
- Power-Up High-Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effect
- Dependable Texas Instruments Quality and Reliability

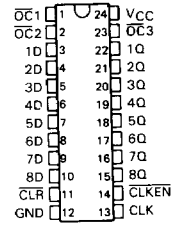
description

These 8-bit flip-flops feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing multiuser registers, I/O ports, bidirectional bus drivers, and working registers.

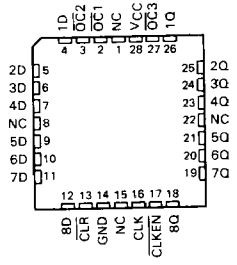
With the clock enable ($\overline{CLKEN}$) low, the eight D-type edge-triggered flip-flops enter data on the low-to-high transitions of the clock. Taking $\overline{CLKEN}$ high will disable the clock buffer, thus latching the outputs. The 'AS825 has non-inverting D inputs and the 'AS826 has inverting $\overline{D}$ inputs. Taking the $\overline{CLR}$ input low causes the eight Q outputs to go low independently of the clock.

Multiuser buffered output-control inputs ($\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$) can be used to place the eight outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components. The output controls do not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

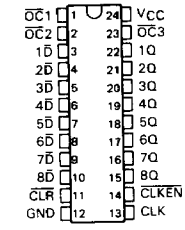
SN54AS825 . . . JT PACKAGE
SN74AS825 . . . DW OR NT PACKAGE
(TOP VIEW)



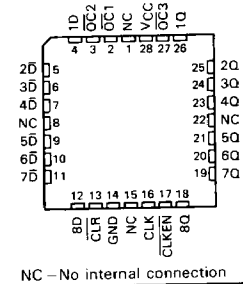
SN54AS825 . . . FK PACKAGE
SN74AS825 . . . FN PACKAGE
(TOP VIEW)



SN54AS826 . . . JT PACKAGE
SN74AS826 . . . DW OR NT PACKAGE
(TOP VIEW)



SN54AS826 . . . FK PACKAGE
SN74AS826 . . . FN PACKAGE
(TOP VIEW)



NC—No internal connection

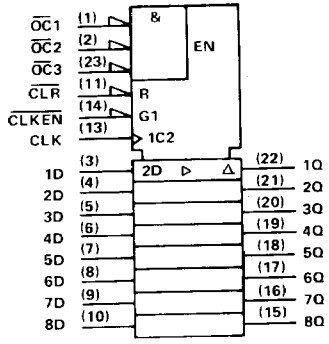
The SN54AS' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74AS' family is characterized for operation from 0°C to 70°C.

'AS825 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

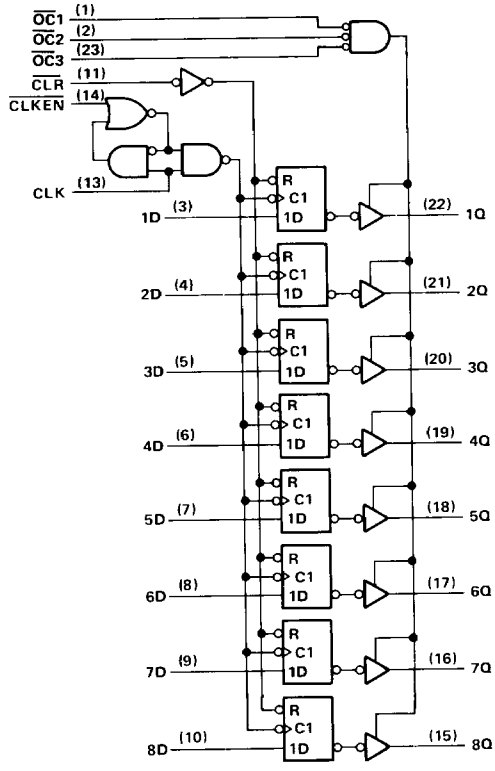
$\overline{OC}$* = H if any of $\overline{OC}$1, $\overline{OC}$2, or $\overline{OC}$3 are high.
$\overline{OC}$* = L if all of $\overline{OC}$1, $\overline{OC}$2, and $\overline{OC}$3 are low.

'AS825 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

'AS825 logic diagram (positive logic)



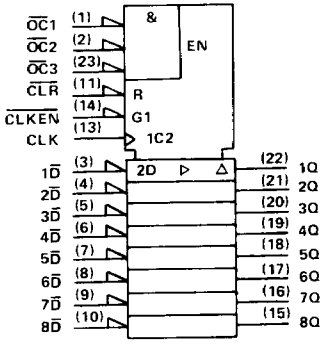
Pin numbers are for DW, JT, and NT packages.

'AS826 FUNCTION TABLE

INPUTS					OUTPUT
$\overline{OC}$*	$\overline{CLR}$	$\overline{CLKEN}$	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	H
L	H	H	X	X	Q_0
H	X	X	X	X	Z

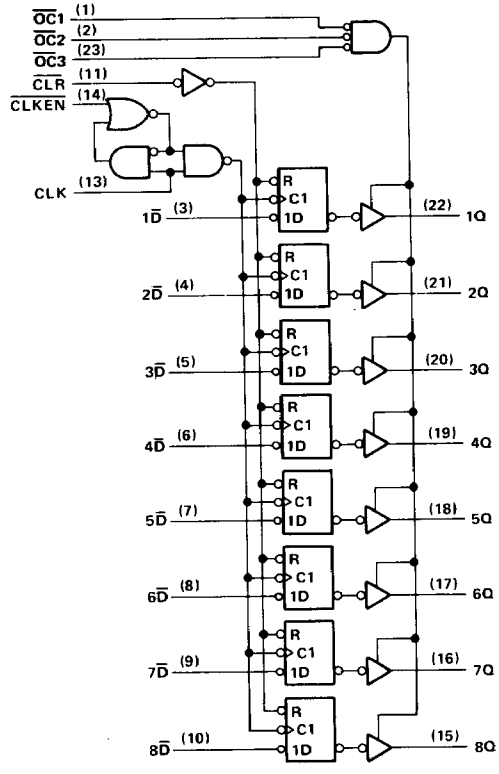
$\overline{OC}$* = H if any of $\overline{OC}1$, $\overline{OC}2$, or $\overline{OC}3$ are high.
$\overline{OC}$* = L if all of $\overline{OC}1$, $\overline{OC}2$, and $\overline{OC}3$ are low.

'AS826 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

'AS826 logic diagram (positive logic)



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Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . 7 V
Input voltage . . . . . 7 V
Voltage applied to a disabled 3-state output . . . . . 5.5 V
Operating free-air temperature range:
SN54AS825, SN54AS826 . . . . . −55°C to 125°C
SN74AS825, SN74AS826 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65 to 150°C

recommended operating conditions

			SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−24			−24	mA
I_{OL}	Low-level output current				32			48	mA
t_w	Pulse duration	$\overline{CLR}$ low	5			4			ns
		CLK high or low	9			8			
t_{su}	Setup time before CLK↑	$\overline{CLR}$ inactive	8			8			ns
		Data	7			6			
		$\overline{CLKEN}$ high or low	7			6			
t_h	Hold time, $\overline{CLKEN}$ or data after CLK↑		0			0			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54AS825 SN54AS826			SN74AS825 SN74AS826			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V_{CC}−2			V
		V_{CC} = 4.5 V,	I_{OH} = −15 mA	2.4	3.2		2.4	3.2		
		V_{CC} = 4.5 V,	I_{OH} = −24 mA	2			2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 32 mA		0.3	0.5				V
		V_{CC} = 4.5 V,	I_{OL} = 48 mA					0.35	0.5	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.4 V			−50			−50	μA
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.5			−0.5	mA
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	−30		−112	mA
I_{CC}	'AS825	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
			Outputs low		56	90		56	90	
			Outputs disabled		59	95		59	95	
	'AS826	V_{CC} = 5.5 V	Outputs high		45	73		45	73	mA
			Outputs low		56	90		56	90	
			Outputs disabled		59	95		59	95	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX				UNIT
			SN54AS825 SN54AS826		SN74AS825 SN74AS826		
			MIN	MAX	MIN	MAX	
t_{PLH}	CLK	Any Q	3.5	9	3.5	7.5	ns
t_{PHL}			3.5	11.5	3.5	11	
t_{PHL}	$\overline{CLR}$	Any Q	3.5	14	3.5	13	ns
t_{PZH}	$\overline{OC}$	Any Q	4	12	4	11	ns
t_{PZL}			4	13	4	12	
t_{PHZ}	$\overline{OC}$	Any Q	2	10	2	8	ns
t_{PLZ}			2	10	2	8	

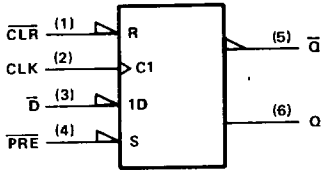
NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

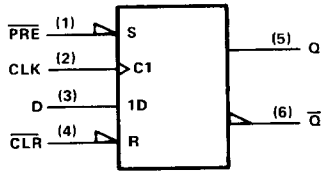
D flip-flop signal conventions

It is normal TI practice to name the outputs and other inputs of a D-type flip-flop and to draw its logic symbol based on the assumption of true data (D) inputs. Then outputs that produce data in phase with the data inputs are called Q and those producing complementary data are called $\overline{Q}$. An input that causes a Q output to go high or a $\overline{Q}$ output to go low is called Preset; an input that causes a $\overline{Q}$ output to go high or a Q output to go low is called Clear. Bars are used over these pin names ($\overline{PRE}$ and $\overline{CLR}$) if they are active-low.

The devices on this data sheet are second-source designs and the pin-name convention used by the original manufacturer has been retained. That makes it necessary to designate the inputs and outputs of the inverting circuit $\overline{D}$ and Q. In some applications it may be advantageous to redesignate the inputs and outputs as D and $\overline{Q}$. In that case, outputs should be renamed as shown below. Also shown are corresponding changes in the graphical symbol. Arbitrary pin numbers are shown in parentheses.

Notice that Q and $\overline{Q}$ exchange names, which causes Preset and Clear to do likewise. Also notice that the polarity indicators (⊏) on $\overline{PRE}$ and $\overline{CLR}$ remain since these inputs are still active-low, but that the presence or absence of the polarity indicator changes at $\overline{D}$, Q, and $\overline{Q}$. Of course pin 5 (Q) is still in phase with the data input D, but now both are considered active high.





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