150V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller

FEATURES

- **Wide V_{IN} Range: 4.5V to 140V (150V Abs Max)**
- **Wide Output Voltage Range: 1V ≤ V_{OUT} ≤ 60V**
- **Low Operating I_Q: 16µA (48V_{IN} to 12V_{OUT} and 3.3V_{OUT})**
- **Adjustable Gate Drive Level Up to 10V**
- **Optional Spread Spectrum Operation**
- **Very Low Dropout: 100% Duty Cycle Operation**
- Low I_Q in Dropout: 78µA (One Channel On)
- R_{SENSE} or Inductor DCR Current Sensing
- Out-of-Phase Controllers Reduce Required Input Capacitance and Power Supply Induced Noise
- Phase-Lockable Frequency (75kHz to 720kHz)
- Programmable Fixed Frequency (50kHz to 750kHz)
- Selectable Continuous, Pulse-Skipping, or Low Ripple Burst Mode® Operation at Light Loads
- Onboard LDO or External NMOS LDO for DRV_{CC}
- $EXTV_{CC}$ LDO Powers Drivers from V_{OUT}
- Programmable Input Overvoltage Lockout
- 48-Lead (7mm × 7mm) eLQFP Package
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

- Automotive and Transportation
- Industrial and Telecommunications
- Military/Avionics

DESCRIPTION

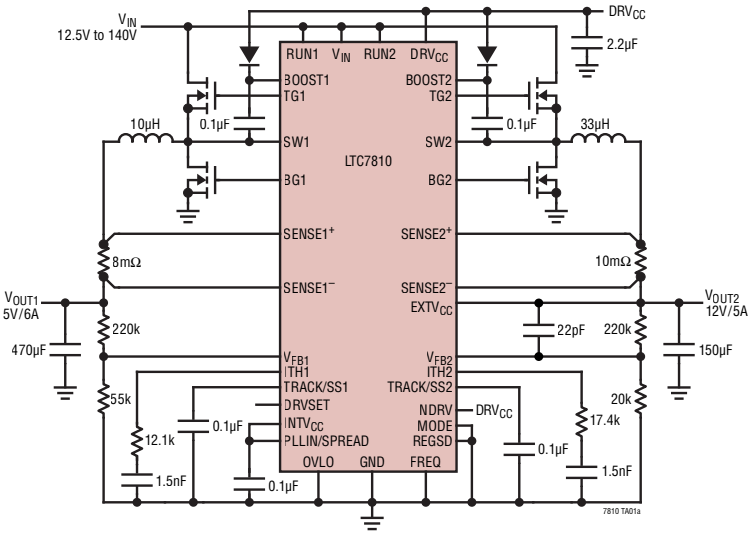
The LTC®7810 is a high performance dual step-down DC/DC switching regulator controller that drives all N-channel synchronous power MOSFET stages that can operate from voltages up to 140V. A constant frequency current mode architecture allows a phase-lockable frequency of up to 720kHz.

The low no-load quiescent current extends operating run time in battery-powered systems. The LTC7810 features a precision 1V reference, enabling the output voltage to be programmed from 1V to 60V. The gate drive voltage for the LTC7810 can be programmed to 6V, 8V, or 10V to allow the use of logic-level or standard-threshold FETs and to maximize efficiency.

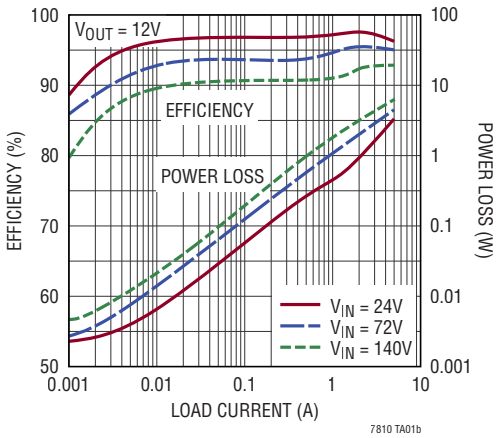
The LTC7810 additionally features spread spectrum operation which significantly reduces the peak radiated and conducted noise on both the input and output supplies, making it easier to comply with electromagnetic interference (EMI) standards.

TYPICAL APPLICATION

High Efficiency Dual 12V/5V Output Step-Down Regulator with Spread Spectrum



Efficiency and Power Loss vs Load Current



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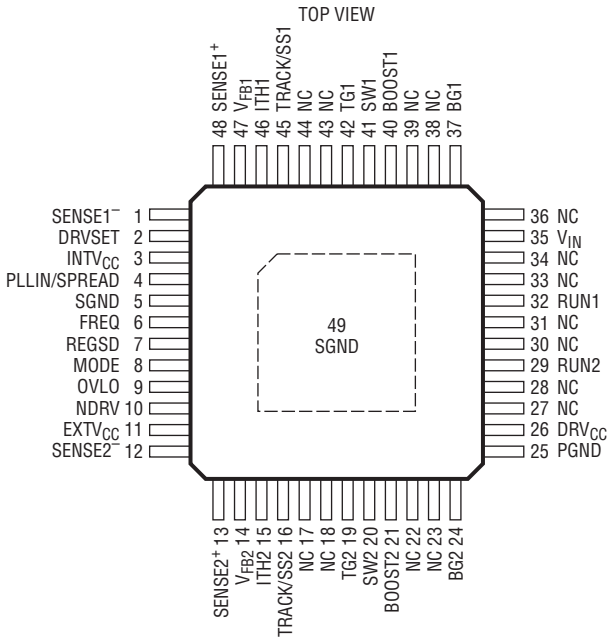
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 150V
RUN1, RUN2 Voltages ..... –0.3V to 150V
BOOST1, BOOST2 ..... –0.3V to 150V
Switch Voltage (SW1, SW2) ..... –5V to 150V
(BOOST1-SW1), (BOOST2-SW2) ..... –0.3V to 11V
$EXTV_{CC}$ Voltage ..... –0.3V to 65V
DRV_{CC} Voltage ..... –0.3V to 11V
($NDRV-DRV_{CC}$) Voltage (Note 9) ..... –0.3V to 6V
PLLIN/SPREAD, FREQ Voltages ..... –0.3V to 6V
TRACK/SS1, TRACK/SS2 Voltages ..... –0.3V to 6V
ITH1, ITH2, V_{FB1}, V_{FB2}, MODE Voltages ..... –0.3V to 6V
OVLO, REGSD, DRVSET Voltages ..... –0.3V to 6V
$SENSE1^+$, $SENSE2^+$, $SENSE1^-$,
$SENSE2^-$ Voltages ..... –0.3V to 65V
BG1, BG2, TG1, TG2 ..... (Note 10)
Operating Junction Temperature Range (Notes 2, 8)
LTC7810E, LTC7810I ..... –40°C to 125°C
LTC7810H ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



LXE PACKAGE
48-LEAD (7mm × 7mm) PLASTIC eLQFP

T_{JMAX} = 150°C, θ_{JA} = 20°C/W
EXPOSED PAD (PIN 49) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC7810ELXE#PBF	LTC7810	48-Lead (7mm × 7mm) Plastic eLQFP	–40°C to 125°C
LTC7810ILXE#PBF	LTC7810	48-Lead (7mm × 7mm) Plastic eLQFP	–40°C to 125°C
LTC7810HLXE#PBF	LTC7810	48-Lead (7mm × 7mm) Plastic eLQFP	–40°C to 150°C
AUTOMOTIVE PRODUCTS**			
LTC7810HLXE#WPBF	LTC7810	48-Lead (7mm × 7mm) Plastic eLQFP	–40°C to 150°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

For more information on lead free part marking, go to: http://www.adi.com/leadfree/
For more information on tape and reel specifications, go to: http://www.adi.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN1,2 = 5V, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply (V_{IN})							
V_{IN}	Input Supply Operating Range	(Note 11)		4.5		140	V
$V_{OUT1,2}$	Regulated Output Voltage Set Point			1		60	V
I_{VIN}	V_{IN} Current in Regulation	Figure 14 Circuit, 48V to 12V and 3.3V, No Load			16		µA
		Figure 14 Circuit, 12V to 3.3V, No Load, RUN2 = 0V			32		µA
I_Q	No-Load DC Supply Current	(Note 5)					
	Shutdown V_{IN} Current	RUN1,2 = 0V			1.5	5	µA
	Sleep Mode V_{IN} Current (Note 3)	V_{SENSE1}^- ≥ 3.2V, V_{EXTVCC} = 12V V_{SENSE1}^- ≥ 3.2V, V_{EXTVCC} = 0V V_{SENSE1}^- < 3.2V			4 25 40	8 50 75	µA µA µA
	Sleep Mode SENSE1⁻ Current (Note 3)	V_{SENSE1}^- ≥ 3.2V			16	30	µA
	Sleep Mode $EXTV_{CC}$ Current (Note 3)	V_{EXTVCC} = 12V			23	45	µA
	Low I_Q Dropout (One Channel On) Combined V_{IN} and V_{SENSE}^- DC Supply Current	V_{FB} = 0.97V, V_{IN} = V_{SENSE}^- ≥ 8V, No Load			78	130	µA
	Low I_Q Dropout (Both Channels On) Combined V_{IN} and V_{SENSE}^- DC Supply Current	$V_{FB1,2}$ = 0.97V, V_{IN} = $V_{SENSE1,2}^-$ ≥ 8V, No Load			110	160	µA
	Pulse-Skipping or Forced Continuous Mode	One Channel On Both Channels On			1.7 2.4		mA mA
	RUN Pin ON Threshold	V_{RUN1}, V_{RUN2} Rising	●	1.17	1.22	1.27	V
	RUN Pin Hysteresis				120		mV
	OVLO Pin OFF Threshold	V_{OVLO} Rising	●	1.17	1.22	1.27	V
	OVLO Pin Hysteresis				65		mV
Controller Operation							
$V_{FB1,2}$	Regulated Feedback Voltage	(Note 4) V_{IN} = 4.5V to 150V, ITH1 = 0.6V to 1.2V –40°C to 85°C, All Grades	●	0.985 0.990	1.0 1.0	1.015 1.010	V V
	Feedback Current	(Note 4)			–5	±50	nA
	Feedback Overvoltage Threshold	Relative to Regulated $V_{FB1,2}$		7	10	13	%
$g_{m1,2}$	Transconductance Amplifier g_m	(Note 4) ITH1,2 = 1.2V, Sink/Source = 5µA			2		mmho
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{FB1,2}$ = 0.9V, $V_{SENSE1,2}^-$ = 3.3V	●	67	75	83	mV
	Current Sense Threshold Matching Between Channels	$V_{FB1,2}$ = 0.9V, $V_{SENSE1,2}^-$ = 3.3V		–5	0	5	mV
$I_{SENSE1,2}^+$	SENSE1,2⁺ Pin Current	$V_{SENSE1,2}^+$ = 3V				±1	µA
I_{SENSE1}^-	SENSE1⁻ Pin Current	V_{SENSE1}^- < 3V 3.2V ≤ V_{SENSE1}^- < $INTV_{CC}$ – 0.5V V_{SENSE1}^- > $INTV_{CC}$ + 0.5V V_{SENSE1}^- ≥ 8V, in Low I_Q Dropout			6 60 540 25		µA µA µA µA
I_{SENSE2}^-	SENSE2⁻ Pin Current	V_{SENSE2}^- < $INTV_{CC}$ – 0.5V V_{SENSE2}^- > $INTV_{CC}$ + 0.5V V_{SENSE2}^- ≥ 8V, in Low I_Q Dropout			4 480 4		µA µA µA
$I_{TRACK/SS1,2}$	Soft-Start Charge Current	$V_{TRACK/SS1,2}$ = 0V		8	10	12	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN1,2 = 5V, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers							
	TG or BG On-Resistance	DRVSET OPEN Pull-up Pull-down			 2.0 1.0		 Ω Ω
	TG or BG Transition Time Rise Time Fall Time	DRVSET OPEN (Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 40 20		 ns ns
	TG Off to BG On Delay Synchronous Switch-On Delay Time	DRVSET OPEN			35		ns
	BG Off to TG On Delay Top Switch-On Delay Time	DRVSET OPEN			35		ns
$t_{ON(MIN)}$	TG Minimum On-Time	(Note 7) DRVSET OPEN			90		ns
	Maximum Duty Cycle	Output in Dropout, V_{SENSE}^- < 8V Output in Dropout, V_{SENSE}^- ≥ 8V			99 100		% %
	BOOST Charge Pump Available Output Current	Output in Dropout, V_{BOOST} = 16V, V_{SW} = 12V, FREQ = 0V			105		µA
	BOOST-SW Charge Pump Voltage	Output in Dropout, V_{SENSE}^- ≥ 8V			8.5		V
Low Dropout (LDO) Linear Regulators							
	DRV_{CC} Regulation Point for $EXTV_{CC}$ and NDRV LDOs	DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET OPEN		5.7 7.6 9.6	6.0 8.0 10.0	6.2 8.3 10.4	V V V
	DRV_{CC} Regulation Point for Internal V_{IN} LDO	DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET OPEN			5.7 7.6 9.6		V V V
V_{CCXO}	$EXTV_{CC}$ LDO Switchover Voltage	$EXTV_{CC}$ Rising DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET OPEN		 4.55 7.3 8.3	 4.7 7.5 8.5	 4.8 7.8 8.8	 V V V
	$EXTV_{CC}$ Switchover Hysteresis				250		mV
UVLO	Undervoltage Lockout	DRV_{CC} Rising DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET OPEN	 ● ● ●	 3.9 5.3 7.2	 4.1 5.5 7.5	 4.3 5.7 7.8	 V V V
		DRV_{CC} Falling DRVSET = $INTV_{CC}$ DRVSET = 0V DRVSET OPEN	 ● ● ●	 3.8 5.0 6.4	 4.0 5.2 6.7	 4.1 5.4 7.0	 V V V
	REGSD Threshold Voltage	V_{REGSD} Rising			1.2		V
	REGSD Charge Current	V_{REGSD} = 1V, REGSD Rising			10		µA
	REGSD Discharge Current	V_{REGSD} = 1V, REGSD Falling			10		µA
	$INTV_{CC}$ Regulation Point				4.5		V
Spread Spectrum Oscillator and Phase-Locked Loop							
f_{OSC}	Low Fixed Frequency	V_{FREQ} = 0V, PLLIN/SPREAD = 0V		160	200	230	kHz
	High Fixed Frequency	V_{FREQ} = $INTV_{CC}$, PLLIN/SPREAD = 0V		230	300	340	kHz
	Programmable Frequency	R_{FREQ} = 25kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 65kΩ, PLLIN/SPREAD = 0V R_{FREQ} = 105kΩ, PLLIN/SPREAD = 0V		 375	105 430 780	 485	kHz kHz kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V, RUN1,2 = 5V, $EXTV_{CC}$ = 0V, DRVSET = $INTV_{CC}$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SYNC}	Synchronizable Frequency Range	PLLIN/SPREAD = External Clock	●	75		720	kHz
	PLLIN Input High Level PLLIN Input Low Level		● ●	2.5		 0.5	V V
	Spread Spectrum Frequency Range (Relative to f_{OSC}) Minimum Frequency Maximum Frequency	PLLIN/SPREAD = $INTV_{CC}$, R_{FREQ} = 105kΩ			 –15 +15		 % %
	Spread Spectrum Modulation Frequency	PLLIN/SPREAD = $INTV_{CC}$			4.5		kHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC7810 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC7810E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC7810I is guaranteed over the –40°C to 125°C operating junction temperature range and the LTC7810H is guaranteed over the –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: $SENSE1^-$ bias current is reflected to the input supply by the formula $I_{VIN} = I_{SENSE1^-} \bullet V_{OUT1}/(V_{IN} \bullet \eta)$, where η is the efficiency. $EXTV_{CC}$ bias current is similarly reflected to the input supply when biased by an output greater than the $EXTV_{CC}$ LDO Switchover Voltage (V_{CCOX}).

Note 4: The LTC7810 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,2}$. The specification at 85°C is not tested in production and is assured by design, characterization and correlation to production testing at other temperatures (125°C for the LTC7810E/LTC7810I, 150°C for the LTC7810H.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current > 40% of I_{MAX} (See Minimum On-Time Considerations in the Applications Information section).

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

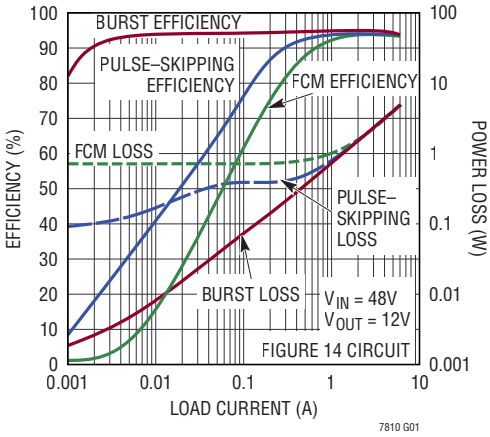
Note 9: Do not apply a voltage or current source to the NDRV pin, other than tying NDRV to DRV_{CC} when not used. If used it must be connected to capacitive loads only (see DRV_{CC} Regulators in the Applications Information section), otherwise permanent damage may occur.

Note 10: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

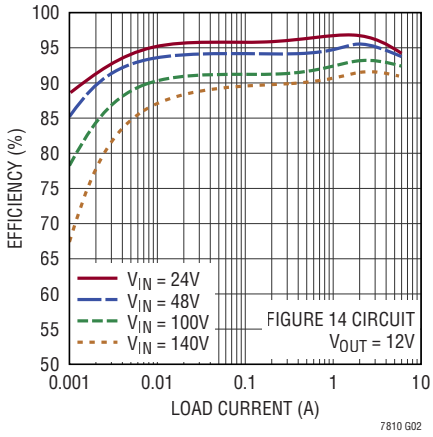
Note 11: The minimum input supply operating range is dependent on the DRV_{CC} UVLO thresholds as determined by the DRVSET pin setting.

TYPICAL PERFORMANCE CHARACTERISTICS

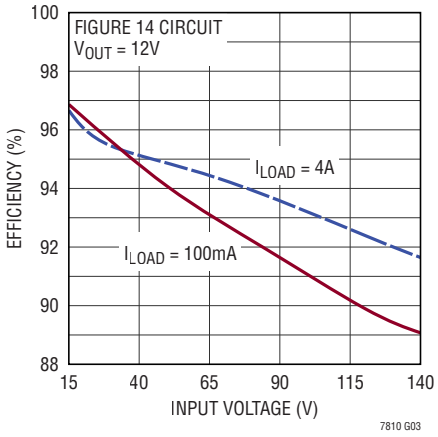
Efficiency and Power Loss vs Load Current



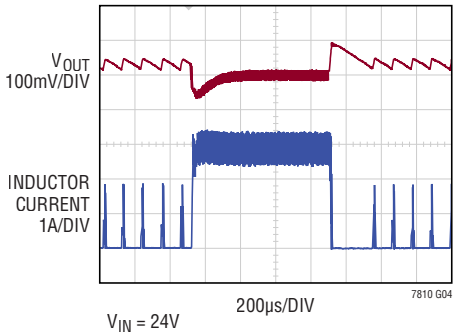
Efficiency vs Load Current



Efficiency vs Input Voltage

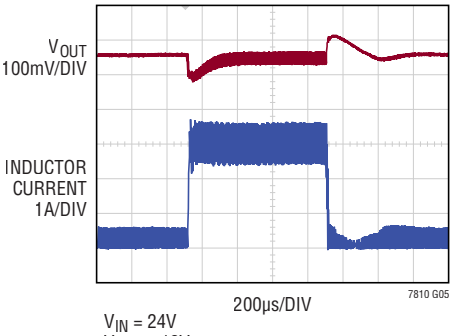


Load Step Burst Mode Operation



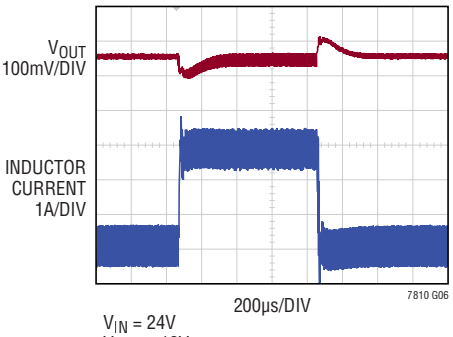
VIN = 24V
VOUT = 12V
100mA to 3A LOAD STEP
FIGURE 14 CIRCUIT, PLLIN/SPREAD = GND

Load Step Pulse-Skipping Mode



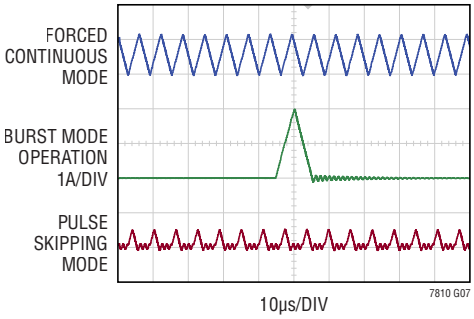
VIN = 24V
VOUT = 12V
100mA to 3A LOAD STEP
FIGURE 14 CIRCUIT, PLLIN/SPREAD = GND

Load Step Forced Continuous Mode



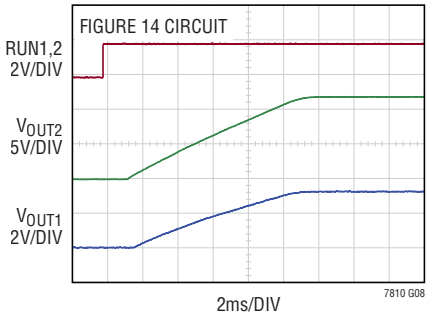
VIN = 24V
VOUT = 12V
100mA to 3A LOAD STEP
FIGURE 14 CIRCUIT, PLLIN/SPREAD = GND

Inductor Current at Light Load

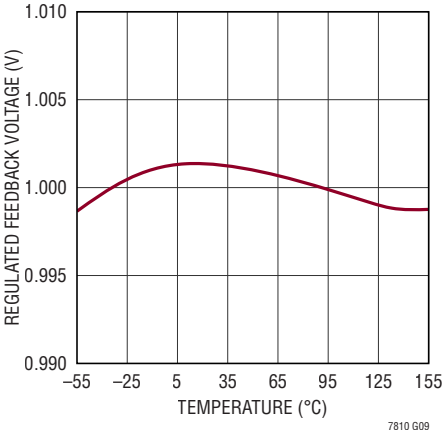


VIN = 24V
VOUT = 12V
ILOAD = 100mA
FIGURE 14 CIRCUIT, PLLIN/SPREAD = GND

Soft Start-Up

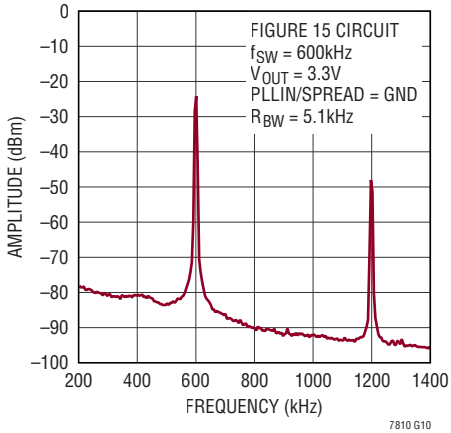


Regulated Feedback Voltage vs Temperature

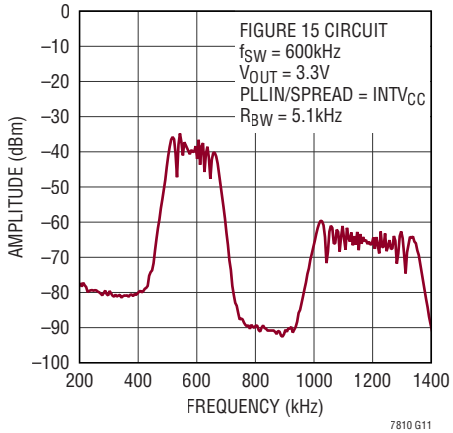


TYPICAL PERFORMANCE CHARACTERISTICS

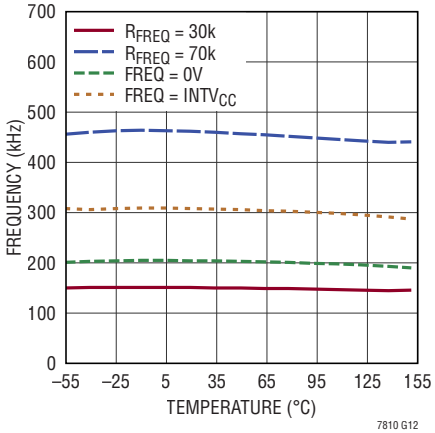
Output Voltage Frequency Spectrum (Spread Spectrum Disabled)



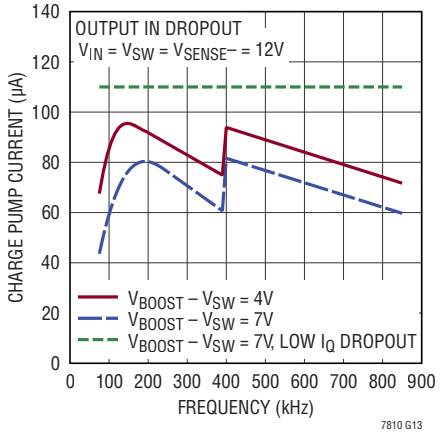
Output Voltage Frequency Spectrum (Spread Spectrum Enabled)



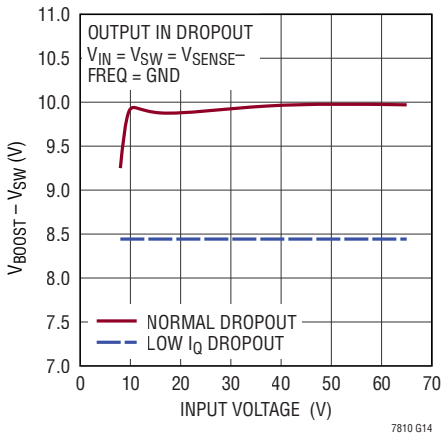
Oscillator Frequency vs Temperature



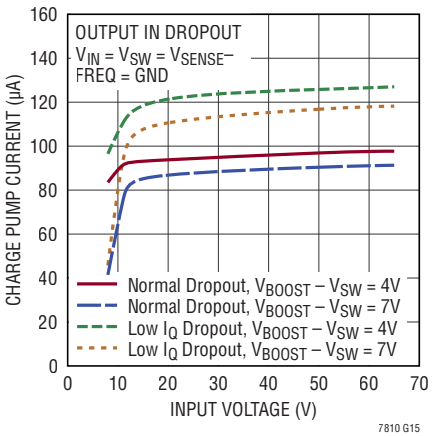
BOOST Charge Pump Output Current vs Frequency



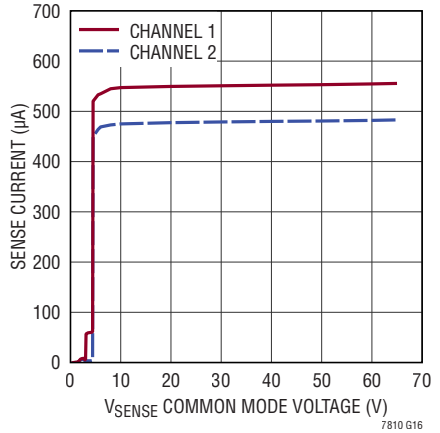
BOOST Charge Pump Output Voltage in Dropout vs Input Voltage



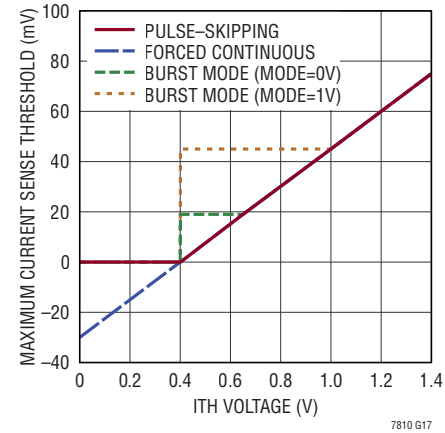
BOOST Charge Pump Output Current in Dropout vs Input Voltage



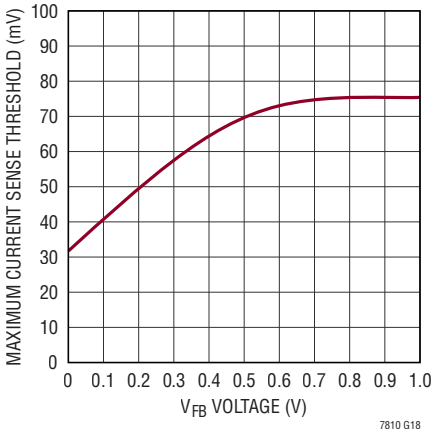
SENSE Pins Total Input Current vs V_{SENSE} Voltage



Maximum Current Sense Threshold vs ITH Voltage

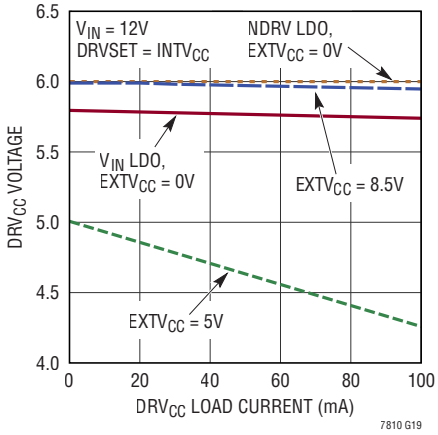


Foldback Current Limit

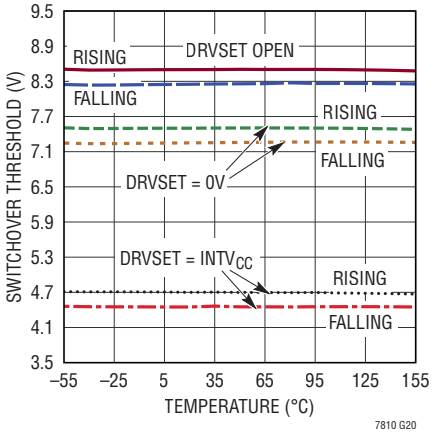


TYPICAL PERFORMANCE CHARACTERISTICS

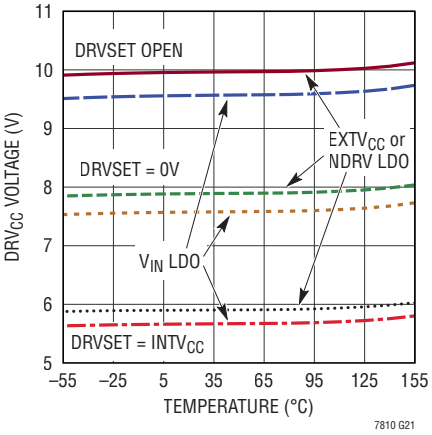
DRV_{CC} Load Regulation



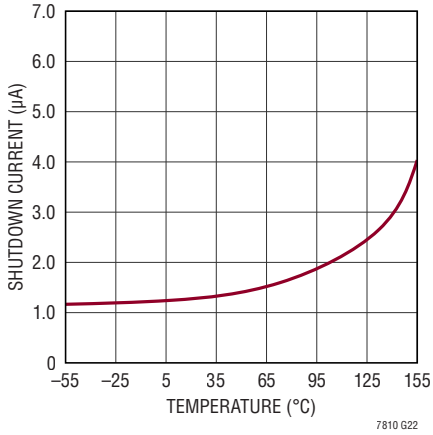
$EXTV_{CC}$ Switchover Thresholds vs Temperature



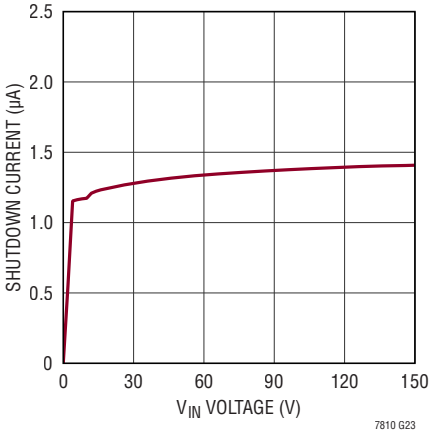
DRV_{CC} Voltage vs Temperature



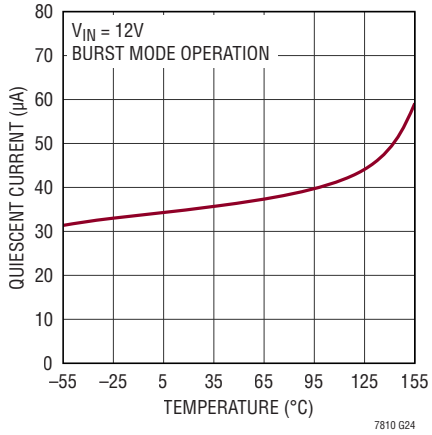
Shutdown Current vs Temperature



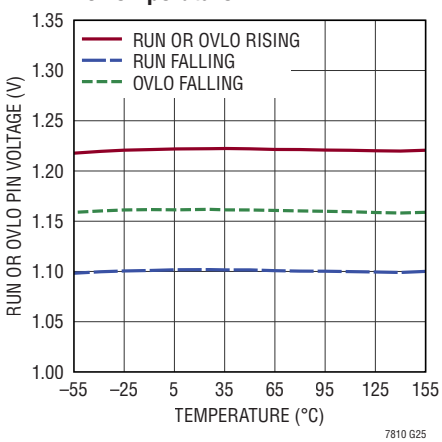
Shutdown Current vs V_{IN} Voltage



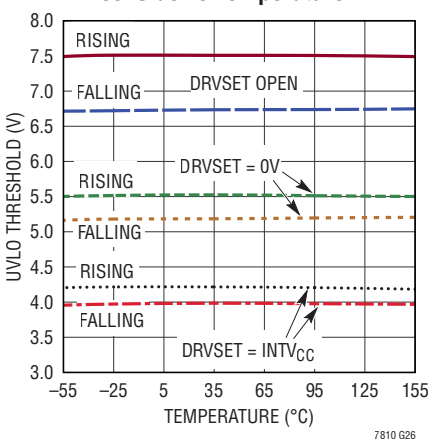
Quiescent Current vs Temperature



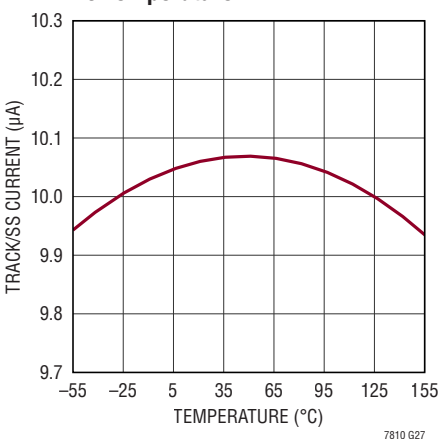
RUN and OVLO Thresholds vs Temperature



DRV_{CC} Undervoltage Lockout Thresholds vs Temperature



TRACK/SS Pull-Up Current vs Temperature



PIN FUNCTIONS

DRVSET (Pin 2): DRV_{CC} Regulation Program Pin. This pin sets the regulation point for the DRV_{CC} low dropout (LDO) linear regulators. Tying this pin to GND sets DRV_{CC} to 8V, tying it to $INTV_{CC}$ sets DRV_{CC} to 6V, and floating this pin sets DRV_{CC} to 10V. The DRV_{CC} UVLO and $EXTV_{CC}$ switchover thresholds change correspondingly with the DRV_{CC} regulation point, as listed in the Electrical Characteristics table.

$INTV_{CC}$ (Pin 3): Output of the Internal 4.5V Low Dropout Regulator. Internal low voltage analog and digital circuits are powered by this supply. A low ESR 0.1µF ceramic bypass capacitor should be connected between $INTV_{CC}$ and GND, as close as possible to the IC.

PLLIN/SPREAD (Pin 4): External Synchronization Input to Phase Detector and Spread Spectrum Enable. When an external clock is applied to this pin, the phase-locked loop will force the rising TG1 signal to be synchronized with the rising edge of the external clock. When not synchronizing to an external clock, tie this input to $INTV_{CC}$ to enable spread spectrum dithering of the oscillator or to ground to disable spread spectrum.

SGND (Pins 5, Exposed Pad Pin 49): Small-signal ground common to both controllers, must be routed separately from high current grounds to the common (–) terminals of the C_{IN} capacitors. The exposed pad must be soldered to PCB ground for rated thermal performance.

FREQ (Pin 6): Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 200kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 300kHz. Other frequencies between 50kHz and 750kHz can be programmed using a resistor between FREQ and GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency.

REGSD (Pin 7): Regulator Shutdown Timer. This pin limits the time allowed for switching while the internal V_{IN} or NDRV linear regulators are operating, due to $EXTV_{CC}$ being below its switchover voltage. A capacitor from REGSD to ground limits the time to $t_{REGSD} = 1.2 \bullet C_{REGSD}/10\mu A$. When the REGSD voltage exceeds 1.2V, the linear regulator shuts down for $29 \bullet t_{REGSD}$, giving a "regulator-on" duty cycle of 3.3%. This pin sources 10µA of current when $EXTV_{CC}$ is below the switchover voltage and the LTC7810 is not in sleep, and sinks 10µA when $EXTV_{CC}$ is above the switchover voltage or when the LTC7810 is in sleep. Ground this pin to disable the regulator shutdown timer.

MODE (Pin 8): Mode Select and Burst Clamp Adjust Input. This input determines how the LTC7810 operates at light loads. Pulling this pin to ground selects Burst Mode operation with a burst clamp level of 25% of $V_{SENSE(MAX)}$. Tying this pin to a voltage between 0.5V and 1V selects Burst Mode and adjusts the burst clamp level between 10% and 60%. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.4V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. Do not float this pin.

OVLO (Pin 9): Overvoltage Lockout Input. Forcing this pin above 1.22V disables switching of the controllers. The DRV_{CC} and $INTV_{CC}$ regulation is maintained during an OVLO event. Exceeding the OVLO threshold triggers a soft-start reset. Tie this pin to ground if the OVLO function is not used.

NDRV (Pin 10): Drive Output for External Pass Device of the NDRV LDO Regulator for DRV_{CC}. Connect this pin to the gate of an external NMOS pass device. An internal charge pump allows NDRV to be driven above V_{IN} for low dropout performance. Tie this pin to DRV_{CC} if the NDRV regulator is not used.

$EXTV_{CC}$ (Pin 11): External Power Input to an Internal LDO Connected to DRVCC. This LDO supplies DRVCC power, bypassing both the internal V_{IN} LDO and the external NDRV LDO whenever $EXTV_{CC}$ is higher than its switchover threshold. See DRVCC Regulators in the Applications Information section. Do not exceed 65V on this pin. Connect this pin to ground if the $EXTV_{CC}$ LDO is not used.

$SENSE1^-$, $SENSE2^-$ (Pins 1, 12): The (–) Input to the Differential Current Comparators. When $SENSE1,2^-$ is greater than $INTV_{CC}$, the $SENSE^-$ pin supplies current to the current comparator. When $SENSE1^-$ is greater than 3.2V, it supplies the majority of the sleep mode quiescent current instead of V_{IN}, further reducing the input-referred quiescent current.

PIN FUNCTIONS

SENSE1+, SENSE2+ (Pins 48, 13): The (+) Input to the Differential Current Comparators. The ITH pin voltage and controlled offsets between the SENSE– and SENSE+ pins in conjunction with R_{SENSE} set the current trip threshold.

V_{FB1}, V_{FB2} (Pins 47, 14): Receives the remotely sensed feedback voltage for each buck controller from an external resistive divider across the output. Tie V_{FB2} to $INTV_{CC}$ for a two-phase single output application, in which both channels share V_{FB1}, ITH1, and TRACK/SS1.

ITH1, ITH2 (Pins 46,15): Error Amplifier Outputs and Switching Regulator Compensation Points. Each associated channel's current comparator trip point increases with this control voltage.

TRACK/SS1, TRACK/SS2 (Pins 45, 16): External Tracking and Soft-Start Input. The LTC7810 regulates the $V_{FB1,2}$ voltage to the lesser of 1V or the voltage on the TRACK/SS1,2 pin. An internal 10µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. The ramp time is equal to 1ms for every 10nF of capacitance. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LTC7810 output to track the other supply during startup.

NC (Pins 17, 18, 22, 23, 27, 28, 30, 31, 33, 34, 36, 38, 39, 43, 44): No Internal Connection. Float these pins or connect to ground.

TG1, TG2 (Pins 42, 19): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $DRV_{CC} – V_D$ superimposed on the switch node voltage SW, where V_D is the forward voltage drop of the external bootstrap diode.

SW1, SW2 (Pins 41, 20): Switch Node Connections to Inductors.

BOOST1, BOOST2 (Pins 40, 21): Bootstrapped Supplies to the Top Side Floating Drivers. Capacitors are connected between the BOOST and SW pins and external bootstrap diodes are tied between the BOOST and DRV_{CC} pins. Voltage swing at the BOOST pins is from DRV_{CC} to (V_{IN} + DRV_{CC}).

BG1, BG2 (Pins 37, 24): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from PGND to DRV_{CC}.

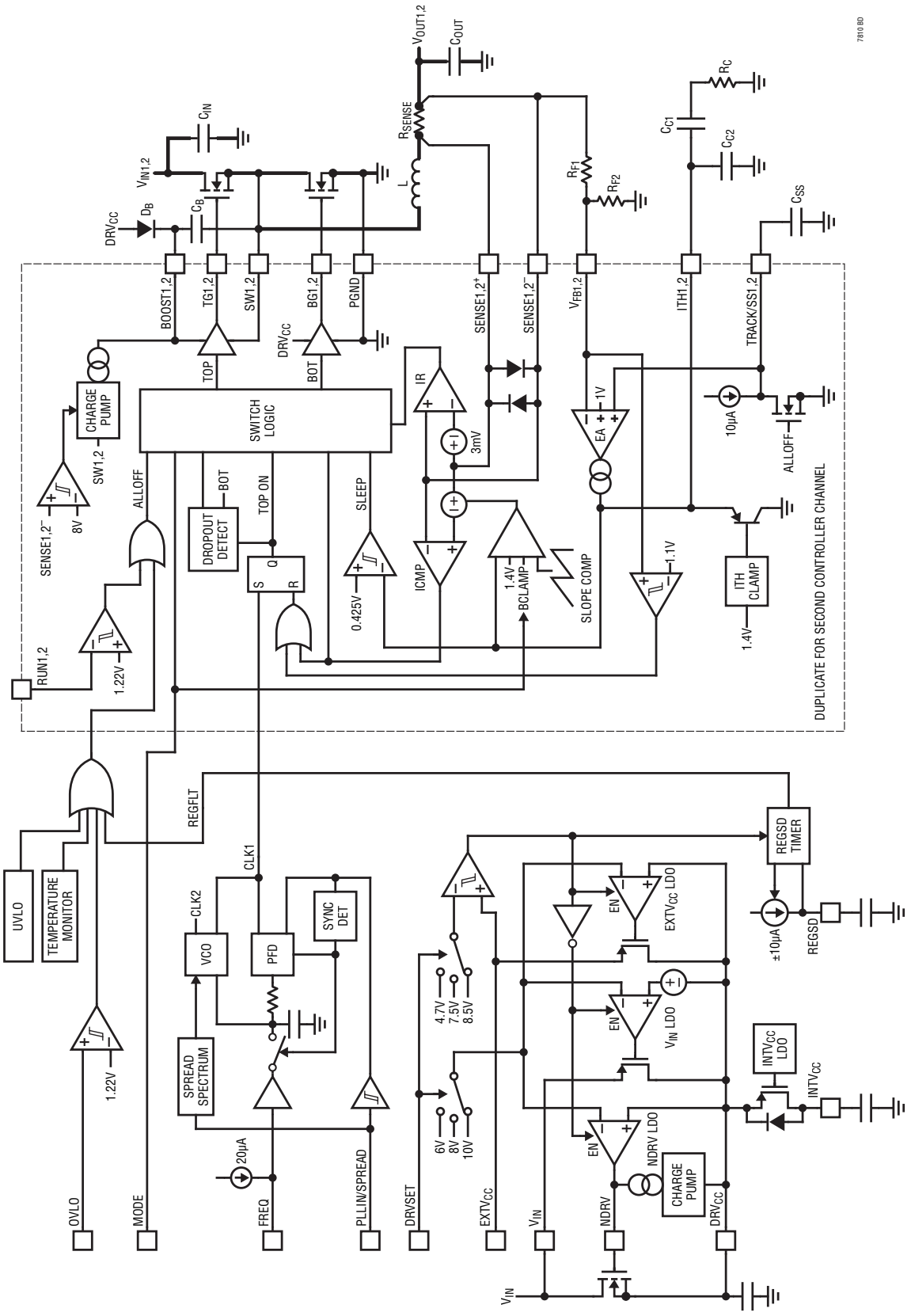
PGND (Pin 25): Driver Power Ground. Connects to the sources of bottom (synchronous) N-channel MOSFETs and the (–) terminal(s) of C_{IN}.

DRV_{CC} (Pin 26): Output of the Internal or External Low Dropout Regulator. The gate drivers are powered from this voltage source. The DRV_{CC} voltage regulation point is set by the DRVSET pin. DRV_{CC} must be decoupled to ground with a 2.2µF to 10µF ceramic or other low ESR capacitor. Do not use the DRV_{CC} pin for any other purpose.

RUN1, RUN2 (Pins 32, 29): Run Control Inputs. Forcing this pin below 1.1V disables switching of the corresponding controller. Forcing both RUN pins below 0.7V shuts down the entire LTC7810, reducing quiescent current to approximately 1.5µA. These pins can be tied to V_{IN} for always-on operation. Do not float these pins.

V_{IN} (Pin 35): Main Supply Pin. A bypass capacitor should be tied between this pin and SGND.

FUNCTIONAL DIAGRAM



OPERATION (Refer to the Functional Diagram)

Main Control Loop

The LTC7810 is a dual synchronous step-down controller utilizing a constant frequency, peak current mode control architecture. The two controller channels operate 180° out of phase which reduces the required input capacitance and power supply induced noise. During normal operation, the external top MOSFET is turned on when the clock for that channel sets the SR latch, causing the inductor current to increase. The top MOSFET is turned off when the main current comparator, ICMP, trips and resets the SR latch. After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on which causes the inductor current to decrease until either the current starts to reverse, as indicated by the reverse current comparator IR, or the beginning of the next clock cycle.

The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier, EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 1V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current matches the new load current.

Power and Bias Supplies (V_{IN}, NDRV, $EXTV_{CC}$, DRV_{CC}, REGSD)

The DRV_{CC} pin supplies power for the MOSFET drivers and can be set to 6V, 8V, or 10V depending on the state of the DRVSET pin. Three LDOs (low dropout linear regulators) are available to provide power to DRV_{CC}. The internal V_{IN} LDO powers DRV_{CC} through a P-channel pass device connected from V_{IN} to DRV_{CC}. At high input voltage, this LDO from V_{IN} dissipates significant power; therefore, to prevent high on-chip power dissipation in high input voltage applications, the LTC7810's NDRV pin can drive the gate of an external N-channel MOSFET linear regulator from V_{IN}. This NDRV LDO includes an internal charge pump that allows NDRV to be driven above V_{IN} for low dropout performance. The internal V_{IN} LDO has a slightly lower regulation point than the NDRV LDO to ensure that the external MOSFET is supplying the current to DRV_{CC}. In high voltage applications, the power dissipation in the V_{IN} and NDRV LDOs is significant and in many cases cannot be supplied indefinitely. Therefore, the LTC7810 also includes an additional $EXTV_{CC}$ LDO that can generate DRV_{CC} more efficiently from a lower voltage supply.

When $EXTV_{CC}$ is taken above its switchover voltage, the $EXTV_{CC}$ LDO turns on and powers DRV_{CC} from the $EXTV_{CC}$ pin. This allows the DRV_{CC} power to be derived from a high efficiency external source such as one of the LTC7810 switching regulator outputs. In general, the $EXTV_{CC}$ pin should be connected to an output voltage (V_{OUT1} or V_{OUT2}) that is greater than the DRV_{CC} regulation point. If both V_{OUT1} and V_{OUT2} are greater than DRV_{CC}, connect $EXTV_{CC}$ to the lesser of the two for higher efficiency and lower power dissipation.

If $EXTV_{CC}$ is below its switchover voltage (for example, if $EXTV_{CC}$ is tied to an output that is shorted to ground), the LTC7810 implements a failsafe regulator timeout to limit the power dissipation in both the internal V_{IN} LDO and the external NDRV LDO. When the DRV_{CC} bias is supplied by the V_{IN} or NDRV LDOs and the part is not in sleep mode, a 10µA current source pull-up charges an external capacitor connected to the REGSD pin. If the voltage on the REGSD exceeds 1.2V, then a regulator timeout occurs and switching of the top and bottom power MOSFETs is disabled, which dramatically reduces the power dissipation. After a long cool-down delay (approximately 29 times the REGSD charge time), a restart is initiated. This results in an "on" duty cycle of approximately 3.3% for the V_{IN} and NDRV LDOs, which reduces the steady-state power dissipation in these LDOs by a factor of 30. When $EXTV_{CC}$ is above its switchover voltage or the part is in sleep mode, the REGSD pin is discharged by a 10µA current source. In low input voltage applications, the regulator shutdown timer may not be needed and can be disabled by tying the REGSD pin to ground. See DRVCC Regulators in the Applications Information section for more information.

OPERATION

Boost Supply and Dropout (BOOST and SW pins)

Each top MOSFET driver is biased from a floating Boost Supply, consisting of the bootstrap capacitor, C_B, and external diode D_B, which normally recharges from DRV_{CC} during each cycle whenever SW goes low.

When the input voltage decreases to a voltage close to its output, the loop may enter dropout and attempt to turn on the top MOSFET continuously. If the output voltage is below 8V, the top MOSFET is forced off for about one-twelfth of the clock period every tenth cycle to allow C_B to recharge, resulting in an effective 99% maximum duty cycle.

If the output voltage on the $SENSE^-$ pins is above 8V, the LTC7810 enables an internal charge pump that allows the top MOSFET to be turned on continuously at 100% duty cycle. Furthermore, if Burst Mode is also selected (MODE ≤ 1V) and the differential SENSE pin voltage ($SENSE^+$ – $SENSE^-$) is less than 30% of $V_{SENSE(MAX)}$, the LTC7810 enters a Low I_Q Dropout mode in which the majority of internal circuitry is disabled, reducing the supply current to 45µA (one channel in dropout, one channel shutdown) or 67µA (both channels in dropout). In low I_Q dropout mode, the internal charge pump is pulsed to maintain an average gate-source voltage on the top MOSFET of 8.5V.

Start-Up and Shutdown (RUN, TRACK/SS, OVLO Pins)

The two channels of the LTC7810 can be independently shut down using the RUN1 and RUN2 pins. Pulling a RUN pin below 1.1V shuts down the main control loop for that channel. Pulling both pins below 0.7V disables both controllers and most internal circuits, including the DRV_{CC} and $INTV_{CC}$ LDOs. In this shutdown state, the LTC7810 draws only 1.5µA of quiescent current.

The RUN pins may be externally pulled up or driven directly by logic. Each pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where one or both controllers are enabled continuously and never shut down. Additionally, a resistive divider from V_{IN} to the RUN pins can be used to set a precise input undervoltage lockout so that the power supply will not operate below a user-adjustable level. Furthermore, switching is similarly inhibited if the voltage on the OVLO pin exceeds 1.22V. This pin can be configured as an input overvoltage lockout to prevent power supply operation during an overvoltage condition on the input supply. When switching is disabled by the RUN or OVLO pins, the LTC7810 can safely sustain input voltages up to the absolute maximum rating of 150V. These events trigger a soft-start reset, which results in a graceful recovery from an input supply transient. Do not float the RUN1, RUN2, or OVLO pins.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the 1V internal reference, the LTC7810 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 1V reference. This allows the TRACK/SS pin to be used as a soft-start which smoothly ramps the output voltage on startup, thereby limiting the input supply inrush current. An external capacitor from the TRACK/SS pin to GND is charged by an internal 10µA pull-up current, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 1V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively the TRACK/SS pins can be used to make the startup of V_{OUT} track that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

Light Load Operation: Burst Mode Operation, Pulse Skipping or Forced Continuous Mode (MODE Pin)

The LTC7810 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode, or forced continuous conduction mode at low load currents.

To select Burst Mode operation, tie the MODE pin to GND or a voltage between 0.5V and 1V. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a DC voltage greater than 1.1V and less than $INTV_{CC}$ – 1.3V. This can be done with a resistive divider between $INTV_{CC}$ and GND, with both resistors being 100k.

OPERATION

When a controller is enabled for Burst Mode operation, the minimum peak current in the inductor (burst clamp) is adjustable and can be programmed by the voltage on the MODE pin. Tying the MODE pin to GND sets the default burst clamp to approximately 25% of the maximum sense voltage even when the voltage on the ITH pin indicates a lower value. A voltage between 0.5V and 1V on the MODE pin programs the burst clamp linearly between 10% and 60% of the maximum sense voltage. This facilitates a trade-off between light load efficiency and output voltage ripple. Higher burst clamp levels result in higher light load efficiency, but also in higher light load output voltage ripple.

In Burst Mode operation, if the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off. The ITH pin is then disconnected from the output of the EA and parked at 0.45V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC7810 draws. If both channels are in sleep mode or if one channel is in sleep mode and the other channel is shut down, the LTC7810 draws only 40µA of quiescent current. When V_{OUT} on channel 1 is 3.2V or higher, the majority of this quiescent current is supplied by the SENSE1$^-$ pin, which further reduces the input-referred quiescent current by the ratio of V_{IN}/V_{OUT} multiplied by the efficiency.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the ITH pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates discontinuously.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference with audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the MODE pin is connected for pulse-skipping mode, the LTC7810 operates in PWM pulse-skipping mode at light loads. In this mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator, ICMP, may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Unlike forced continuous mode and pulse-skipping mode, Burst Mode cannot be synchronized to an external clock. Therefore, if Burst Mode is selected and the PLLIN/SPREAD pin is clocked to use the phase-locked loop, the LTC7810 switches from Burst Mode to forced continuous mode.

OPERATION

Frequency Selection, Spread Spectrum, and Phase-Locked Loop (FREQ and PLLIN/SPREAD Pins)

The free running switching frequency of the LTC7810 controllers is selected using the FREQ pin. Tying FREQ to GND selects 200kHz while tying FREQ to $INTV_{CC}$ selects 300kHz. Placing a resistor between FREQ and GND allows the frequency to be programmed between 50kHz and 750kHz.

Switching regulators can be particularly troublesome for applications where electromagnetic interference (EMI) is a concern. To improve EMI, the LTC7810 can operate in spread spectrum mode, which is enabled by tying the PLLIN/SPREAD pin to $INTV_{CC}$. This feature varies the switching frequency at a 4.5kHz rate with a triangular frequency modulation of ±15% of the frequency set by the FREQ pin. For example, if the LTC7810's frequency is programmed to switch at 300kHz, enabling spread spectrum will modulate the frequency between 255kHz and 345kHz at a 4.5kHz rate.

A phase-locked loop (PLL) is available on the LTC7810 to synchronize the internal oscillator to an external clock source connected to the PLLIN/SPREAD pin. The LTC7810's phase detector (PFD) and low pass filter adjust the voltage of the VCO input to align the turn-on of controller 1's external top MOSFET to the rising edge of the synchronizing signal. Thus, the turn-on of controller 2's external top MOSFET is 180° out-of-phase to the rising edge of the external clock source.

The VCO input voltage is prebiased to the free running frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock to the rising edge of TG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency. The LTC7810's PLL is guaranteed to lock to an external clock source whose frequency is between 75kHz and 720kHz. The PLLIN/SPREAD pin is TTL compatible with thresholds of 1.6V (rising) and 1.1V (falling) and is guaranteed to operate with a clock signal swing of 0.5V to 2.5V.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC7810 application circuit. External component selection is largely driven by the load requirement and begins with the selection of the current sense components, operating frequency, and light load operating mode. The power stage components, consisting of the inductor, input and output capacitors, and power MOSFETs can then be chosen. Next, feedback resistors are selected to set the desired output voltage. Then, the remaining external components are selected, such as for V_{IN} undervoltage/overvoltage lockout, soft-start, DRV_{CC} bias, and loop compensation.

Current Sense Selection

The LTC7810 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing has become popular because it saves expensive current sensing resistors and is more power efficient, particularly in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value.

The $SENSE^+$ and $SENSE^-$ pins are the inputs to the current comparators. The common mode voltage range on these pins is 0V to 65V (absolute maximum), enabling the LTC7810 to regulate output voltages up to a nominal 60V (allowing margin for tolerances and transients). The $SENSE^+$ pin is high impedance, drawing less than ≈1µA. This high impedance allows the current comparators to be used in inductor DCR sensing. The impedance of the $SENSE^-$ pin changes depending on the common mode voltage. When $SENSE^-$ is less than $INTV_{CC}$ – 0.5V, it is relatively high impedance, drawing ≈4µA. When $SENSE^-$ is above $INTV_{CC}$ + 0.5V, a higher current (≈480µA) flows into the pin. Between $INTV_{CC}$ – 0.5V and $INTV_{CC}$ + 0.5V, the current transitions from the smaller current to the higher current. Channel 1's $SENSE1^-$ has an additional ≈60µA current when its voltage is above 3.2V to bias internal circuitry from V_{OUT1}, thereby reducing the effective input supply current.

Filter components mutual to the sense lines should be placed close to the LTC7810, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

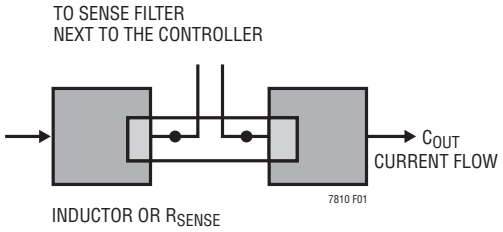


Figure 1. Sense Lines Placement with Inductor or Sense Resistor

Low Value Resistor Current Sensing

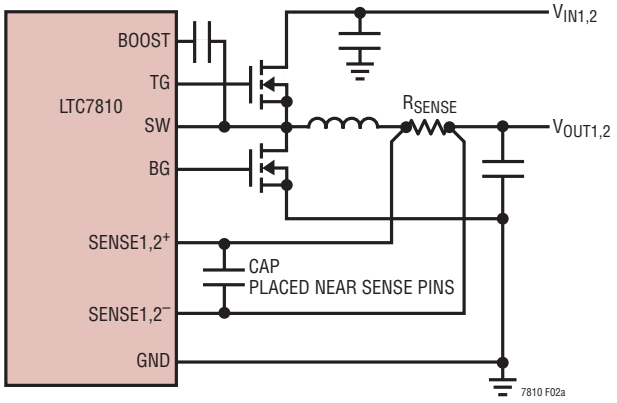
A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current. Each controller's current comparator has a threshold $V_{SENSE(MAX)}$ of 75mV. The current comparator threshold voltage sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}} \quad (1)$$

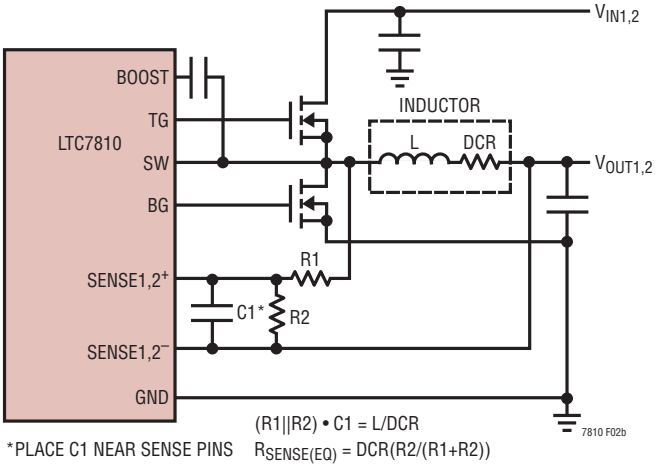
Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC7810 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor,

APPLICATIONS INFORMATION



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Current Sensing Methods

power loss through a sense resistor would cost several points of efficiency compared to inductor DCR sensing.

If the external (R1||R2)•C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}} \quad (2)$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for $V_{SENSE(MAX)}$ in the Electrical Characteristics table.

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of copper resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. To scale the maximum inductor DCR to the desired sense resistor value (R_D), use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}} \quad (3)$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pin's ±1µA current.

The equivalent resistance R1||R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1} \quad (4)$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D} \quad (5)$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS\ R1} = \frac{(V_{IN(MAX)} - V_{OUT}) \bullet V_{OUT}}{R1} \quad (6)$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing

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or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Setting the Operating Frequency

Selection of the operating frequency is a trade-off between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing gate charge and transition losses, but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

For most LTC7810 applications, a good balance between size and efficiency is achieved with a switching frequency between 150kHz and 350kHz. Operating at higher switching frequencies up to 750kHz is readily possible, but switching losses generally limit the input voltage to lower levels. The switching frequency is set using the FREQ and PLLIN/SPREAD pins as shown in Table 1.

Table 1.

FREQ PIN	PLLIN/SPREAD PIN	FREQUENCY
0V	0V	200kHz
$INTV_{CC}$	0V	300kHz
Resistor to GND	0V	50kHz to 750kHz
Any of the Above	External Clock 75kHz to 720kHz	Phase-Locked to External Clock
Any of the Above	$INTV_{CC}$	Spread Spectrum f_{OSC} modulated ±15%

Tying the FREQ pin to ground selects 200kHz while tying FREQ to $INTV_{CC}$ selects 300kHz. Since the FREQ pin sources 20µA, placing a resistor between FREQ and ground allows the frequency to be programmed anywhere between 50kHz and 750kHz. Choose a FREQ pin resistor from Figure 3 or the following equation:

$$R_{FREQ} = \frac{f_{OSC}}{9} + 13.5k \quad (7)$$

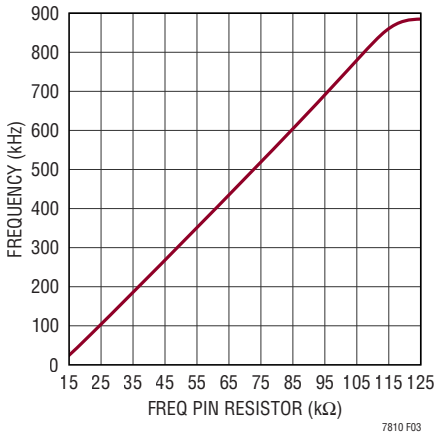

Figure 3. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

To improve EMI, spread spectrum mode can optionally be selected by tying the PLLIN/SPREAD pin to $INTV_{CC}$. When spread spectrum is enabled, the switching frequency varies with a 4.5kHz triangular modulation to ±15% of the frequency selected by the FREQ pin. Spread spectrum may be used in any operating mode selected by the MODE pin (Burst Mode, pulse-skipping, or forced continuous mode).

A phase-locked loop (PLL) is also available on the LTC7810 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/SPREAD pin. Once synchronized, TG1 is aligned to the rising edge of the synchronizing signal. See the Phase-Locked Loop and Frequency Synchronization section for details.

Selecting the Light-Load Operating Mode

The LTC7810 can be set to enter high efficiency Burst Mode operation, constant frequency pulse-skipping mode or forced continuous conduction mode at light load currents. To select Burst Mode operation with default burst clamp (25% of $V_{SENSE(MAX)}$), tie the MODE pin to ground. To linearly adjust the burst clamp between 10% and 60%, tie the mode pin to a voltage between 0.5V (10% burst clamp) and 1V (60% burst clamp). See the Burst Clamp Programming section for more information. To select forced continuous operation, tie the MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the MODE pin to a divider comprised of two 100k resistors from $INTV_{CC}$ to

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ground. When synchronized to an external clock through the PLLIN/SPREAD pin, if Burst Mode or forced continuous operation is selected, the LTC7810 operates in forced continuous mode. If pulse-skipping is selected, the LTC7810 remains in pulse-skipping. Table 2 summarizes the use of the MODE pin to select light load operating mode.

Table 2.

MODE PIN	LIGHT-LOAD OPERATING MODE	MODE WHEN SYNCHRONIZED
0V	Burst Mode 25% Burst Clamp	Forced Continuous Mode
0.5V to 1V	Burst Mode 10% to 60% Burst Clamp	Forced Continuous Mode
2.25V (100k Divider from $INTV_{CC}$)	Pulse-Skipping Mode	Pulse-Skipping Mode
$INTV_{CC}$	Forced Continuous Mode	Forced Continuous Mode

In general, the requirements of each application will dictate the appropriate choice for light-load operating mode. In Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator turns off the bottom MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the regulator operates in discontinuous operation. In addition, when the load current is very light, the inductor current will begin bursting at frequencies lower than the switching frequency, and enter a low current sleep mode when not switching. As a result, Burst Mode operation has the highest possible efficiency at light load.

In forced continuous mode, the inductor current is allowed to reverse at light loads and switches at the same frequency regardless of load. In this mode, the efficiency at light loads is considerably lower than in Burst Mode operation. However, continuous operation has the advantage of lower output voltage ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

In pulse-skipping mode, constant frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the PWM comparator may remain tripped for several cycles and force the top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation. Consequently, pulse-skipping mode represents a compromise between light load efficiency, output ripple and EMI.

In some applications, it may be desirable to change light load operating mode based on the conditions present in the system. For example, if a system is inactive, one might select high efficiency Burst Mode operation by keeping the MODE pin set to 0V. When the system wakes, one might send an external clock to PLLIN/SPREAD, or tie MODE to $INTV_{CC}$ to switch to low noise forced continuous mode. Such on-the-fly mode changes can allow an individual application to benefit from the advantages of each light-load operating mode.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET switching and gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, decreases with higher inductance or higher frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below

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the burst clamp, which can be programmed between 10% and 60% of the current limit determined by R_{SENSE}. (For more information see the Burst Clamp Programming section.) Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency regulators generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance value selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred for high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates hard, which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET Selection

Two external power MOSFETs must be selected for each controller in the LTC7810: one N-channel MOSFET for the top (main) switch and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the DRV_{CC} voltage. This voltage can be set to 6V, 8V, or 10V depending on configuration of the DRVSET pin. Therefore, both logic-level and standard-level threshold MOSFETs can be used in most applications depending on the programmed DRV_{CC} voltage. Pay close attention to the BV_{DSS} specification for the MOSFETs as well.

Selection criteria for the power MOSFETs include the on resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$
$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \quad (9)$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{OUT(MAX)}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{DRVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$
$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(I_{OUT(MAX)}\right)^2(1+\delta)R_{DS(ON)} \quad (10)$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the main N channel equations include an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty cycle is low

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or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the two-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula shown in Equation 11 to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2} \quad (11)$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC7810, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The benefit of the LTC7810 two-phase operation can be calculated by using Equation 11 for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the reduced overlap of current pulses required through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Also, the input protection fuse resistance, battery resistance, and PC board trace resistance losses are also reduced due to the reduced peak currents in a two-phase system. The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing. The drains of the top MOSFETs should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}. A small (0.1µF to 1µF) bypass capacitor between the chip V_{IN} pin and ground, placed close to the LTC7810, is also suggested. An optional 2.2Ω to 10Ω resistor placed between C_{IN} and the V_{IN} pin provides further isolation from a noisy input supply.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx \Delta I_L\left(ESR + \frac{1}{8 \bullet f \bullet C_{OUT}}\right) \quad (12)$$

where f is the operating frequency, C_{OUT} is the output capacitance and ΔI_L is the ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Setting the Output Voltage

The LTC7810 output voltages are each set by an external feedback resistor divider carefully placed across the output, as shown in Figure 4 The regulated output voltage is determined by:

$$V_{OUT} = 1V\left(1 + \frac{R_B}{R_A}\right) \quad (13)$$

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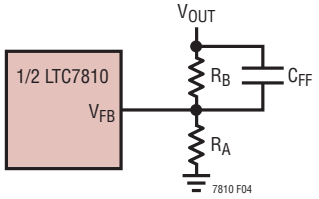

Figure 4. Setting the Output Voltage

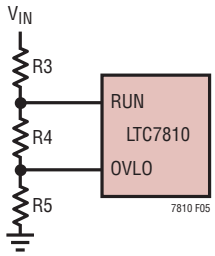

Figure 5. Adjustable UV and OV Lockout

To improve the frequency response, a feedforward capacitor, C_{FF} , may be used. Great care should be taken to route the V_{FB} lines away from noise sources, such as the inductor or the SW lines.

For applications with multiple output voltage levels, select channel 1 to be the lowest output voltage that is greater than 3.2V. When the SENSE1$^-$ pin (connected to V_{OUT1}) is above 3.2V, it (instead of V_{IN}) biases some internal circuitry, thereby increasing light load Burst Mode efficiency. Similarly, connect $EXTV_{CC}$ to the lowest output voltage that is greater than the selected DRV_{CC} regulation point. $EXTV_{CC}$ is then used to supply the high current gate drivers as well as to relieve additional quiescent current from V_{IN}, further reducing the V_{IN} pin current to 4µA in sleep.

RUN Pins and Overvoltage/Undervoltage Lockout

The LTC7810 is enabled using the RUN1 and RUN2 pins. The RUN pins have a rising threshold of 1.22V with 120mV of hysteresis. Pulling a RUN pin below 1.1V shuts down the main control loop and resets the soft-start for that channel. Pulling both RUN pins below 0.7V disables the controllers and most internal circuits, including the DRVCC and $INTV_{CC}$ LDOs. In this state, the LTC7810 draws only 1.5µA of quiescent current.

The RUN pins are high impedance must be externally pulled up/down or driven directly by logic. Each RUN pin can tolerate up to 150V (absolute maximum), so it can be conveniently tied to V_{IN} in always-on applications where the controller is enabled continuously and never shut down. Do not float the RUN pins.

The OVLO pin operates in a similar but inverted fashion to the RUN pins. Both channels of the LTC7810 are disabled when the OVLO pin rises above its threshold of 1.22V with 65mV of hysteresis. Soft-start is reset following an OVLO event, resulting in a graceful recovery from an input supply transient. The OVLO pin is high impedance and must be kept below its absolute maximum rating of 6V. A Zener diode clamp should be placed on the OVLO pin if its 6V rating becomes a limitation. The OVLO pin must be grounded if it is not used.

The RUN and OVLO pins can be configured as undervoltage (UVLO) and overvoltage (OVLO) lockouts on the V_{IN} supply with a resistor divider from V_{IN} to ground. A simple resistor divider can be used as shown in Figure 5 to meet specific V_{IN} voltage requirements.

The current that flows through the R3-R4-R5 divider will directly add to the shutdown, sleep, and active current of the LTC7810, and care should be taken to minimize the impact of this current on the overall efficiency of the application circuit. Resistor values in the MΩ range may be required to keep the impact on quiescent shutdown and sleep currents low. To pick resistor values, the sum total of R3 + R3 + R5 (R_{TOTAL}) should be chosen first based on the allowable DC current that can be drawn from V_{IN}.

The individual values of R3, R4 and R5 can be calculated from the following equations:

$$R5 = R_{TOTAL} \bullet \frac{1.22V}{\text{Rising } V_{IN} \text{ OVLO Threshold}}$$

$$R4 = R_{TOTAL} \bullet \frac{1.22V}{\text{Rising } V_{IN} \text{ UVLO Threshold}} - R5 \qquad (14)$$

$$R3 = R_{TOTAL} - R5 - R4$$

For applications that do not require a precise OVLO, the OVLO pin can be tied directly to ground. The RUN pin in this type of application can be used as an external UVLO using the previous equations with R5 = 0Ω.

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Similarly, for applications that do not require a precise UVLO, the RUN pin can be tied to V_{IN}. In this configuration, the UVLO threshold is limited to the internal DRVCC UVLO thresholds as shown in the Electrical Characteristics table. The resistor values for the OVLO can be computed using the previous equations with R3 = 0Ω.

Tracking and Soft-Start (TRACK/SS1, TRACK/SS2 Pins)

The start-up of each V_{OUT} is controlled by the voltage on the TRACK/SS pin (TRACK/SS1 for channel 1, TRACK/SS2 for channel 2). When the voltage on the TRACK/SS pin is less than the internal 1V reference, the LTC7810 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of the internal reference. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to track another supply during start-up.

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 6. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC7810 will regulate its feedback voltage (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. For a desired soft-start time, t_{SS}, select a soft-start capacitor $C_{SS} = t_{SS} \bullet 10\mu F/sec$.

Alternatively, the TRACK/SS1 and TRACK/SS2 pins can be used to track two (or more) supplies during start-up, as shown qualitatively in Figure 7a and Figure 7b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 8. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B} \qquad (15)$$

For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$

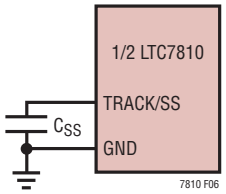
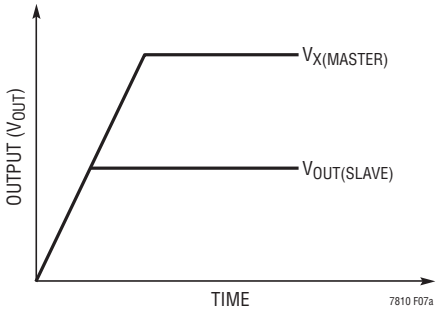
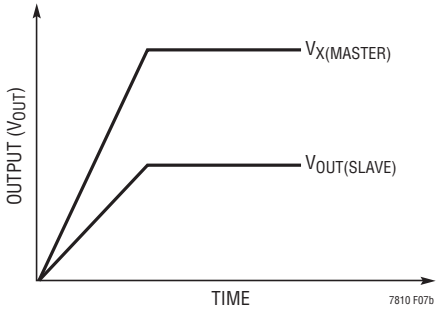


Figure 6. Using the TRACK/SS Pin to Program Soft-Start



(7a) Coincident Tracking



(7b) Ratiometric Tracking

Figure 7. Two Different Modes of Output Voltage Tracking

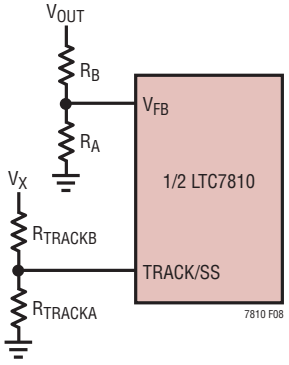


Figure 8. Using the TRACK/SS Pin for Tracking

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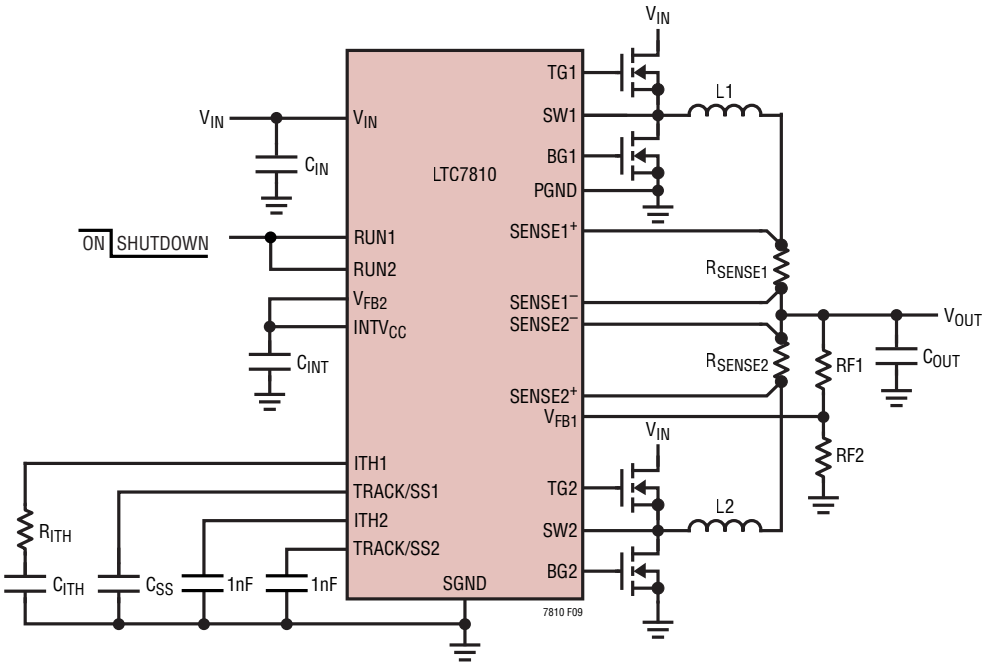

Figure 9. Single Output Two-Phase Operation

Single Output Two-Phase Operation

For high power applications, the two channels can be operated in a two-phase single output configuration. The two channels switch 180° out-of-phase, which reduces the required output capacitance in addition to the required input capacitance and power supply induced noise. To configure the LTC7810 for two-phase operation, tie V_{FB2} to $INTV_{CC}$ and RUN2 to RUN1. To prevent high frequency noise from coupling into the unused ITH2 and TRACK/SS2 pins, either tie them to ground or, for lower burst mode quiescent current, place 1nF capacitors from these pins to ground. The RUN1, V_{FB1}, ITH1, TRACK/SS1 pins are then used to control both channels, but each channel uses its own ICMP and IR comparators to monitor their respective inductor currents. Figure 9 shows the connections for single output two-phase operation.

DRV_{CC} Regulators

The LTC7810 features three separate low dropout linear regulators (LDO) that can supply power at the DRV_{CC} pin. The internal V_{IN} LDO uses an internal P-channel pass device between the V_{IN} and DRV_{CC} pins. The internal $EXTV_{CC}$ LDO uses an internal P-channel pass device between the $EXTV_{CC}$ and DRV_{CC} pins. The NDRV LDO utilizes the NDRV pin to drive the gate of an external N channel MOSFET acting as a linear regulator with its drain connected to V_{IN}.

The NDRV LDO provides an alternative method to supply power to DRV_{CC} from the input supply without dissipating the power inside the LTC7810 IC. It has an internal charge pump that allows NDRV to be driven above the V_{IN} supply, allowing for low dropout performance. The V_{IN} LDO has a slightly lower regulation point than the NDRV LDO, such that all DRV_{CC} current flows through the external N-channel MOSFET (and not through the internal P-channel pass device) when DRV_{CC} reaches regulation. Do not float the NDRV pin. If the NDRV LDO is not being used, short NDRV to DRV_{CC}. When laying out the PC board, care should be taken to route NDRV away from any switching nodes, such as SW, TG, and BOOST. Coupling to the NDRV node could cause its voltage to collapse and the NDRV LDO to lose regulation. If this occurs, the internal V_{IN} LDO would take over and maintain DRV_{CC} voltage at a slightly lower regulation point. However, internal heating of the IC would become a concern.

High frequency noise from the V_{IN} supply could also couple into the NDRV node through the gate-to-drain capacitance of the MOSFET and adversely affect NDRV regulation. The following are methods that could mitigate this potential

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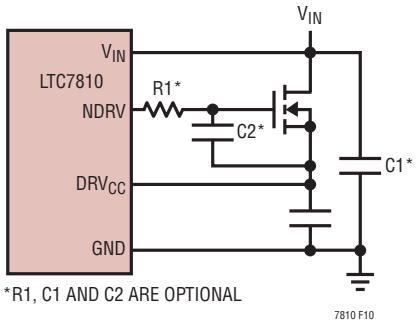

Figure 10. Configuring the NDRV LDO

issue (refer to Figure 10): 1) Add local decoupling capacitors right next to the drain of the external NDRV N-channel MOSFET in the PCB layout; 2) Insert a resistor (~100Ω) in series with the gate of the NDRV MOSFET; 3) Insert a small capacitor (~1nF) between the gate and source of the NDRV MOSFET. When testing the application circuit, be sure the NDRV voltage does not collapse over the entire input voltage and output current operating range of the buck regulators.

The DRV_{CC} regulation point is set to 6V, 8V, or 10V based on the state of the DRVSET pin. Tie DRVSET to $INTV_{CC}$ to select 6V, to GND to select 8V, or float it to select 10V. Select the regulation point based on the MOSFETs that are used in the application. The regulation point should be set high enough to be above the "knee" in the MOSFET I_D vs V_{GS} curve. Setting the regulation point too low results in excess power loss in the MOSFETs due to I^2R losses. Setting the regulation point too high results in excess power loss due to the additional gate charge required to switch the MOSFETs. The optimum regulation point can be selected by comparing the input supply current at a specific operating point. The DRV_{CC} UVLO thresholds and $EXTV_{CC}$ switchover thresholds adjust correspondingly to the selected regulation point and are summarized in Table 3.

Table 3.

DRVSET PIN	NDRV AND $EXTV_{CC}$ LDO REGULATION POINT	INTERNAL V_{IN} LDO REGULATION POINT	DRV_{CC} UVLO RISING THRESHOLDS	$EXTV_{CC}$ SWITCHOVER RISING THRESHOLDS
$INTV_{CC}$	6V	5.8V	4.2V	4.7V
GND	8V	7.7V	5.5V	7.5V
FLOATING	10V	9.6V	7.5V	8.5V

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC7810 to be exceeded. The DRV_{CC} current, which is dominated by the gate charge current, may be supplied by the V_{IN} LDO, NDRV LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than its switchover threshold (4.7V, 7.5V, or 8.5V as determined by the DRVSET pin described above), the V_{IN} and NDRV LDOs are enabled. Power dissipation in this case is highest and is equal to $V_{IN} \bullet I_{DRVCC}$. If the NDRV LDO is not being used, this power is dissipated inside the IC. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, if DRV_{CC} is set to 6V, the DRV_{CC} current is limited to less than 38mA from a 72V supply when not using the $EXTV_{CC}$ supply at a 70°C ambient temperature:

$$T_J = 70°C + (38mA)(72V)(20°C/W) = 125°C \qquad (16)$$

To prevent the maximum junction temperature from being exceeded, the V_{IN} supply current must be checked while operating in forced continuous mode (MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above its switchover threshold, the V_{IN} LDO and NDRV LDOs are turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above the switchover threshold minus the comparator hysteresis. The $EXTV_{CC}$ LDO attempts to regulate the DRV_{CC} voltage to the voltage as programmed by the DRVSET pin, so while $EXTV_{CC}$ is less than this voltage, the LDO is in dropout and the DRV_{CC} voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than the programmed voltage, up to an absolute maximum of 65V, DRV_{CC} is regulated to the programmed voltage.

Significant efficiency and thermal gains can be realized by powering DRV_{CC} from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

This is accomplished by tying the $EXTV_{CC}$ pin directly to an output voltage that is greater than the DRV_{CC} regulation

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point. If both V_{OUT1} and V_{OUT2} are greater than the DRV_{CC} regulation point, tie $EXTV_{CC}$ to the lesser of the two for lowest power dissipation. The $EXTV_{CC}$ pin's absolute maximum voltage of 65V enables it to be connected to an output in nearly any application. $EXTV_{CC}$ may also be connected to any other supply in the system that is higher than the DRV_{CC} regulation point and capable of providing the MOSFET gate drive current.

For the previous example, tying the $EXTV_{CC}$ pin to a 12V supply reduces the junction temperature from 125°C to:

$$T_J = 70°C + (38mA)(12V)(20°C/W) = 79°C \quad (17)$$

In applications where both outputs are less than the DRV_{CC} regulation point, and no other supply available in the system, additional circuitry is required to derive DRV_{CC} power from the output.

Using the $EXTV_{CC}$ LDO allows the MOSFET driver and control power to be derived from one of the LTC7810's switching regulator outputs during normal operation and from the V_{IN} LDO or NDRV LDO when the output is out of regulation (e.g., start-up, short-circuit).

For a condition that keeps $EXTV_{CC}$ below its switchover threshold for a long period of time, such as a persistent short-circuit, the LTC7810 provides a regulator shutdown timeout to limit excessive power dissipation from the V_{IN} supply. When DRV_{CC} is supplied by the V_{IN} or NDRV LDOs and the part is not in sleep mode, a 10µA current source out of the REGSD pin charges an external capacitor. When the voltage on the REGSD pin reaches 1.2V, a regulator timeout fault occurs and switching stops. After a long cool-down delay (approximately 29 times the length of the initial timeout) during which the REGSD pin is cycled between 0.2V and 1.2V, a restart is initiated. When the LTC7810 is in Burst Mode and goes to sleep, or if $EXTV_{CC}$ rises above its switchover voltage, no significant power is being dissipated in the V_{IN} or NDRV LDOs, and the REGSD pin is therefore discharged with a 10µA current.

Figure 11 shows the REGSD connection. Be sure to select the REGSD timeout to be longer than it takes for the output voltage to reach the $EXTV_{CC}$ switchover threshold during soft-start. This is accomplished by selecting the value of C_{REGSD} to be greater than or equal to the value of the soft-start capacitor for the channel that $EXTV_{CC}$ is tied

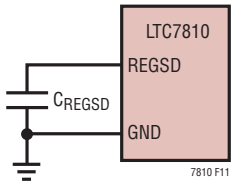

Figure 11. Using the REGSD Pin

to. For low voltage applications where power dissipation from V_{IN} is not significant, the regulator shutdown timer can be disabled by grounding the REGSD pin.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. This will cause DRV_{CC} to be powered from the internal V_{IN} or NDRV LDO resulting in an efficiency penalty at high input voltages. If $EXTV_{CC}$ is grounded, the REGSD feature must be defeated by grounding the REGSD pin.
2. $EXTV_{CC}$ connected directly to one of the LTC7810's outputs. This is the normal connection for an application with an output greater than the DRV_{CC} regulation point and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If an external supply is available, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements. This supply may be higher or lower than V_{IN}; however, if the NDRV LDO is also used and V_{IN} is lower than DRV_{CC}, keep in mind that the external NMOS has a body diode from DRV_{CC} to V_{IN}, and may require a diode in series with its drain to avoid back-biasing V_{IN} from DRV_{CC}.
4. $EXTV_{CC}$ connected to an output-derived boost or charge pump. For regulators where both of the LTC7810 outputs are low voltage, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than the DRV_{CC} regulation point.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode D_B from DRV_{CC} when

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the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the top MOSFET switch and turns it on. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external diode must be greater than $V_{IN(MAX)}$.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low-leakage and fast recovery. Pay close attention to the reverse leakage current specification for this diode, especially at high temperatures where it generally increases substantially.

The topside MOSFET drivers include internal charge pumps that deliver current to the bootstrap capacitor when the top MOSFET is on continuously, such as when the output is in dropout (100% duty cycle). The diode selected for the boost topside driver should have a reverse leakage less than the available output current the charge pump can supply. Curves displaying the available charge pump current under different operating conditions can be found in the Typical Performance Characteristics section.

A leaky diode D_B can not only prevent the top MOSFET from fully turning on but it can also create a current path from the BOOST pin to DRV_{CC}. This can cause DRV_{CC} to rise if the diode leakage exceeds the current consumption on DRV_{CC}. This is particularly a concern in Burst Mode operation where the load on DRV_{CC} can be very small. There is an internal voltage clamp on DRV_{CC} that prevents the DRV_{CC} voltage from running away, but this clamp should be regarded as a failsafe only. The external Schottky or silicon diode should be carefully chosen such that DRV_{CC} never gets charged up higher than its normal regulation voltage.

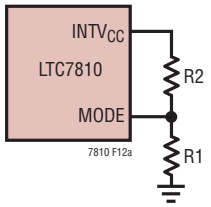
Burst Clamp Programming

Burst Mode operation is enabled if the voltage on the MODE pin is 0V or in the range between 0.5V to 1V. The burst clamp, which sets the minimum peak inductor current, can be programmed by the MODE pin voltage. If the MODE pin is grounded, the burst clamp is set to 25% of the maximum sense voltage ($V_{SENSE(MAX)}$). A MODE pin voltage between 0.5V and 1V varies the burst clamp linearly between 10% and 60% of $V_{SENSE(MAX)}$ through the following equation:

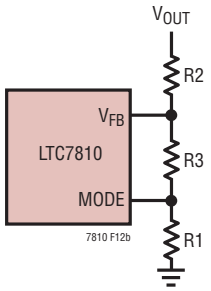
$$\text{BURST CLAMP} = \frac{V_{MODE} - 0.4V}{1V} \bullet 100\% \qquad (18)$$

where V_{MODE} is the voltage on the MODE pin and burst clamp is the percentage of $V_{SENSE(MAX)}$. The burst clamp level facilitates a trade-off between light load efficiency and light load output voltage ripple. Higher burst clamp levels increase the output voltage ripple due to higher peak inductor currents, but also increase the sleep time between burst pulses which increases efficiency.

The MODE pin is high impedance and V_{MODE} can be set by a resistor divider from the $INTV_{CC}$ pin (Figure 12a). As a lower quiescent current alternative, the MODE pin can be connected to either V_{FB} feedback divider by use of a third divider resistor (R3) as shown in Figure 12b to program the burst clamp between 10% and 60% (V_{MODE} = 0.5V to 1V). In the configuration of Figure 12b, when



(12a) Using $INTV_{CC}$ to Program the Burst Clamp



(12b) Using V_{FB} to Program the Burst Clamp

Figure 12. Programming the Adjustable Burst Clamp

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the output voltage is in regulation, the output voltage and MODE pin voltage are:

$$V_{OUT} = 1V\left(1+\frac{R2}{R1+R3}\right)$$
$$V_{MODE} = 1V\left(\frac{R1}{R1+R3}\right) \quad (19)$$

Fault Conditions: Current Limit and Current Foldback

The LTC7810 includes current foldback to help limit load current when the output is shorted to ground. If the output voltage falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100% to 40% of its maximum selected value. Under short-circuit conditions with very low duty cycles, the LTC7810 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC7810 (≈90ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)}\left(\frac{V_{IN}}{L}\right) \quad (20)$$

The resulting average short-circuit current is:

$$I_{SC} = 40\% \bullet I_{LIM(MAX)} - \frac{1}{2}\Delta I_{L(SC)} \quad (21)$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator detects faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the overvoltage condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes.

A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self-heating on chip, the overtemperature shutdown circuitry will shut down the LTC7810. When the junction temperature exceeds approximately 180°C, the overtemperature circuitry disables the DRV_{CC} LDO, causing the DRV_{CC} supply to collapse and effectively shut down the entire LTC7810 chip. When the junction temperature drops back to the approximately 160°C, the DRV_{CC} LDO turns back on. Long-term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Phase-Locked Loop and Frequency Synchronization

The LTC7810 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a low pass filter, and a voltage-controlled oscillator (VCO). This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN/SPREAD pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock. If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input.

If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector

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output is high impedance and the internal filter capacitor, CLP, holds the voltage at the VCO input.

Note that the LTC7810 can only be synchronized to an external clock whose frequency is within range of the LTC7810's internal VCO, which is nominally 50kHz to 750kHz. This is guaranteed to be between 75kHz and 720kHz. Typically, the external clock (on the PLLIN/SPREAD pin) input high threshold is 1.6V, while the input low threshold is 1.1V. The LTC7810 is guaranteed to synchronize to an external clock that swings up to at least 2.5V and down to 0.5V or less.

Rapid phase-locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free running frequency be near the external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

When synchronized to an external clock, the LTC7810 operates in forced continuous mode if the MODE pin is set to Burst Mode operation or forced continuous operation. If the MODE pin is set to pulse-skipping operation, the LTC7810 maintains pulse-skipping operation when synchronized.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC7810 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)} \quad (22)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC7810 is approximately 90ns. However, as the peak sense voltage decreases, the minimum on-time gradually increases up to about 130ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC7810 circuits: 1) IC V_{IN} current, 2) DRV_{CC} regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. DRV_{CC} current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from DRV_{CC} to ground. The resulting dQ/dt is a current out of DRV_{CC} that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

   Supplying DRV_{CC} from an output-derived source power through $EXTV_{CC}$ will scale the V_{IN} current required for the driver and control circuits by a factor of (Duty Cycle)/(Efficiency). For example, in a 20V to 5V

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application, 10mA of DRV_{CC} current results in approximately 2.5mA of V_{IN} current. This reduces the mid-current loss from 10% or more (if the driver was powered directly from V_{IN}) to only a few percent.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is chopped between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 30mΩ, R_L = 50mΩ, R_{SENSE} = 10mΩ and R_{ESR} = 40mΩ (sum of both input and output capacitance losses), then the total resistance is 130mΩ. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the top MOSFET(s), and become significant only when operating at high input voltages (typically 20V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = 1.7 \bullet V_{IN}^2 \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f \quad (23)$$

Other hidden losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these system level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD(ESR)}$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC-coupled and AC-filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the first page circuit will provide an adequate starting point for most applications.

The ITH series RC-CC filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be

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used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing RC and the bandwidth of the loop will be increased by decreasing C_C. If RC is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise-time should be controlled so that the load rise-time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 48V (nominal), V_{IN} = 140V (max), V_{OUT} = 12V, $I_{OUT(MAX)}$ = 6A, and f = 150kHz. The schematic representing this design example is shown as channel 2 in Figure 14 in the Typical Applications section.

1. Set the operating frequency. Since the input can be high voltage, a low switching frequency is selected to minimize transition losses on the top MOSFET. The operating frequency is not one of the internal preset values of 200kHz or 300kHz, so a resistor from the FREQ pin to GND is required, with a value of:

$$R_{FREQ} = \frac{150kHz}{9} + 13.5k = 30.2k\Omega \quad (24)$$

2. Determine the inductor value. Initially select a value based on an inductor ripple current of 30%. The inductor ripple current can be calculated from the following equation:

$$L = \frac{V_{OUT}}{(f)(\Delta I_L)}\left(1 - \frac{V_{OUT}}{V_{IN(NOM)}}\right) = 33\mu H \quad (25)$$

The highest value of ripple current occurs at the maximum input voltage, in this case, the ripple at V_{IN} = 140V is 37%.

3. Verify that the minimum on-time of 90ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}(f)} = 571ns \quad (26)$$

This is more than sufficient to satisfy the minimum on-time requirement. If the minimum on-time were violated, either the frequency could be decreased (with inductor value accordingly adjusted) or the OVLO pin could be used to limit the maximum input voltage where switching occurs.

4. Select the R_{SENSE} resistor value. The peak inductor current is the maximum DC output current plus half of the inductor ripple current. Or (6A)(1 + 0.30/2) = 6.9A in this case. The R_{SENSE} resistor value can then be calculated based on the minimum value for the maximum current sense threshold (67mV):

$$R_{SENSE} \leq \frac{67mV}{6.9A} \cong 10m\Omega \quad (27)$$

5. Select the feedback resistors. If very light load efficiency is required, high value feedback resistors may be used to minimize the current due to the feedback divider. However, in most applications a feedback divider current in the range of 10µA to 100µA or more is acceptable. For a 50µA feedback divider current, R_A = 1V/50µA = 20kΩ. R_B can then be calculated as:

$$R_B = R_A\,(12V - 1V) = 220k\Omega \quad (28)$$

6. Select the MOSFETs. The best way to evaluate MOSFET performance in a particular application is to build and test the circuit on the bench which is facilitated by an LTC7810 demo board. However, an educated guess about the application is helpful to initially select

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MOSFETs. Since this is a high input voltage application, transition losses will likely dominate the power loss in the top MOSFET. Therefore, choose a MOSFET with low gate charge to minimize this loss term, such as an Infineon BSC520N15NS3G which has low gate charge, a V_{DS} rating of 150V, $R_{DS(ON)}$ of 52mΩ, and a maximum drain current of 21A. Due to the high transition losses that occur with a 140V input voltage, two MOSFETs may needed in parallel to more evenly balance the dissipated power and to lower the $R_{DS(ON)}$.

The bottom MOSFET does not experience transition losses, and its power loss is generally dominated by I^2R losses. For this reason, the bottom MOSFET is typically chosen to be of lower $R_{DS(ON)}$ and subsequently higher gate charge than the top MOSFET. For this example, an Infineon BSC093N15NS5 is chosen with an $R_{DS(ON)}$ of just 9mΩ.

The DRVSET pin for these MOSFETs should be configured for either 8V or 10V to avoid the "knee" in the MOSFET I_D vs V_{GS} curve. Losses due to the gate charge required to turn on the MOSFETs may be greater with DRV_{CC} set to 10V, but I^2R losses may decrease; therefore, both configurations of the DRVSET pin should be attempted in the lab to determine the most efficient operating point.

7. Select the input and output capacitors. C_{IN} is chosen for an RMS current rating of at least 4A ($I_{OUT}/2$, with margin) at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

   $$V_{ORIPPLE} = R_{ESR} \bullet \Delta I_L = 0.02\Omega \bullet 1.8A = 36mV_{P-P} \quad (29)$$

   On the 12V output, this is equal to 0.30% of peak to peak voltage ripple.

8. Determine the bias supply components. Since the regulated output is greater than the DRV_{CC} regulation point, tie $EXTV_{CC}$ to V_{OUT} to supply the gate drive current from the output. For a 10ms soft start, select a 0.1µF capacitor for the TRACK/SS pin. Select a 0.33µF capacitor for the REGSD pin for a 40ms REGSD timeout, which is longer than the soft-start time to ensure that the output has an opportunity to start up before the regulator shutdown timer expires. As a first pass estimate for the bias components, select C_{DRVCC} = 4.7µF, C_{INTVCC} = 0.1µF, boost supply capacitor C_B = 0.1µF and low leakage boost supply diode CMPD3003A from Central Semiconductor.

9. Determine and set application-specific parameters. Set the MODE pin based on the trade-off of light load efficiency and constant frequency operation. Set the PLLIN/SPREAD pin based on whether a fixed, spread spectrum, or phase-locked frequency is desired. The RUN and OVLO pins can be used to control the input voltage window within which the regulator operates. Use ITH compensation components from the typical applications as a first guess, check the transient response for stability, and modify as necessary.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. Figure 13 illustrates the current waveforms present in the various branches of the two-phase synchronous buck regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs MTOP1 and MTOP2 located within 1cm of each other with a common drain connection at C_{IN}? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.

2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{DRVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, bottom N-channel MOSFET and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the loop described above.

APPLICATIONS INFORMATION

3. Does the LTC7810's V_{FB} pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
5. Is the DRV_{CC} and decoupling capacitor connected close to the IC, between the DRV_{CC} and the ground pin? This capacitor carries the MOSFET drivers' current peaks.
6. Keep the switching nodes (SW1, SW2), top gate (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposite channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the output side of the LTC7810 and occupy minimum PC trace area.
7. Use a modified star ground technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the DRV_{CC} decoupling capacitor, the bottom of the voltage feedback resistive divider and the GND pin of the IC.

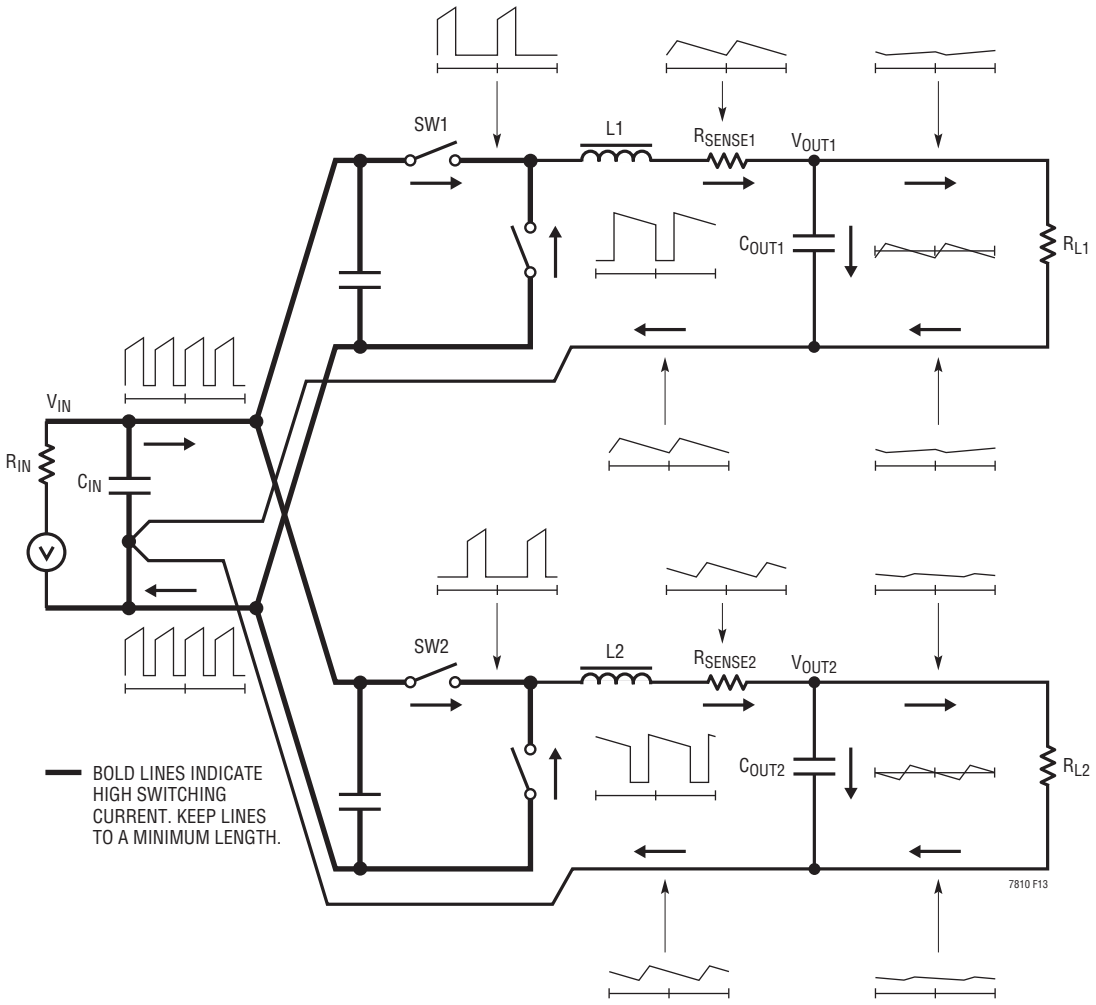


Figure 13. Branch Current Waveforms

APPLICATIONS INFORMATION

PC Board Layout Debugging

Start with one controller at a time. It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold - typically 25% of the maximum designed current level in Burst Mode operation.

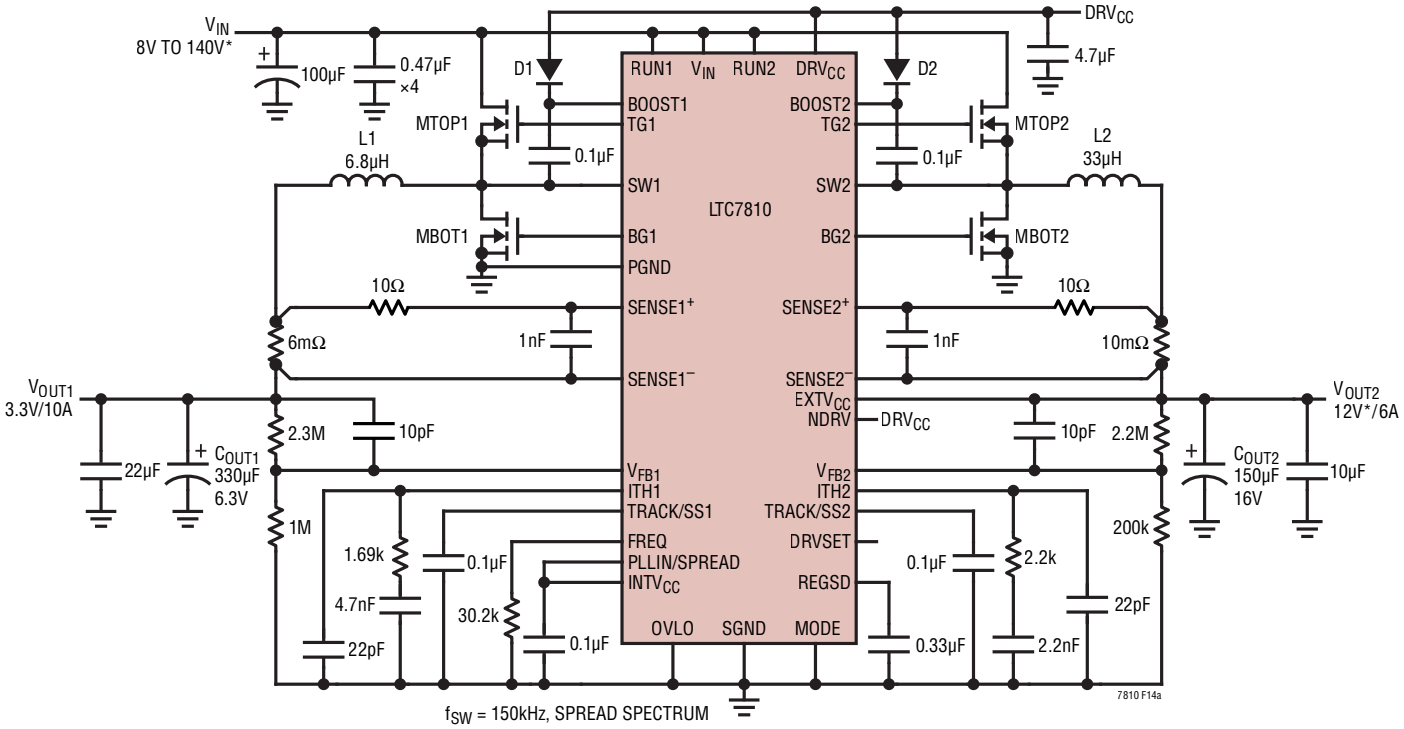
The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. Only after each controller is checked for its individual performance should both controllers be turned on at the same time. A particularly difficult region of operation is when one channel is nearing its current comparator trip point when the other channel is turning on its top MOSFET. This occurs around 50% duty cycle on either channel due to the phasing of the internal clocks and may cause minor duty cycle jitter.

Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, the top MOSFET, and the bottom MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

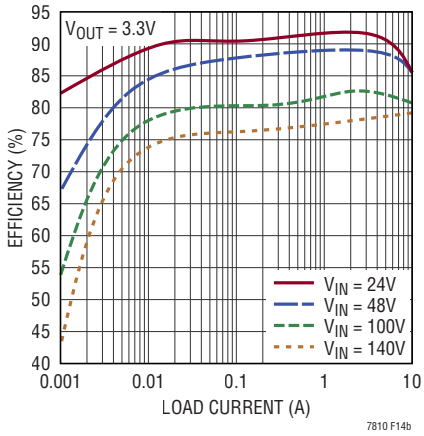
An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS

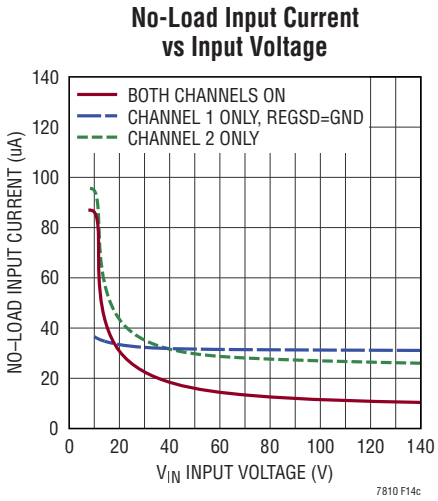


* V_{OUT2}, FOLLOWS V_{IN} WHEN V_{IN} IS LESS THAN THE REGULATION POINT
MTOP1,2, MBOT2: INFINEON BSC520N15NS3G
MBOT1: INFINEON BSC190N15NS3G
D1,2: CENTRAL SEMI CMHD3595
L1: COILCRAFT SER2915L-682KL
L2: WURTH 7443633300
C_{OUT1}: KEMET T520V337M006ATE025
C_{OUT2}: KEMET T521D157M016ATE050

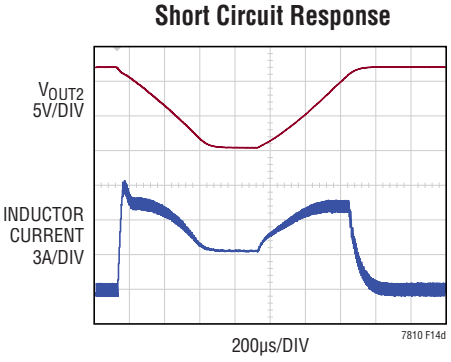
(14a)



(14b)



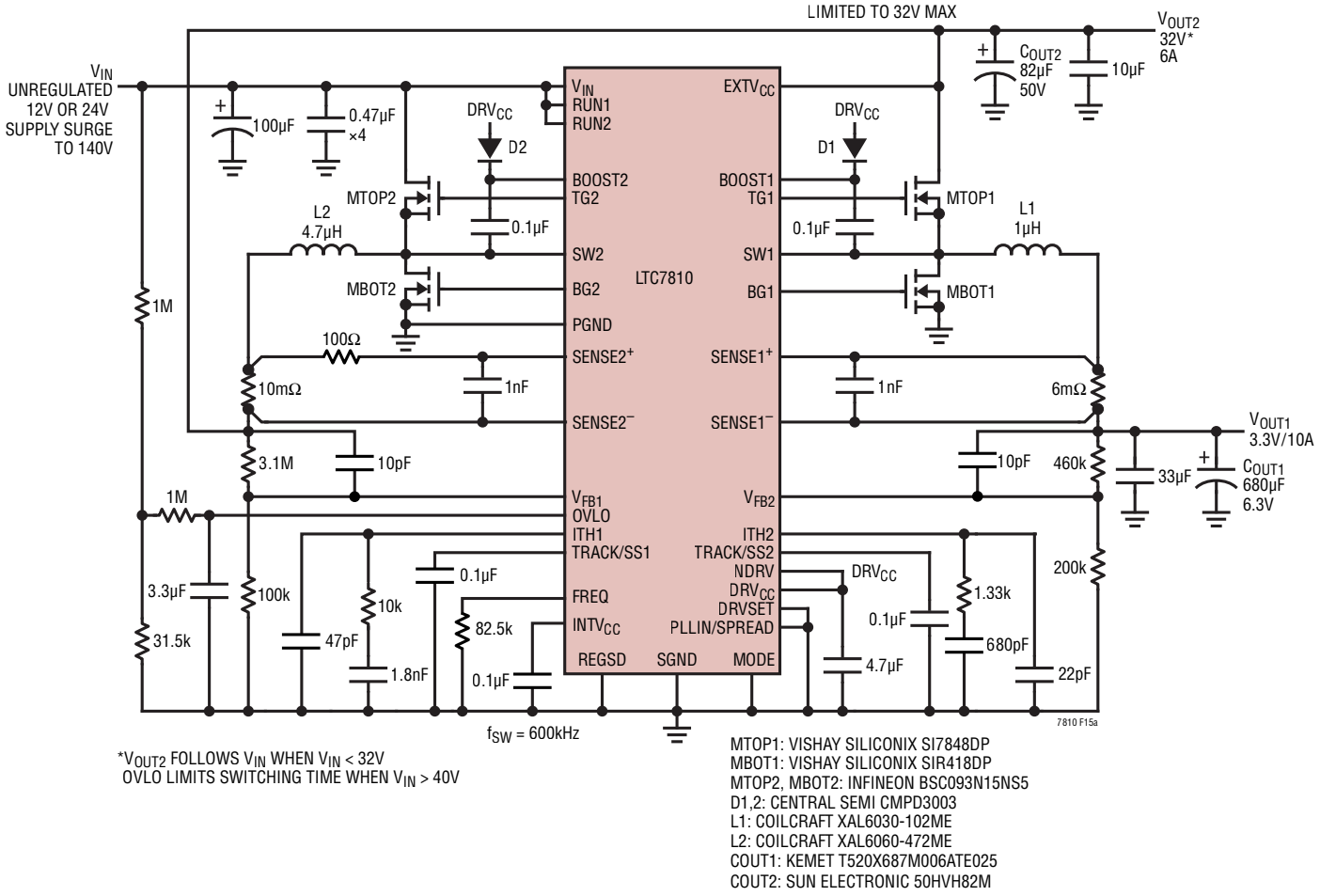
(14c)



(14d)

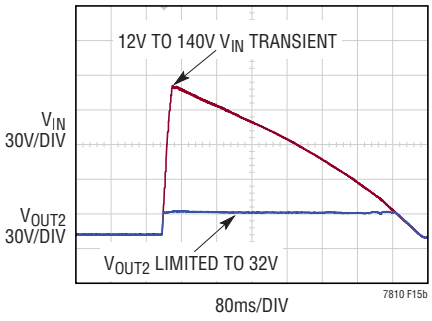
Figure 14. High Efficiency Dual 3.3V/12V Step-Down Regulator with Spread Spectrum

TYPICAL APPLICATIONS



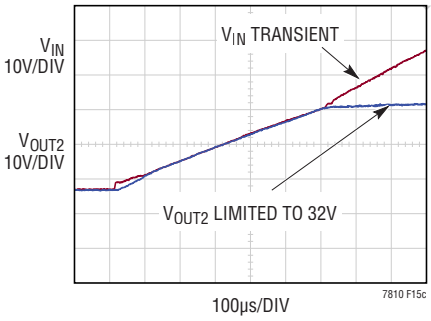
(15a)

Surge Transient Response



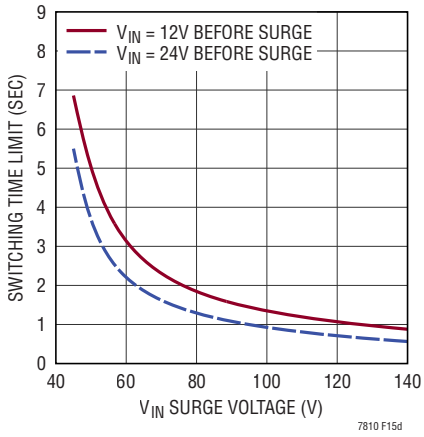
(15b)

Surge Transient Response



(15c)

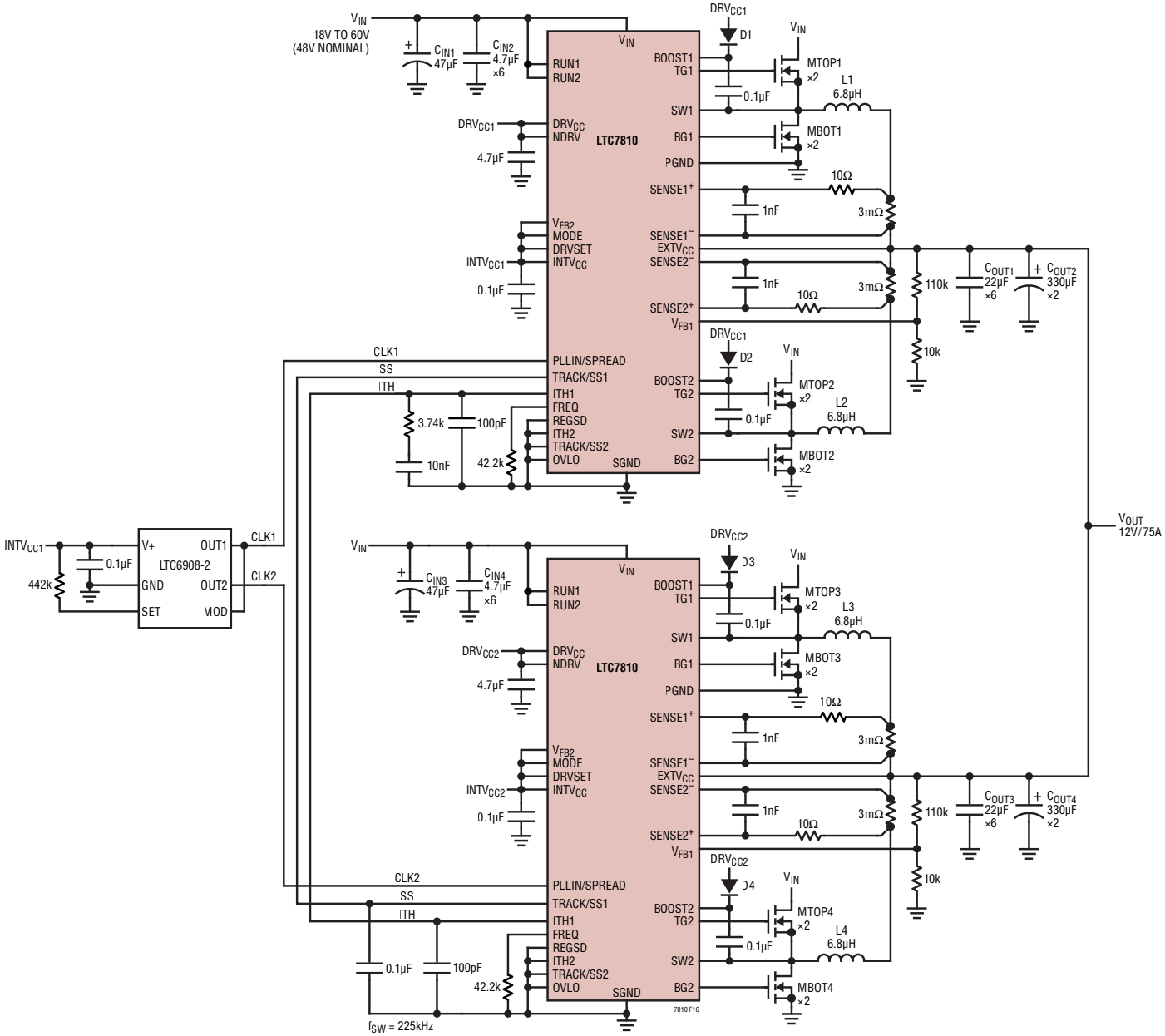
Switching Time Limit vs Input Voltage Surge



(15d)

Figure 15. Small Size High Efficiency Switching Surge Stopper and 3.3V/10A Regulator

TYPICAL APPLICATIONS

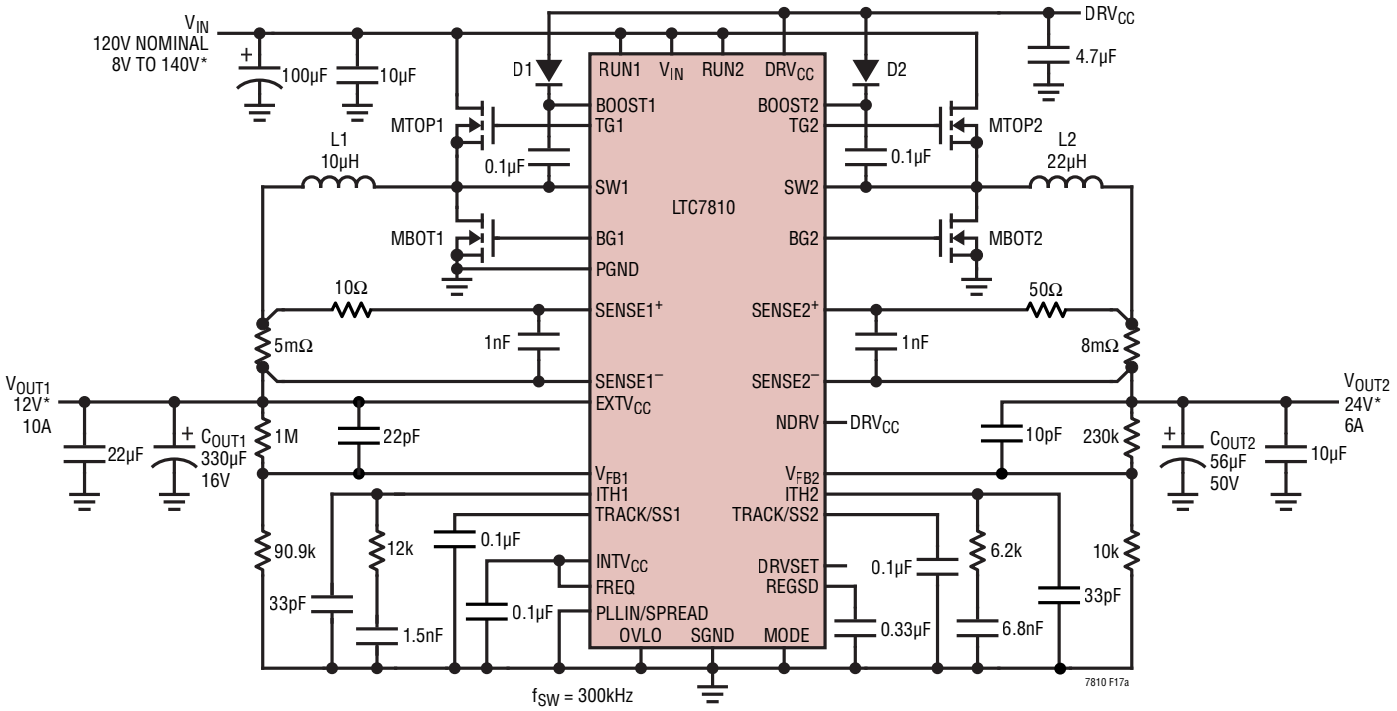


MTOP1,2,3,4: INFINEON BSC340N08NS3
MBOT1,2,3,4: INFINEON BSC042NE7NS3
D1,2,3,4: CENTRAL SEMI CMDP3003
L1,2,3,4: COILCRAFT SER2918H-682KL

C_{IN1},C_{IN3}: SUN 100CE47LX
C_{IN2},C_{IN4}: TDK CGA6M3X7S2A475M200AB
C_{OUT1},C_{OUT3}: MURATA GRM32ER71E226ME15L
C_{OUT2},C_{OUT4}: SUN 25HVH330M

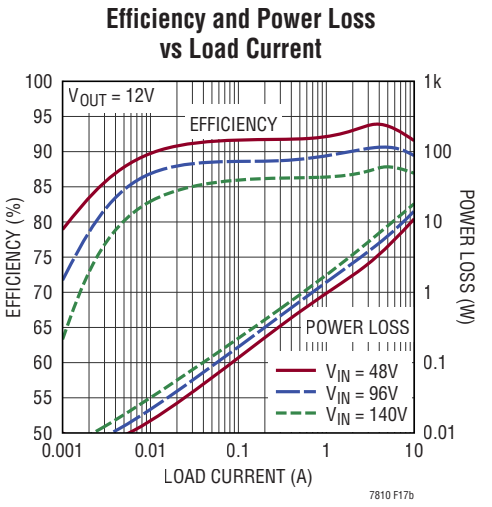
Figure 16. High Efficiency Four Phase Single Output 12V/75A (900W) Step-Down Regulator

TYPICAL APPLICATIONS

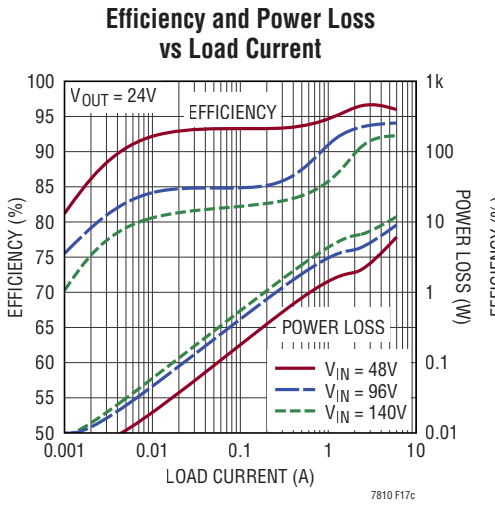


* V_{OUT1}, V_{OUT2} FOLLOW V_{IN} WHEN V_{IN} IS LESS THAN THE REGULATION POINT
MTOP1,2: INFINEON BSC520N15NS3G
MBOT1,2: INFINEON BSC360N15NS3G
D1,2: CENTRAL SEMI CMPD3003
L1: VISHAY IHLP6767GZER100M11
L2: VISHAY IHLP6767GZER220M11
C_{OUT1}: KEMET T521X337MO16ATE025
C_{OUT2}: SUN ELECTRONIC 50HVH56M

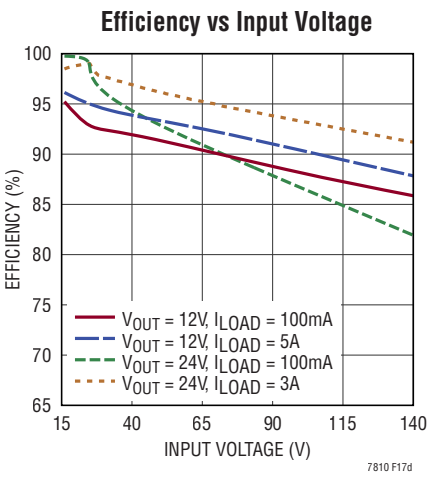
(17a)



(17b)



(17c)



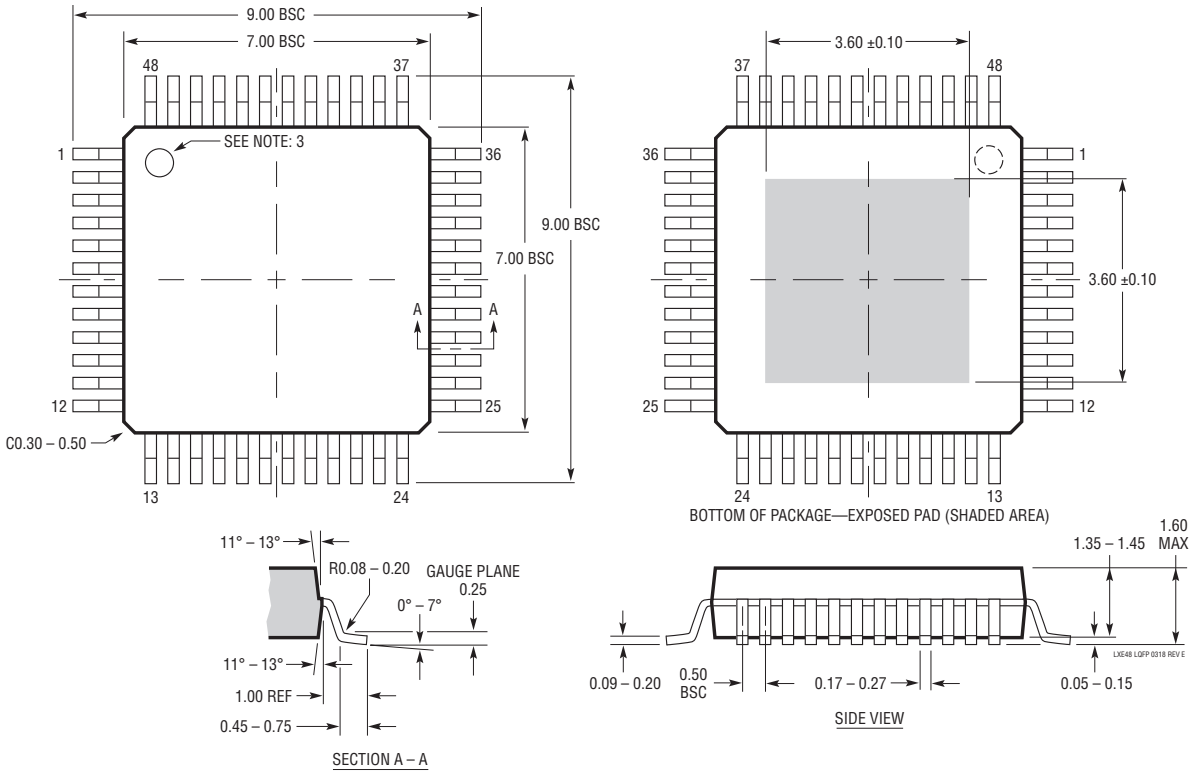
(17d)

Figure 17. High Efficiency High Voltage Dual 24V/12V Step-Down Regulator

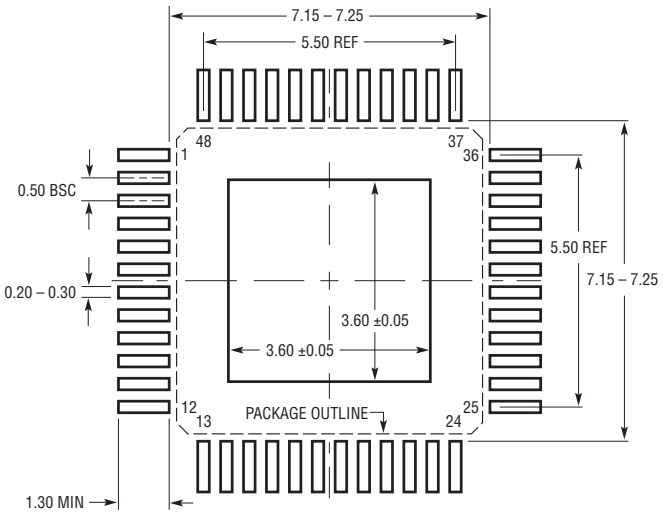
PACKAGE DESCRIPTION

Please refer to http://www.adi.com/designtools/packaging/ for the most recent package drawings.

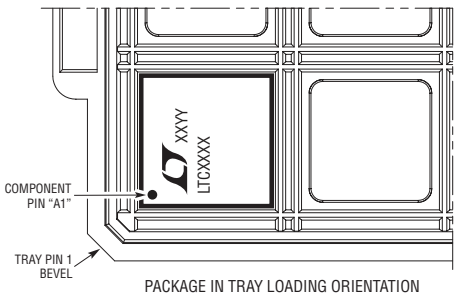
LXE Package
48-Lead Plastic Exposed Pad LQFP (7mm × 7mm)
(Reference LTC DWG #05-08-1832 Rev E)
Exposed Pad Variation BB



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DIMENSIONS OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.25mm (10 MILS) BETWEEN THE LEADS AND ON ANY SIDE OF EXPOSED PAD, MAX 0.50mm (20 MILS) AT CORNER OF EXPOSED PAD, IF PRESENT
3. PIN-1 INDENTIFIER IS A MOLDED INDENTATION
4. DRAWING IS NOT TO SCALE



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



PACKAGE IN TRAY LOADING ORIENTATION

Rev. B

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	04/19	Corrected Figure 9 and Figure 16 schematics	25, 37
B	10/22	Added AEC-Q100 Qualified	1
		Added #W Flow Part Number	3

TYPICAL APPLICATION

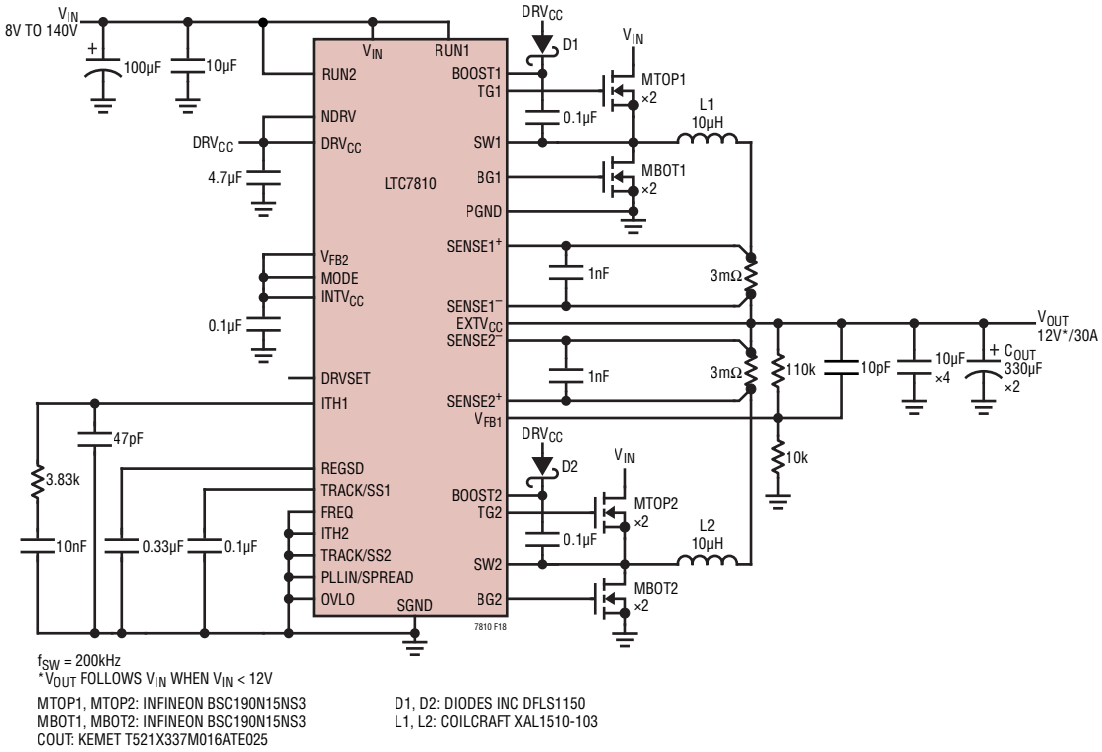


Figure 18. High Efficiency 360W Two Phase Single Output 12V Step-Down Regulator

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC7801/ LTC3895	150V Low I_Q, Synchronous Step-Down DC/DC Controller with 100% Duty Cycle	4V ≤ V_{IN} ≤ 140V, 150V Absolute Maximum, PLL Fixed Frequency 50kHz to 900kHz, 0.8V ≤ V_{OUT} ≤ 60V, Adjustable 5V to 10V Gate Drive, I_Q = 40µA, 4mm × 5mm QFN-24, TSSOP-24, TSSOP-38(31)
LTC7103	105V, 2.3A Low EMI Synchronous Step-Down Regulator	4.4V ≤ V_{IN} ≤ 105V, 1V ≤ V_{OUT} ≤ V_{IN}, I_Q = 2µA Fixed Frequency 200kHz to 2MHz, 5mm × 6mm QFN
LTC3638	High Efficiency, 140V 250mA Step-Down Regulator	Integrated Power MOSFETs, 4V≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC3896	150V Low I_Q, Synchronous Inverting DC/DC Controller with Ground-Referenced Control/Interface Pins	4V ≤ V_{IN} ≤ 140V, 150V Absolute Maximum, PLL Fixed Frequency 50kHz to 900kHz, –0.8V ≤ V_{OUT} ≤ –60V, Adjustable 5V to 10V Gate Drive, I_Q = 40µA
LTC3892/ LTC3892-1	60V Low I_Q, Dual, 2-Phase Synchronous Step-Down DC/DC Controller with 99% Duty Cycle	4V ≤ V_{IN} ≤ 60V, PLL Fixed Frequency 50kHz to 900kHz, 0.8V ≤ V_{OUT} ≤ 0.99V_{IN}, Adjustable 5V to 10V Gate Drive, I_Q = 29µA
LTC3639	High Efficiency, 150V 100mA Synchronous Step-Down Regulator	Integrated Power MOSFETs, 4V≤ V_{IN} ≤ 150V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LT8631	100V, 1A Synchronous Micropower Step-Down Regulator	Integrated Power MOSFETs, 3V≤ V_{IN} ≤ 100V, 0.8V ≤ V_{OUT} ≤ 60V, I_Q = 7µA, TSSOP-20
LTC7138	High Efficiency, 140V 400mA Step-Down Regulator	Integrated Power MOSFETs, 4V≤ V_{IN} ≤ 140V, 0.8V ≤ V_{OUT} ≤ V_{IN}, I_Q = 12µA, MSOP-16(12)
LTC3899	60V Triple Output, Buck/Buck/Boost Synchronous Controller with 30µA Burst Mode I_Q	4.5V (Down to 2.2V After Start-Up) ≤ V_{IN} ≤ 60V, Buck V_{OUT} Range: 0.8V to 60V, Boost V_{OUT} Up to 60V
LTC7860	High Efficiency Switching Surge Stopper	3.5V ≤ V_{IN} ≤ 60V, Expandable to 200V+, Adjustable V_{OUT} Clamp and Current Limit, Power Inductor Improves EMI, MSOP-12