Octal Bus Buffer/Line Driver
Inverting with 3-State Outputs

MC74VHC240

The MC74VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74VHC240 is an inverting 3–state buffer, and has two active–low output enables. This device is designed to drive bus lines or buffer memory address registers.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7V, allowing the interface of 5V systems to 3V systems.

- High Speed: t_{PD} = 3.6ns (Typ) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA (Max) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2V to 5.5V Operating Range
- Low Noise: V_{OLP} = 0.9V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300mA
- ESD Performance: HBM > 2000V; Machine Model > 200V
- Chip Complexity: 120 FETs or 30 Equivalent Gates

DW SUFFIX
20–LEAD SOIC WIDE PACKAGE
CASE 751D–04

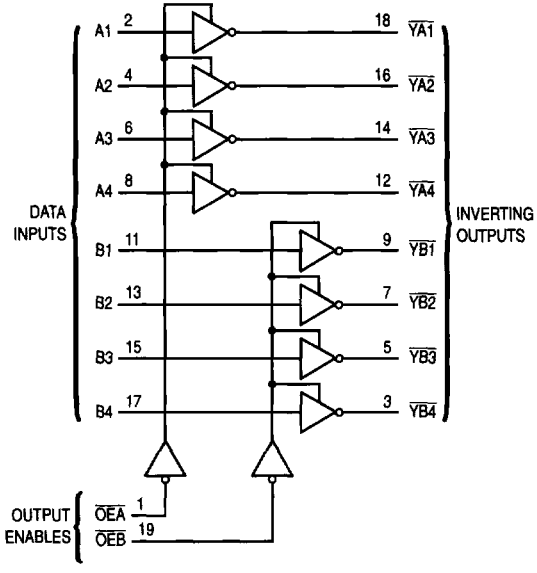
DT SUFFIX
20–LEAD TSSOP PACKAGE
CASE 948E–02

M SUFFIX
20–LEAD SOIC EIAJ PACKAGE
CASE 967–01

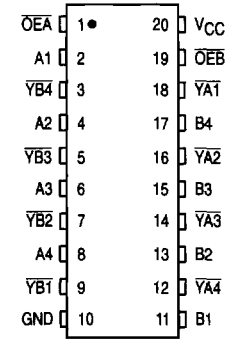
ORDERING INFORMATION

MC74VHCXXXDW	SOIC WIDE
MC74VHCXXXDT	TSSOP
MC74VHCXXXM	SOIC EIAJ

LOGIC DIAGRAM



PIN ASSIGNMENT



FUNCTION TABLE

INPUTS		OUTPUTS
$\overline{OEA}$, $\overline{OEB}$	A, B	$\overline{YA}$, $\overline{YB}$
L	L	H
L	H	L
H	X	Z

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	– 0.5 to + 7.0	V
V_{in}	DC Input Voltage	– 0.5 to + 7.0	V
V_{out}	DC Output Voltage	– 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	– 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 75	mA
P_D	Power Dissipation in Still Air, SOIC Packages†	500	mW
	TSSOP Package†	450	
T_{stg}	Storage Temperature	– 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: – 7 mW/°C from 65° to 125°C
TSSOP Package: – 6.1 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		– 40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V	0	100	ns/V
		V_{CC} =5.0V ±0.5V	0	20	

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = – 40 to 85°C Min	T_A = – 40 to 85°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 to 5.5	1.50 V_{CC} x 0.7			1.50 V_{CC} x 0.7		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 to 5.5			0.50 V_{CC} x 0.3		0.50 V_{CC} x 0.3	V
V_{OH}	Minimum High–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = – 50µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		V
		V_{in} = V_{IH} or V_{IL} I_{OH} = – 4mA I_{OH} = – 8mA	3.0 4.5	2.58 3.94			2.48 3.80		
V_{OL}	Maximum Low–Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OL} = 50µA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} I_{OL} = 4mA I_{OL} = 8mA	3.0 4.5			0.36 0.36		0.44 0.44	
I_{in}	Maximum Input Leakage Current	V_{in} = 5.5V or GND	0 to 5.5			± 0.1		± 1.0	µA

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C			T_A = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I_{OZ}	Maximum Three–State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5			± 0.25		± 2.5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{in} = V_{CC} or GND	5.5			4.0		40.0	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns)

Symbol	Parameter	Test Conditions	T_A = 25°C			T_A = – 40 to 85°C		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, A to $\overline{YA}$ or B to $\overline{YB}$	V_{CC} = 3.3 ± 0.3V C_L = 15pF		5.3	7.5	1.0	9.0	ns
		V_{CC} = 3.3 ± 0.3V C_L = 50pF		7.8	11.0	1.0	12.5	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF		3.6	5.5	1.0	6.5	
		V_{CC} = 5.0 ± 0.5V C_L = 50pF		5.1	7.5	1.0	8.5	
t_{PZL}, t_{PZH}	Output Enable Time $\overline{OEA}$ to $\overline{YA}$ or $\overline{OEB}$ to $\overline{YB}$	V_{CC} = 3.3 ± 0.3V C_L = 15pF R_L = 1kΩ		6.6	10.6	1.0	12.5	ns
		V_{CC} = 3.3 ± 0.3V C_L = 50pF R_L = 1kΩ		9.1	14.1	1.0	16.0	
		V_{CC} = 5.0 ± 0.5V C_L = 15pF R_L = 1kΩ		4.7	7.3	1.0	8.5	
		V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		6.2	9.3	1.0	10.5	
t_{PLZ}, t_{PHZ}	Output Disable Time $\overline{OEA}$ to $\overline{YA}$ or $\overline{OEB}$ to $\overline{YB}$	V_{CC} = 3.3 ± 0.3V C_L = 50pF R_L = 1kΩ		10.3	14.0	1.0	16.0	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50pF R_L = 1kΩ		6.7	9.2	1.0	10.5	
t_{OSLH}, t_{OSHL}	Output to Output Skew	V_{CC} = 3.3 ± 0.3V C_L = 50pF (Note 1.)			1.5		1.5	ns
		V_{CC} = 5.0 ± 0.5V C_L = 50pF (Note 1.)			1.0		1.0	
C_{in}	Maximum Input Capacitance			4	10		10	pF
C_{out}	Maximum Three–State Output Capacitance (Output in High–Impedance State)			6				pF

		Typical @ 25°C, V_{CC} = 5.0V	
C_{PD}	Power Dissipation Capacitance (Note 2.)	17	pF

1. Parameter guaranteed by design. $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$.
2. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0ns, C_L = 50pF, V_{CC} = 5.0V)

Symbol	Parameter	T_A = 25°C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.6	0.9	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	– 0.6	– 0.9	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		3.5	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		1.5	V

SWITCHING WAVEFORMS

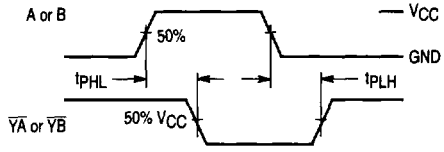


Figure 1.

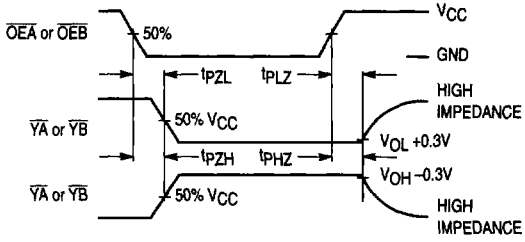
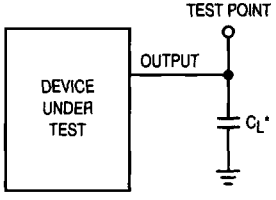


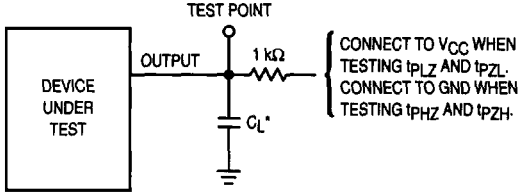
Figure 2.

TEST CIRCUITS



* Includes all probe and jig capacitance

Figure 3. Test Circuit



* Includes all probe and jig capacitance

Figure 4. Test Circuit

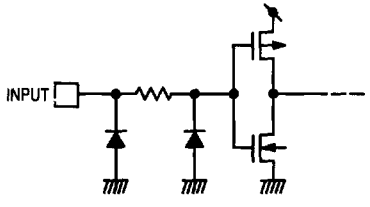


Figure 5. Input Equivalent Circuit